TRIPLE SYNCHRONOUS BUCK CONTROLLER WITH NMOS LDO CONTROLLER

FEATURES

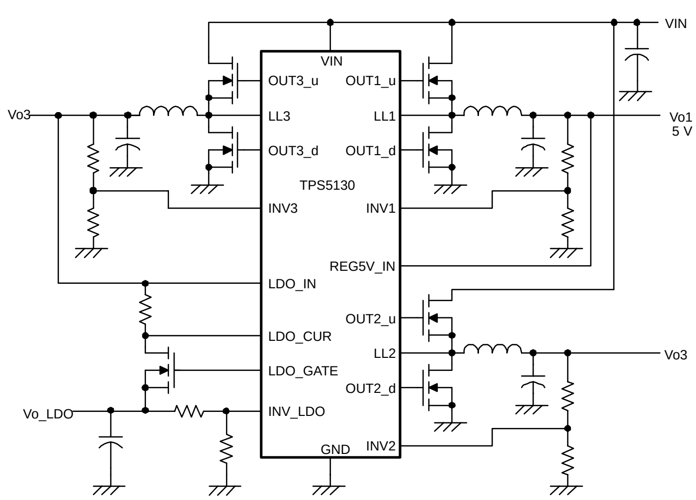
- **Three Independent Step-Down DC/DC Controllers and One LDO Controller**
- **Input Voltage Range**
  - **Switcher: 4.5 V ~ 28 V**
  - **LDO: 1.1 V ~ 3.6 V**
- **Output Voltage Range**
  - **Switcher: 0.9 V ~ 5.5 V**
  - **LDO: 0.9 V ~ 2.5 V**
- **Synchronous for High Efficiency**
- **Precision V_{ref} (±1.5%)**
- **PWM Mode Control : Max. 500 kHz Operation**
- **Auto PWM/SKIP Mode Available**
- **High Speed Error Amplifier**
- **Over Current Protection With Temperature Compensation Circuit for Each Channel**
- **Overvoltage and Undervoltage Protection**
- **Programmable Short-Circuit Protection**
- **Powergood With Programmable Delay Time**
- **5-V and 3.3-V Linear Regulators**

APPLICATIONS

- **Notebook PCs, PDAs**
- **Consumer Game Systems**
- **DSP Application**

DESCRIPTION

The TPS5130 is composed of three independent synchronous buck regulator controllers (SBRC) and one low drop-out (LDO) regulator controller. On-chip high-side and low-side synchronous rectifier drivers are integrated to drive less expensive N-channel MOSFETs. The LDO controller can also drive an external N-channel MOSFET. Since the input current ripple is minimized by operating 180 degree out of phase, it allows a smaller input capacitance resulting in reduced power supply cost. The SBRC of the TPS5130 automatically adjusts from PWM mode to SKIP mode to maintain high efficiency under light load conditions. Resistor-less current protection for the synchronous buck controller and the fixed high-side driver voltage simplifies the system design and reduces the external parts count. The LDO controller has a current limit protection and overshoot protection to suppress output voltage hump at load transient. To further extend battery life, the TPS5130 features dead-time control and very low quiescent current.



See application section of this data sheet for more detailed information.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES PLASTIC TQFP (PT)[1]
–40°C to 85°C	TPS5130PT

(1) The PT package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS5130PTR).

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
48 pin PT	3210 mW	25.7 mW/°C	1670 mW

(1) These devices are mounted on a JEDEC high-k board (2 oz. traces on surface, 2-layer 1 oz. plane inside). (Assumes the maximum junction temperature is 150°C)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		TPS5130
Supply voltage, [2] VIN		–0.3 V to 30 V
Input voltage range[2], V_I	LH1/2/3	–0.3 V to 35 V
	VIN_SENSE12/3, LL1/2/3, STBY_LDO, STBY_VREF3.3/5, TRIP1/2/3	–0.3 V to 30 V
	INV1/2/3, CT, SS_STBY1/2/3, INV_LDO, LDO_OUT, FLT, PG_DELAY, VREF3.3/5, LDO_IN, LDO_CUR, PWM_SEL, REG5V_IN	–0.3 V to 7 V
Output voltage range, V_O [2]	OUT1/2/3_u	–0.3 V to 35 V
	FB1/2/3, PGOUT, OUT1/2/3_d	–0.3 V to 7 V
	LDO_GATE	–0.3 V to 9 V
	REF	–0.3 V to 3 V
Operating ambient temperature range, T_A		–40°C to 85°C
Storage temperature, T_{stg}		–55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	VIN	4.5		28	V
	LDO_IN	1.1		3.6	V
	REG5V_IN	4.5		5.5	V
Input voltage, V_I	OUT1/2/3_u, LH1/2/3	–0.1		33	V
	VIN_SENSE1/2/3	4.5		28	V
	STBY_LDO, LL1/2/3, TRIP, STBY_VREF3.3/5	–0.1		28	V
	LDO_GATE	–0.1		8	V
	INV1/2/3, INV_LDO, CT, PWM_SEL, FLT, PG_DELAY, SS_STBY1/2/3	–0.1		6	V
	PGOUT, FB1/2/3, OUT1/2/3_d	–0.1		5.5	V
	LDO_CUR, LDO_OUT	–0.1		3.5	V
Oscillator frequency, f_{osc}			300	500	kHz
Operating free-air temperature, T_A		–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{(VIN)} = V_{(VIN\_SENSE12)} = V_{(VIN\_SENSE3)}$ = 12 V (unless otherwise noted)

Supply Current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	T_A = 25°C, $V_{(LDO\_IN)}$ = 3.6 V, $V_{(CT)} = V_{(INVx)} = V_{(INV\_LDO)}$ = 0 V, $V_{(PWM\_SEL)}$ = 0 V		2	3	mA
$I_{CC(STBY)}$	Standby current	$V_{(SS\_STBYx)}$ = 0 V, $V_{(STBY\_LDO)}$ = 0V, $V_{(STBY\_VREF3.3/5)}$ = 5 V		150	250	µA
$I_{CC(S)}$	Shutdown current	$V_{(SS\_STBYx)}$ = 0 V, $V_{(STBY\_LDO)}$ = 0V, $V_{(STBY\_VREF3.3/5)}$ = 0 V		0.001	10	µA

Reference Voltage

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Reference voltage				0.85		V
$V_{ref(tol)}$	Reference voltage tolerance	T_A = 25°C,	I_{ref} = 50 µA	–1.5%		1.5%	
		T_A = 0°C to 85°C,	I_{ref} = 50 µA	–2%		2%	
		T_A = –40°C to 85°C,	I_{ref} = 50 µA	–2.5%		2.5%	
	Line regulation	$V_{(VIN)}$ = 4.5 V to 28 V,	I_{ref} = 50 µA		0.05	5	mV
	Load regulation	I_{ref} = 0.1 µA to 1 mA			0.15	5	mV

5 V Internal Switch

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{T(LH)}$	Threshold voltage	High	REG5V_IN voltage	4.2		4.8	V
$V_{T(HL)}$		Low		4.1		4.7	V
V_{hys}	Hysteresis		REG5V_IN voltage	30		200	mV

VREF5

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage		I_O = 0 mA to 50 mA, $V_{(VIN)}$ = 5.5 V to 28 V,	T_A = 25°C	4.8		5.2	V
	Line regulation		$V_{(VIN)}$ = 5.5 V to 28 V,	I_O = 10 mA			20	mV
	Load regulation		I_O = 1 mA to 10 mA,	$V_{(VIN)}$ = 5.5 V			40	mV
I_{OS}	Short-circuit output current		$V_{(VREF5)}$ = 0 V,	T_A = 25°C	65			mA
$V_{T(LH)}$	UVLO threshold voltage	High	VREF5 voltage		3.6		4.2	V
$V_{T(HL)}$		Low			3.5		4.1	V
V_{hys}	Hysteresis		VREF5 voltage		30		200	mV

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{(VIN)} = V_{(VIN\_SENSE12)} = V_{(VIN\_SENSE3)} = 12$ V (unless otherwise noted)

VREF3.3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	I_O = 0 mA to 30 mA, $V_{(VIN)}$ = 5.5 V to 28 V, T_A = 25°C	3.15	3.30	3.45	V
	Line regulation	$V_{(VIN)}$ = 5.5 V to 28 V, I_O = 10 mA			20	mV
	Load regulation	I_O = 1 mA to 10 mA, $V_{(VIN)}$ = 5.5 V			40	mV
I_{OS}	Short circuit output current	$V_{(VREF3.3)}$ = 0 V, T_A = 25°C	–30			mA

Control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	SS_STBYx, STBY_LDO, PWM_SEL, STBY_VREF3.3/5	2.2			V
V_{IL}	Low-level input voltage	SS_STBYx, STBY_LDO, PWM_SEL, STBY_VREF3.3/5			0.3	V

Output Voltage Monitor

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP comparator threshold	SBRC, LDO	0.91	0.95	0.99	V
UVP comparator threshold	SBRC, LDO	0.51	0.55	0.59	V
PG comparator low-level threshold		0.75	0.79	0.81	V
PG comparator high-level threshold		0.88	0.91	0.94	V
PG propagation delay from INVx, INV_LDO to PGOUT (no load at PG_DELAY)	Powergood H to L		6.5		µs
	Powergood L to H		16		
$I_{(PG\_DELAY)}$ PG_DELAY source current			–1.8		µA
Timer latch current source	UVP protection	–1.5	–2.3	–3.1	µA
	OVP protection	–80	–125	–180	

Oscillator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	Oscillation frequency	PWM mode, $C_{(CT)}$ = 44 pF, T_A = 25°C		300		kHz
V_{OH}	High level output voltage	dc	1	1.1	1.2	V
		f_{osc} = 300 kHz		1.17		
V_{OL}	Low level output voltage	dc	0.4	0.5	0.6	V
		f_{osc} = 300 kHz		0.43		

Error Amplifier for SBRC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	INVx voltage, T_A = 25°C		2	10	mV
	Open loop voltage gain		50			dB
	Unity-gain bandwidth			2.5		MHz
$I_{O(snk)}$	Output sink current	$V_{(FBx)}$ = 1 V	0.2	0.7		mA
$I_{O(src)}$	Output source current	$V_{(FBx)}$ = 1 V	–0.2	–0.9		mA

Duty Control

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum duty control	CH1/3, f_{osc} = 300 kHz, $V_{(INVx)}$ = 0 V		82%		
	CH2, f_{osc} = 300 kHz, $V_{(INVx)}$ = 0 V		97%		

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{(VIN)} = V_{(VIN\_SENSE12)} = V_{(VIN\_SENSE3)}$ = 12 V (unless otherwise noted)

Output Drivers

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	OUT_u sink current	$V_{(OUTx\_u)} - V_{(LLx)}$ = 3 V		1.2		A
	OUT_u source current	$V_{(LHx)} - V_{(OUTx\_u)}$ = 3 V		–1.2		A
	OUT_d sink current	$V_{(OUTx\_d)}$ = 3 V		1.5		A
	OUT_d source current	$V_{(OUTx\_d)}$ = 2 V		–1.5		A
	LDO_GATE sink current	$V_{(LDO\_GATE)}$ = 2 V		2		mA
	LDO_GATE source current	$V_{(LDO\_GATE)}$ = 2 V		–1.4		mA
$I_{(TRIPx)}$	TRIP current	T_A = 25°C	11	13	15	µA

Soft Start

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SS\_STBYx)}$	Soft start current	$V_{(SS\_STBYx)}$ = 0.7 V	–1.6	–2.3	–2.9	µA

Error Amplifier for LDO Controller

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{(LDO\_IN)}$ = 3.3 V, T_A = 25 °C		2	10	mV
	Open loop voltage gain	$V_{(LDO\_IN)}$ = 3.3 V	50			dB
	Unity-gain bandwidth	$V_{(LDO\_IN)}$ = 3.3 V, C_L = 2000 pF		1.4		MHz

Current Limit for LDO Controller

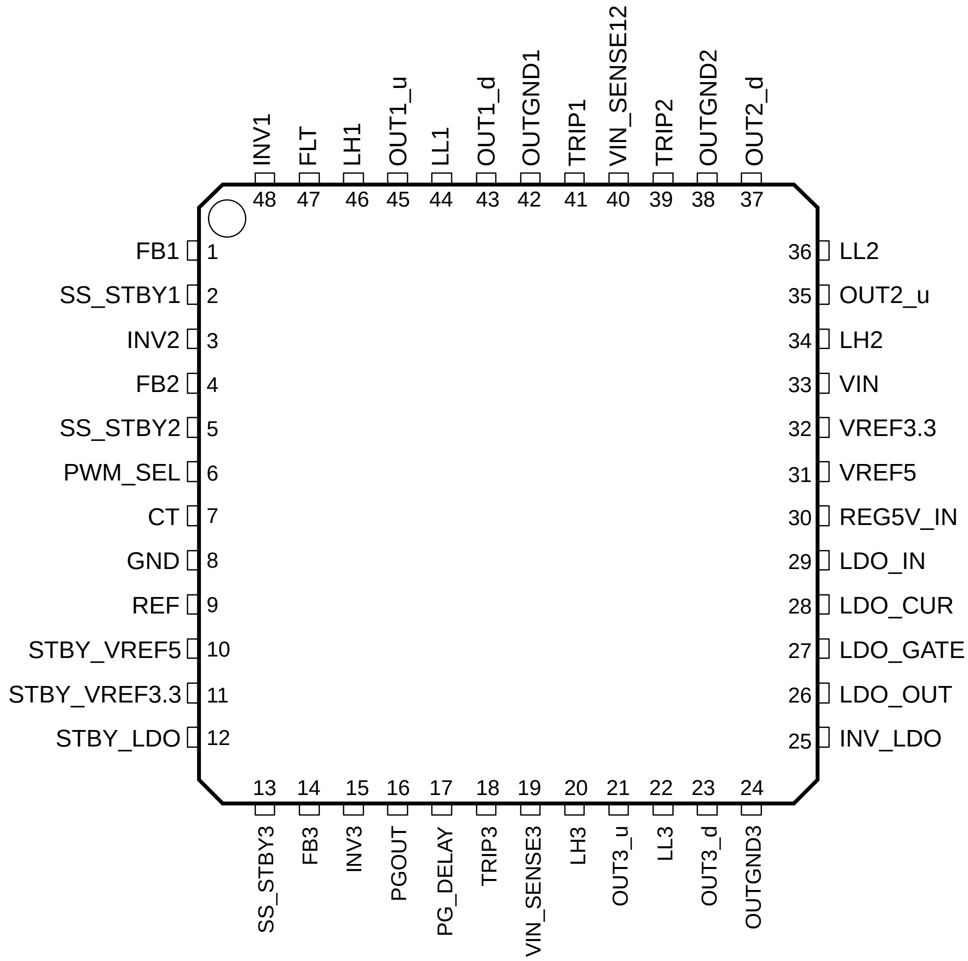
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current limit comparator threshold voltage	$V_{(LDO\_IN)}$ = 3.3 V	40	50	60	mV

Overshoot Protection for LDO Controller

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO_OUT sink current	$V_{(LDO\_OUT)} = V_{(LDO\_GATE)}$ = 1.5 V		25		mA

PIN ASSIGNMENTS

PT
(TOP VIEW)



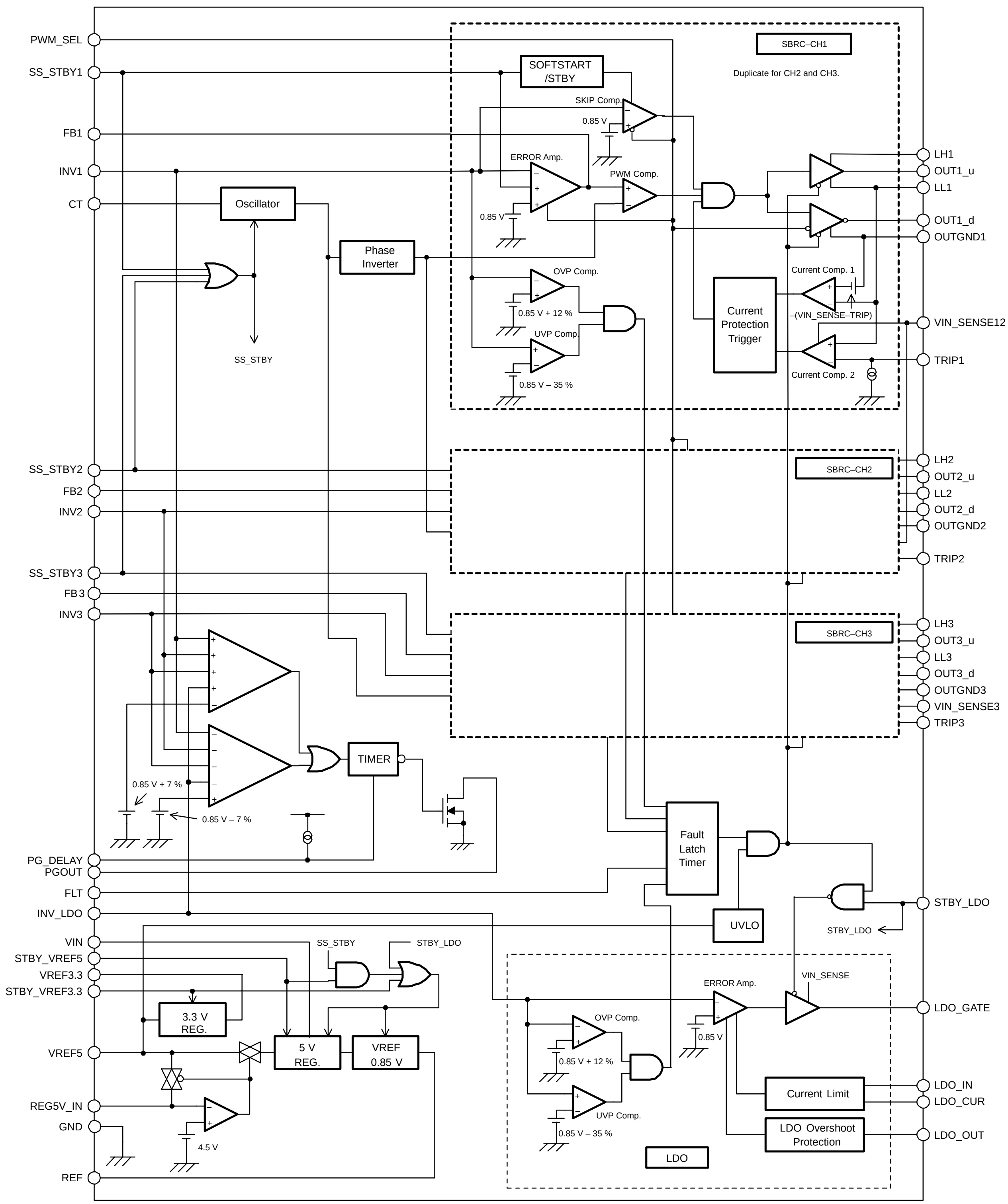
Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CT	7	I/O	External capacitor from CT to GND adjusts frequency of the triangle oscillator.
FB1	1	O	Feedback output of SBRC-CH1 error amplifier
FB2	4	O	Feedback output of SBRC-CH2 error amplifier
FB3	14	O	Feedback output of SBRC-CH3 error amplifier
FLT	47	I/O	Fault latch timer pin. An external capacitor connected between FLT and GND sets FLT enable time up.
GND	8	–	Signal GND
INV1	48	I	Inverting inputs of SBRC-CH1 error amplifier, skip comparator, OVP1/UVP1 comparator and PG comparator
INV2	3	I	Inverting inputs of SBRC-CH2 error amplifier, skip comparator, OVP2/UVP2 comparator and PG comparator
INV3	15	I	Inverting inputs of SBRC-CH3 error amplifier, skip comparator, OVP3/UVP3 comparator and PG comparator
INV_LDO	25	I	Inverting inputs of LDO error amplifier, OVP/UVP comparators and PG comparator.
LDO_CUR	28	I	Current sense input of LDO regulator.
LDO_GATE	27	O	Gate control output of external MOSFET for LDO regulator
LDO_OUT	26	I/O	LDO regulator's output connection. If output voltage has an overshoot when output current changes high to low quickly, it absorbs electrical charge from this pin.
LDO_IN	29	I	Supply voltage input and current sense input of LDO regulator

Terminal Functions (Continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
LH1	46	I/O	Bootstrap capacitor connection for SBRC-CH1 high-side gate driver.
LH2	34	I/O	Bootstrap capacitor connection for SBRC-CH2 high-side gate driver.
LH3	20	I/O	Bootstrap capacitor connection for SBRC-CH3 high-side gate driver.
LL1	44	I/O	SBRC-CH1 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator.
LL2	36	I/O	SBRC-CH2 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator.
LL3	22	I/O	SBRC-CH3 high-side gate driving return. Connect this pin to the junction of the high-side and low-side MOSFETs for floating drive configuration. This pin is also an input terminal for current comparator.
OUT1_d	43	O	Gate drive output for SBRC-CH1 low-side MOSFETs
OUT2_d	37	O	Gate drive output for SBRC-CH2 low-side MOSFETs
OUT3_d	23	O	Gate drive output for SBRC-CH3 low-side MOSFETs
OUT1_u	45	O	Gate drive output for SBRC-CH1 high-side MOSFETs.
OUT2_u	35	O	Gate drive output for SBRC-CH2 high-side MOSFETs.
OUT3_u	21	O	Gate drive output for SBRC-CH3 high-side MOSFETs.
OUTGND1	42	O	Ground for SBRC-CH1 MOSFETs drivers. It is connected to the current limiting comparator's negative input.
OUTGND2	38	O	Ground for SBRC-CH2 MOSFETs drivers. It is connected to the current limiting comparator's negative input.
OUTGND3	24	O	Ground for SBRC-CH3 MOSFETs drivers. It is connected to the current limiting comparator's negative input.
PGOUT	16	O	Powergood open drain output. PG comparators monitor all SBRC's and LDO's over voltage and under voltage. The threshold is ±7%. When one of the output is beyond this condition, powergood output goes low.
PG_DELAY	17	I/O	Programmable delay for Powergood. Connect an external capacitor between this pin and GND to specify time delay.
PWM_SEL	6	I	PWM or auto PWM/SKIP mode select. H : auto PWM/SKIP L : PWM fixed
REF	9	O	0.85-V reference voltage output. This 0.85-V reference voltage is used to set the output voltage and the reference for the over and undervoltage protections. This reference voltage is dropped down from the internal 5-V regulator.
REG5V_IN	30	I	External 5-V input
SS_STBY1	2	I/O	Soft start control and stand by control for SBRC-CH1. Connect an external capacitor between this pin and GND to specify soft start time.
SS_STBY2	5	I/O	Soft start control and stand by control for SBRC-CH2. Connect an external capacitor between this pin and GND to specify soft start time.
SS_STBY3	13	I/O	Soft start control and stand by control for SBRC-CH3. Connect an external capacitor between this pin and GND to specify soft start time.
STBY_LDO	12	I	Standby control input for LDO regulator. LDO regulator can be switched into standby mode by grounding the STBY_LDO pin.
STBY_VREF3.3	11	I	Standby control for 3.3-V linear regulator.
STBY_VREF5	10	I	Standby control for 5-V linear regulator.
TRIP1	41	I	External resistor connection for SBRC-CH1 output current protection control.
TRIP2	39	I	External resistor connection for SBRC-CH2 output current protection control.
TRIP3	18	I	External resistor connection for SBRC-CH3 output current protection control.
VIN	33	I	Supply voltage input
VIN_SENSE12	40	I	SBRC-CH1/2 supply voltage monitor for reference of current limit. Input range is 4.5 V to 28 V.
VIN_SENSE3	19	I	SBRC-CH 3 supply voltage monitor for reference of current limit. Input range is 4.5 V to 28 V.
VREF3.3	32	O	3.3-V linear regulator output
VREF5	31	O	5-V linear regulator output.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

PWM OPERATION

The SBRC block has a high-speed error amplifier to regulate the output voltage of the synchronous buck converter. The output voltage of the SBRC is fed back to the inverting input (INVx (x=1,2,3)) of the error amplifier. The noninverting input is internally connected to a 0.85-V precise band gap reference circuit. The unity gain bandwidth of the amplifier is 2.5 MHz. This decreases the amplifier delay during fast load transients and contributes to a fast response. Loop gain and phase compensation is programmable by an external C, R network between the FBx and INVx pins. The output signal of the error amplifier is compared with a triangular wave to achieve the PWM control signal. The oscillation frequency of this triangular wave sets the switching frequency of the SBRC and is determined by the capacitor connected between the CT and GND pins. The PWM mode is used for the entire load range if the PWM_SEL pin is set LOW, or used in high output current condition if auto PWM/SKIP mode is selected by setting the same pin to HIGH.

SKIP MODE OPERATION

The PWM_SEL pin selects either the auto PWM/SKIP mode or fixed PWM mode. If this pin is lower than 0.3-V, the SBRC operates in the fixed PWM mode. If 2.5 V (min.) or higher is applied, it operates in auto PWM/SKIP mode. In the auto PWM/SKIP mode, the operation changes from constant frequency PWM mode to an energy-saving SKIP mode automatically in accordance with load conditions. Using a MOSFET with ultra-low $r_{DS(on)}$ when the auto SKIP function is implemented is not recommended. The SBRC block has a hysteretic comparator to regulate the output voltage of the synchronous buck converter during SKIP mode. The delay from the comparator input to the driver output is typically 1.2 µs. In the SKIP mode, the frequency varies with load current and input voltage.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current and low $r_{DS(on)}$ N-channel MOSFET(s). The current rating of the driver is 1.2 A at source and sink. When configured as a floating driver, a 5-V bias voltage is delivered from VREF5 pin. The instantaneous drive current is supplied by the flying capacitor between the LHx and LLx pins since a 5-V power supply does not usually have low impedance. It is recommended to add a 5 Ω to 10 Ω resistor between the gate of the high-side MOSFET(s) and the OUTx_u pin to suppress noise. The maximum voltage that can be applied between the LHx and OUTGNDx pins is 33 V.

When selecting the high current rating MOSFET(s), it is important to pay attention to both gate drive power dissipation and the rise/fall time against the dead-time between high-side and low-side drivers. The gate drive power is dissipated from the controller IC and it is proportional to the gate charge at V_{GS} = 5 V, PWM switching frequency, and the numbers of all MOSFETs used for low-side and high-side switches. This gate drive loss should not exceed the maximum power dissipation of the device.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current and low $r_{DS(on)}$ N-channel MOSFET(s). The maximum drive voltage is 5 V from the internal regulator or REG5V_IN pin. The current rating of the driver is typically 1.5 A at source and sink. Gate resistance is not necessary for the low-side MOSFET for switching noise suppression since it turns on after the parallel diode is turned on (ZVS). It needs the same dissipation consideration when using high current rating MOSFET(s). Another issue that needs precaution is the gate threshold voltage. Even though the OUTx_d pin is shorted to the OUTGNDx pin with low resistance when the low-side MOSFET(s) is OFF, high dv/dt of the LLx pin during turnon of the high-side arm will generate a voltage peak at the OUTx_d pin through the drain to gate capacitance, C_{dg}, of the low-side MOSFET(s). To prevent a short period shoot-through during this switching event, the application designer should select MOSFET(s) with adequate threshold voltage.

DEAD-TIME

The internally defined dead-time prevents shoot-through-current flowing through the main power MOSFETs during switching transitions. Typical value of the dead-time is 100 ns.

STANDBY

The SBRC controller, the LDO controller, and the internal regulators can be switched into standby mode separately as shown in Table 1. The standby mode current, when both controllers and regulators are off, can be as low as 1 nA.

Table 1. Standby Logic

INPUT					FUNCTION			
STBY_VREF5	SS_STBYx	STBY_VREF3.3	STBY_LDO	$V_{(REG5V\_IN)} > 4.5V$	VREF5	VREF3.3	SBRCx	LDO
L	L	L	L	False	OFF	OFF	OFF	OFF
L(1)	L(1)	L(1)	L(1)	True(1)	ON(1)	OFF(1)	OFF(1)	OFF(1)
H	L	L	L	x	ON	OFF	OFF	OFF
L	H	L	L	x	OFF	OFF	OFF	OFF
H	H	L	L	x	ON	OFF	ON	OFF
L	L	H	L	x	ON	ON	OFF	OFF
H	L	H	L	x	ON	ON	OFF	OFF
L	H	H	L	x	ON	ON	OFF	OFF
H	H	H	L	x	ON	ON	ON	OFF
L	L	L	H	x	ON	OFF	OFF	ON
H	L	L	H	x	ON	OFF	OFF	ON
L	H	L	H	x	ON	OFF	OFF	ON
H	H	L	H	x	ON	OFF	ON	ON
L	L	H	H	x	ON	ON	OFF	ON
H	L	H	H	x	ON	ON	OFF	ON
L	H	H	H	x	ON	ON	OFF	ON
H	H	H	H	x	ON	ON	ON	ON

(1) This functional mode is not recommended.
x = true or false

SOFT START

Soft start ramp up of the SBRC is controlled by the SS_STBYx pin voltage, which is controlled by an internal current source and an external capacitor connected between the SS_STBYx and GND pins. When the STBY_VREF5 and/or SS_STBYx pin voltages are forced to LOW, the SBRCx is disabled. When the STBY_VREF5 pin voltage is set to HIGH and the SS_STBYx pin floats, the internal current source starts to charge the external capacitor. The output voltage ramps up as the SS_STBYx pin voltage increases from 0 V to 0.85 V. The soft start time is easily calculated from the supply current and the capacitance value (see application information). The soft start timing circuit for the LDO is integrated into the device. The soft start time is fixed and can be as short as 600 µs. This is observed when the LDO is turned on separately from the SBRC. Simultaneous start-up of one of the SBRC and the LDO, is also possible. Tie the LDO input to the SBRCx's output, let both the STBY_VREF5 and STBY_LDO voltages rise to the HIGH level, and invoke Soft start on the SS_STBYx pin; then the LDO's output follows the ramp of the SBRCx's output.

OVER CURRENT PROTECTION

Over current protection (OCP) is achieved by comparing the drain-to-source voltage of the high-side and low-side MOSFET to a set-point voltage, which is defined by both the internal current source, $I_{(TRIP)}$, and the external resistor connected between the VIN_SENSEx and the TRIPx pins. $I_{(TRIP)}$ has a typical value of 13 µA at 25°C. When the drain-to-source voltage exceeds the set-point voltage during low-side conduction, the high-side current comparator becomes active, and the low-side pulse is extended until this voltage comes back below the threshold. If the set-point voltage is exceeded during high-side conduction in the following cycle, the current limit circuit terminates the high-side driver pulse. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated to latch both the high-side and low-side drivers OFF. In the TPS5130, trip current $I_{(TRIP)}$ has a temperature coefficient of 3400 ppm/°C in order to compensate for temperature drift of the MOSFET on-resistance.

OCP FOR THE LDO

To achieve the LDO current limit, a sense resistor must be placed in series with the N-channel MOSFET drain, connected between the LDO_IN and LDO_CUR pins (see reference schematic). If the voltage drop across this sense resistor exceeds 50 mV, the output voltage is reduced to approximately 22% of the nominal value, thus it activates the UVP to start the FLT latch timer. When the time is up, the LDO_GATE pin is pulled LOW to makes the LDO regulator shut down. Note that all of the SBRCs are latched OFF at the same time since the LDO and the SBRCs share the same FLT capacitor.

OVER VOLTAGE PROTECTION

For overvoltage protection (OVP), the TPS5130 monitors the INVx and INV_LDO pin voltages. When the INVx or INV_LDO pin voltage is higher than 0.95 V (0.85 V +12%), the OVP comparator output goes low and the FLT timer starts to charge an external capacitor connected to FLT pin. After a set time, the FLT circuit latches the high-side MOSFET driver, the low-side MOSFET drivers, and the LDO. The latched state of each block is summarized in Table 2. The timer source current for the OVP latch is 125 µA(typ.), and the time-up voltage is 1.185 V (typ.). The OVP timer is designed to be 50 times faster than the under voltage protection timer described in Table 2.

Table 2. OVP Logic

OVP OCCURRED AT	HIGH-SIDE MOSFET DRIVER	LOW-SIDE MOSFET DRIVER	LDO
SBRC	OFF	ON	OFF
LDO	OFF	OFF	OFF

UNDER VOLTAGE PROTECTION

For under voltage protection (UVP), the TPS5130 monitors the INVx and INV_LDO pin voltages. When the INVx or INV_LDO pin voltage is lower than 0.55 V (0.85 V - 35 %), the UVP comparator output goes low, and the FLT timer starts to charge the external capacitor connected to FLT pin. Also, when the current comparator triggers the OCP, the UVP comparator detects the under voltage output and starts the FLT capacitor charge, too. After a set time, the FLT circuit latches all of the MOSFET drivers to the OFF state. The timer latch source current for UVP is 2.3 µA (typ.), and the time-up voltage is also 1.185 V (typ.). The UVP function of the LDO controller is disabled when voltage across the pass transistor is less than 0.23 V (typ.).

FLT

When an OVP or UVP comparator output goes low, the FLT circuit starts to charge the FLT capacitor. If the FLT pin voltage goes beyond a constant level, the TPS5130 latches the MOSFET drivers. At this time, the state of MOSFET is different depending on the OVP alert and the UVP alert (see Table 2). The enable time used to latch the MOSFET drivers is decided by the value of the FLT capacitor. The charging constant current value depends on whether it is an OVP alert or a UVP alert as shown in the following equation:

FLT source current (OVP) = FLT source current (UVP) $\times$ 50

UNDER VOLTAGE LOCK OUT (UVLO)

When the output voltage of the internal 5-V regulator or the REG5V_IN voltage decreases below about 4 V, the output stages of all the SBRCs and the LDO are turned off. This state is not latched, and the operation recovers immediately after the input voltage becomes higher than the turnon value again. The typical hysteresis voltage is 100 mV.

UVLO FOR LDO

The LDO_IN voltage is monitored with a hysteretic comparator. When this voltage is less than 1 V, the UVLO circuit disables the UVP/OVP comparators that monitor the INV_LDO voltage. In case the SBRC overcurrent protection is activated prior to that of the LDO's, this protection function may also be observed.

LDO CONTROL

The LDO controller can drive an external N-channel MOSFET. This realizes a fast response as well as an ultralow dropout voltage regulator. For example, it is easy to configure both a 1.8-V and a 1.5-V high current power supply for core and I/O of modern digital processors, one from the SBRC and the other from the LDO. The LDO_IN voltage range is from 1.1 V to 3.6 V, and the output voltage is adjustable from 0.9 V to 2.5 V by an external resistor divider. Gain and phase of the high-speed error amplifier for this LDO control is internally compensated and is connected to the 0.85-V band gap reference circuit. The gate driver buffer is supplied by VIN_SENSE voltage. In the relatively high output voltage applications, make sure that output voltage plus threshold voltage of the pass transistor is less than the minimum VIN. More precisely,

$VIN - 0.7 \geq V_{thn} + V_{(LDO\_OUT)}$

where V_{thn} is the threshold voltage of the Nch MOSFET.

The LDO controller is also equipped with OVP, UVP, overcurrent limit, and overshoot protection functions.

OVERSHOOT PROTECTION

In the event that load current changes from high to low very quickly, the LDO regulator output voltage may start to overshoot. In order to resist this phenomenon, the LDO controller has an overshoot protection function. If the LDO regulator output overshoots, the controller draws electrical charge out from the LDO_OUT pin to hold it stable.

POWERGOOD

A single powergood circuit monitors the SBRCx output voltages and the LDO output voltage. The powergood pin is an open drain output. When the INV or INV_LDO voltage goes beyond ±7% of 0.85 V, the powergood pin is pulled down to the LOW level. Powergood propagation delay is programmable by controlling rising time using an external capacitor connected to the PG_DELAY pin. During the soft start period, powergood indicates LOW, in other words *power bad*.

Table 3. Powergood Logic

SS_STBY1	SS_STBY2	SS_STBY3	STBY_LDO	POWERGOOD
L	L	L	L	L
H	L	L	L	H
L	H	L	L	H
H	H	L	L	H
L	L	H	L	H
H	L	H	L	H
L	H	H	L	H
H	H	H	L	H
H or L	H or L	H or L	H	H

5-V REGULATOR

An internal linear voltage regulator is used for the high-side driver bootstrap. Since the input voltage ranges from 4.5 V to 28 V, this feature offers a fixed bootstrap voltage to simplify the drive design. It is active if the STBY_VREF5 is HIGH and has a tolerance of 4%. The 5-V regulator is used for powering the low-side driver and the VREF. When this regulator is disconnected from the MOSFET drivers, it is used only for the source of VREF.

3.3-V REGULATOR

The TPS5130 has a 3.3-V linear regulator. The output is made from the internal 5-V regulator or an external 5 V from the REG5V_IN pin. The maximum output current of this regulator is limited to 30 mA by an output current limit control. A ceramic capacitor of 4.7 µF should be connected between the VREF3.3 and GND pins to stabilize the output voltage.

EXTERNAL 5-V INPUT AND 5-V SWITCH

If the internal 5-V switch detects 5-V input from the REG5V_IN pin, the internal 5-V regulator is disconnected from the MOSFET drivers. The external 5 V is used for both the high-side bootstrap and the low-side driver, thus increasing the efficiency. When an excess voltage is applied to the REG5V_IN pin, the OVP timer starts to charge the FLT capacitor and latches all the MOSFET drivers and the LDO at OFF state after a set time.

PHASE INVERTER

The SBRC3 of the TPS5130 operates in the same phase as the internal triangular oscillator output while the SBRC1 and the SBRC2 operate 180 degrees out of phase. When the SBRC1 and the SBRC3 (or the SBRC2 and the SBRC3) share the same input power supply, the TPS5130 realizes 180 degrees out of phase operation that reduces input current ripple and enables the input capacitor value smaller.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs JUNCTION TEMPERATURE

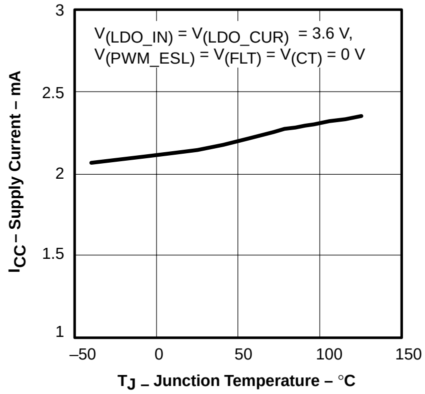


Figure 1

SUPPLY CURRENT (SHUTDOWN) vs JUNCTION TEMPERATURE

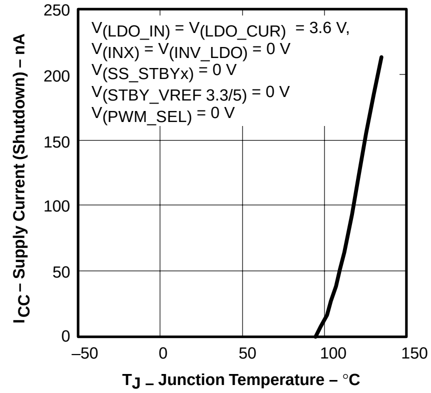


Figure 2

SOURCE CURRENT FLT(OVP) vs JUNCTION TEMPERATURE

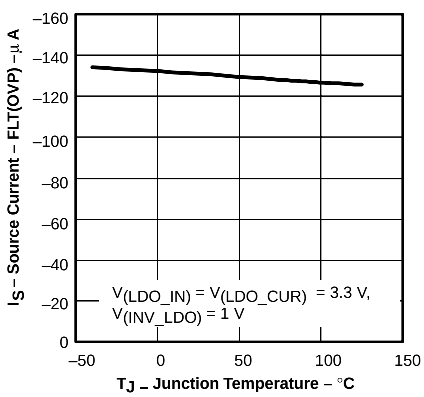


Figure 3

SOURCE CURRENT FLT(UVP) vs JUNCTION TEMPERATURE

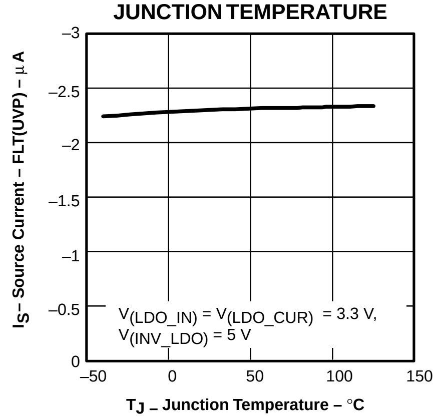


Figure 4

TRIP CURRENT vs JUNCTION TEMPERATURE

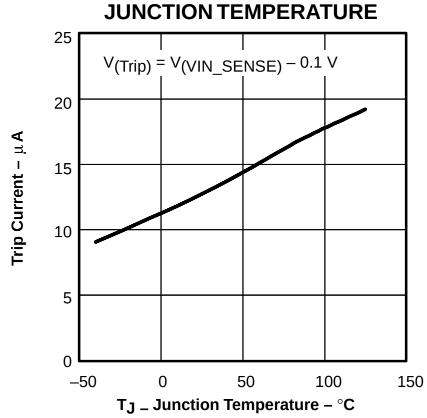


Figure 5

SINK CURRENT (LDO_GATE) vs OUTPUT VOLTAGE

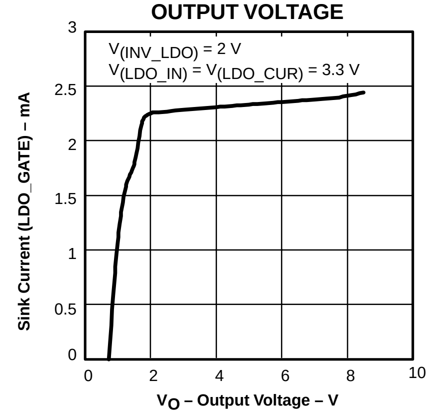


Figure 6

$V_{(VIN\_SENSE)} = 12$ V, unless otherwise noted

TYPICAL CHARACTERISTICS

SOURCE CURRENT (LDO_GATE)
vs
OUTPUT VOLTAGE

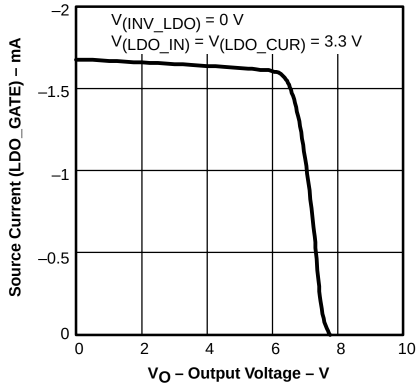


Figure 7

THRESHOLD VOLTAGE (OVP)
vs
JUNCTION TEMPERATURE

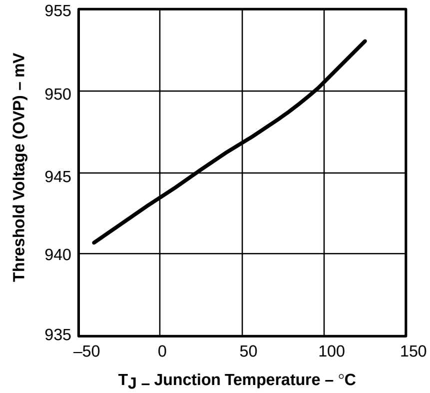


Figure 8

OSCILLATOR FREQUENCY
vs
CAPACITANCE

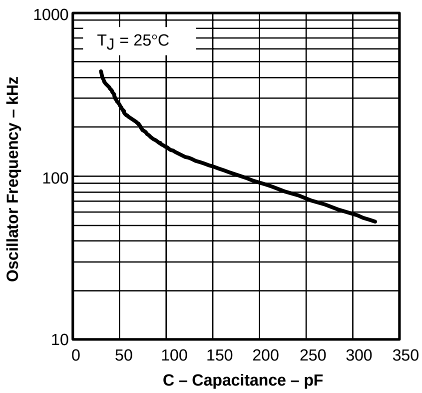


Figure 9

OUTPUT MAXIMUM DUTY CYCLE
vs
JUNCTION TEMPERATURE

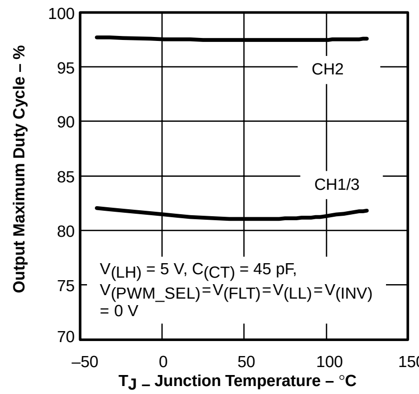


Figure 10

DELAY TIME FLT(OVP)
vs
CAPACITANCE

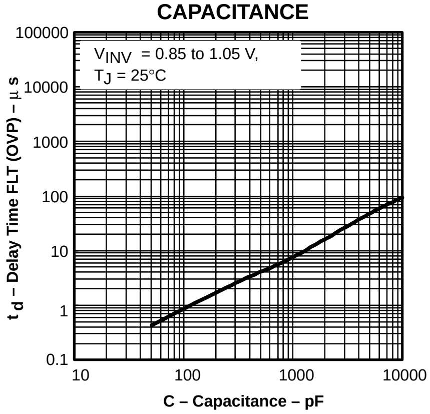


Figure 11

DELAY TIME FLT(UVP)
vs
CAPACITANCE

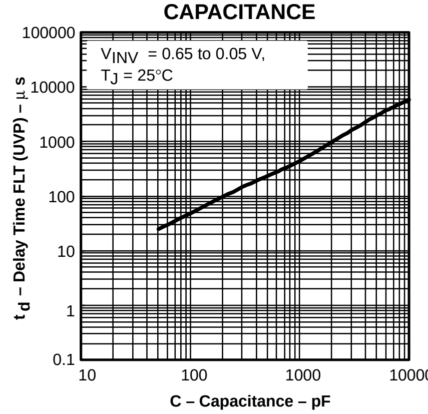


Figure 12

V_{VIN_SENSE} = 12 V, unless otherwise noted

TYPICAL CHARACTERISTICS

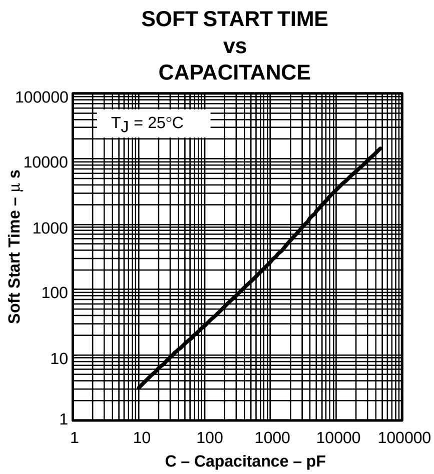


Figure 13

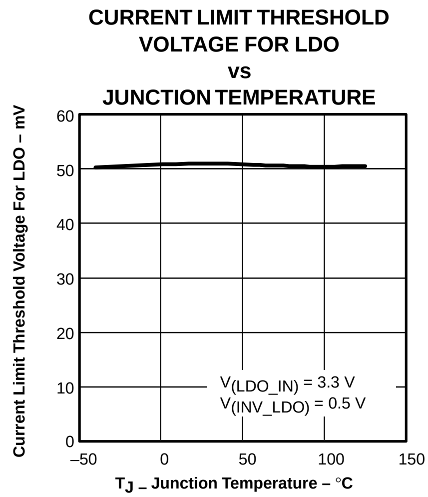


Figure 14

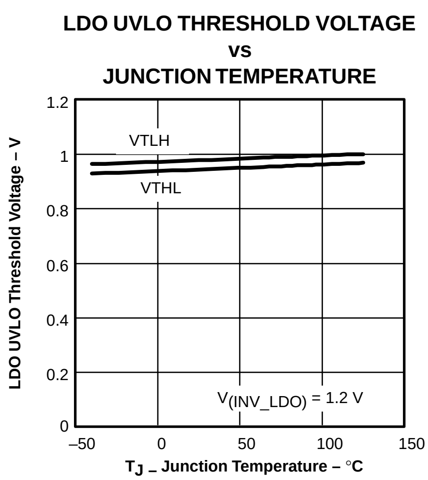


Figure 15

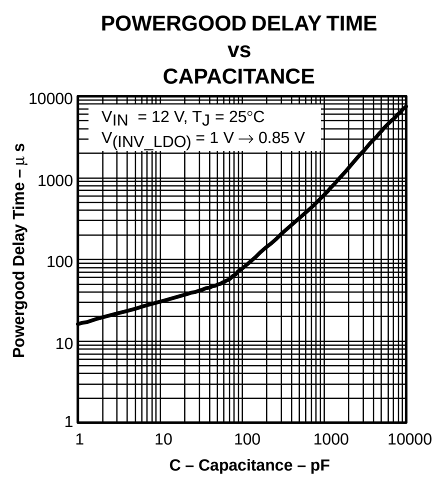


Figure 16

V_{VIN_SENSE} = 12 V, unless otherwise noted

APPLICATION INFORMATION

The design shown is a reference design for a notebook PC application. An evaluation module (EVM) is available for customer testing and evaluation.

The following key design procedures aid in the design of the notebook PC power supply using TPS5130.

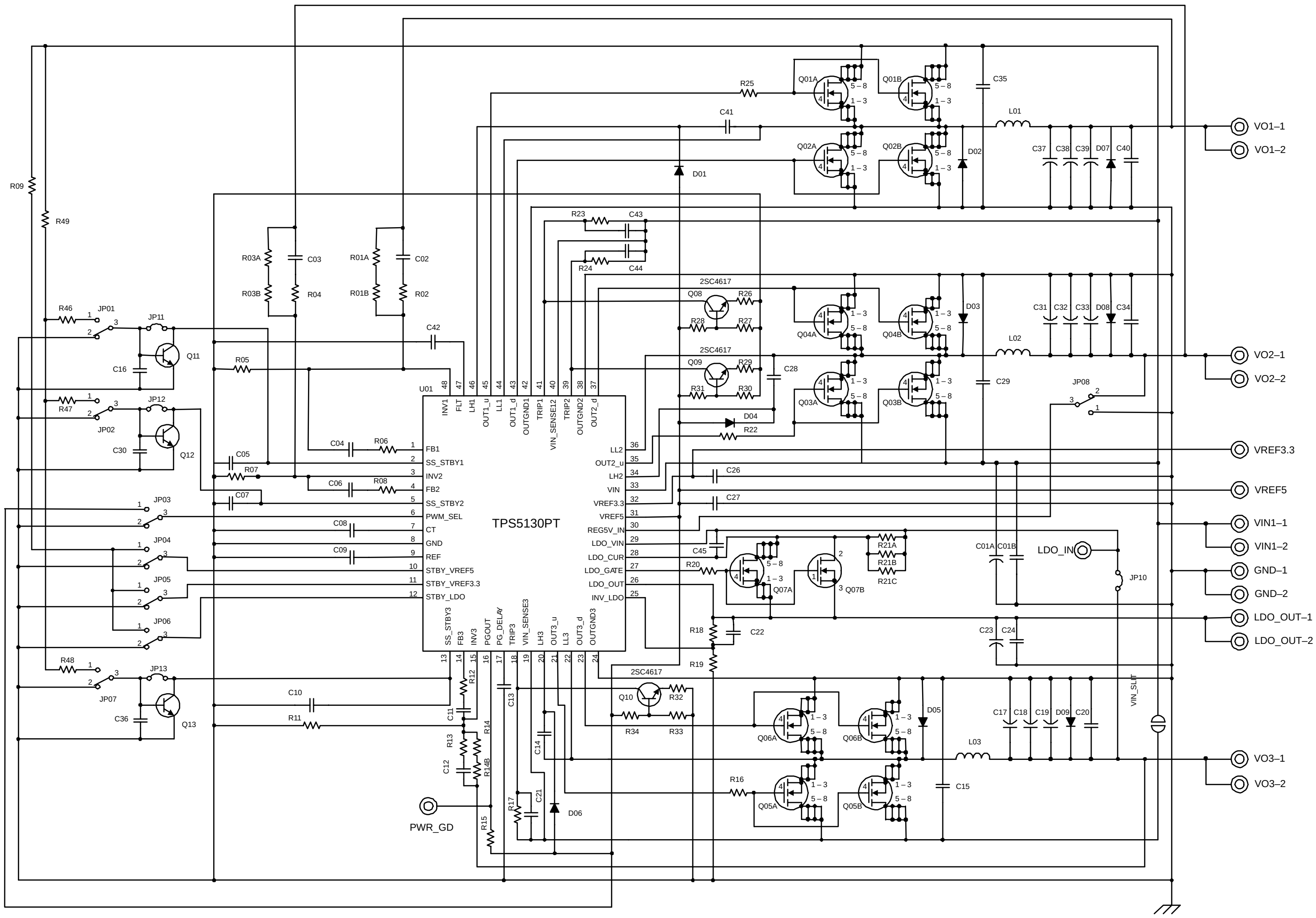


Figure 17. EVM Schematic

An optional circuit composed of Q08, Q09, Q10, R26, R27, R28, R29, R30, R31, R32, R33, and R34 can be used to increase temperature coefficient of the trip current.

OUTPUT VOLTAGE SETPOINT CALCULATION

In the following calculation, assume the output voltage of SBRC1 (V_O1), SBRC2 (V_O2), SBRC3 (V_O3), and LDO (V_O4) are 3.3 V, 5 V, 1.8 V, and 1.5 V respectively. The reference voltage and the voltage divider set the output voltage. In the TPS5130, the reference voltage is 0.85 V, and the divider is composed of three resistors in the EVM design that are R01A, R01B, and R05 for the first SBRC output; R03A, R03B, and R07 for the second SBRC output ; R14A, R14B, and R11 for the third SBRC output ; R18 and R19 for LDO regulator output.

$$V_O = \frac{R1 \times V_{ref}}{R2} + V_{ref} \text{ or } R2 = \frac{R1 \times V_{ref}}{V_O - V_{ref}}$$

where R1 is the top resistor (kΩ) (R01A + R01B or R03A + R03B or R14A + R14B or R18); R2 is the bottom resistor (kΩ) (R05 or R07 or R11 or R19); V_O is the required output voltage (V); V_{ref} is the reference voltage (0.85 V in TPS5130). The value for R1 is set as a part of the compensation circuit and the value of R2 may be calculated to achieve the desired output voltage. In the EVM design, the value of R1 is determined as R01A = 27 kΩ and R01B = 1.8 kΩ for V_O1, R03A = 47 kΩ and R03B = 1.8 kΩ for V_O2, R14A = 10 kΩ and R14B = 1.2 kΩ for V_O3, and R18 = 6.8 k + 820 Ω for V_O4 considering stability. For V_O1:

$$R05 = \frac{(27\text{ k} + 1.8\text{ k}) \times 0.85}{3.3 - 0.85} = 9.99\text{ k}\Omega$$

Therefore, use 10 kΩ.

In a same manner, R07 = R11 = R19 = 10 kΩ as follows.

$$R07 = \frac{(47\text{ k} + 1.8\text{ k}) \times 0.85}{5 - 0.85} = 10.00\text{ k}\Omega$$

$$R11 = \frac{(10\text{ k} + 1.2\text{ k}) \times 0.85}{1.8 - 0.85} = 10.02\text{ k}\Omega$$

$$R19 = \frac{(6.8\text{ k} + 820) \times 0.85}{1.5 - 0.85} = 9.96\text{ k}\Omega$$

The values of R01B, R03B, R14B and R19 are chosen so that the calculated values of R05, R07, R11, and R19 are standard value resistors and the V_O setpoint maintains the highest precision. This is best accomplished by combining two resistor values. If a standard value resistor can not be applied, use a value for R01A, R03A, R14A, and R18 that is just slightly less than the desired total. A small resistor value in the range of tens or hundreds of ohms for R01B, R03B, R14B and R18 can then be added to generate the desired final value.

OUTPUT INDUCTOR SELECTION

The required value for the output filter inductor can be calculated by using the equation below, assuming the magnitude of the ripple current is 20 % of the maximum output current:

$$L_{(out)} = \frac{VIN - V_O}{0.2 \times I_O} \times \frac{V_O}{VIN} \times \frac{1}{f_S}$$

Where $L_{(out)}$ is output filter inductor value (H), VIN is the input voltage (V), I_O is the maximum output current (A), f_S is the switching frequency (Hz).

Example : VIN = 8 V; V_O = 3.3 V; I_O = 4 A; f_S = 300 kHz.

Then, $L_{(out)}$ = 8.1 µH.

If faster output response is required for a sudden transition of the load, smaller inductance value is recommended.

OUTPUT INDUCTOR RIPPLE CURRENT

The output inductor current can affect not only the efficiency, but also the output voltage ripple. The equation is exhibited below:

$$I_{(ripple)} = \frac{VIN - V_O - I_O \times \left(r_{DS(on)} + R_L\right)}{L_{(out)}} \times \frac{V_O}{VIN} \times \frac{1}{f_S}$$

where $I_{(ripple)}$ is the peak-to-peak ripple current (A) through the inductor; Io is the output current; $r_{DS(on)}$ is the on-time resistance of MOSFET (Ω); R_L is the inductor dc resistance (Ω). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example: VIN = 8 V; V_O = 3.3 V; I_O = 4 A; rDS(on) = 25 mΩ; R_L = 10 mΩ; f_S = 300 kHz; $L_{(out)}$ = 4 µH.

Then, the ripple current $I_{(ripple)}$ = 1.57 A

OUTPUT CAPACITOR SELECTION

Selection of the output capacitor is basically dependent on the amount of peak-to-peak ripple voltage allowed on the output and the ability of the capacitor to dissipate the RMS ripple current. Assuming that the ESR of the output filter sees the entire inductor ripple current then:

$$V_{pp} = I_{(ripple)} \times R_{(esr)}$$

And a suitable capacitor must be chosen so that the peak-to-peak output ripple is within the limits allowable for the application.

OUTPUT CAPACITOR RMS CURRENT

Assuming the inductor ripple current totally goes through the output capacitor to ground, the RMS current in the output capacitor can be calculated as:

$$I_O(rms) = \frac{I_{(ripple)}}{\sqrt{12}}$$

where I_O(rms) is maximum RMS current in the output capacitor (A); $I_{(ripple)}$ is the peak-to-peak inductor ripple current (A).

Example: $I_{(ripple)}$ = 1.57 A, then, I_O(rms) = 0.45 A

INPUT CAPACITOR RMS CURRENT

Since the SBRC3 of the TPS5130 operates 180 degree off phase against the SBRC1 and SBRC2, total RMS current in the input capacitor is calculated as follows, assuming the input current totally goes into the input capacitor to the power ground, and ignoring ripple current in the inductor.

When the duty cycle of the SBRC2 (D2) is over 50 %,

$$I_I(rms) = \sqrt{(D1 \times I_O1^2) + (D2 \times I_O2^2) + (D3 \times I_O3^2) + (2D1 \times I_O1 \times I_O2) + (2D2 - 1) \times I_O2 \times I_O3 - I_Ox^2}$$

$$I_Ox = (D1 \times I_O1) + (D2 \times I_O2) + (D3 \times I_O3) \qquad D2 \geq 0.5 \geq D1 \geq D3$$

I_I(rms) is the input RMS current in the input capacitor; DX is duty cycles, defined as V_O/V_I in this case, of the SBRCx.

When D2 is less than 50%,

$$I_I(rms) = \sqrt{(D1 \times I_O1^2) + (D2 \times I_O2^2) + (D3 \times I_O3^2) + (2D1 \times I_O1 \times I_O2) - I_Ox^2}$$

Example: VIN = 12 V, V_O1 = 3.3 V, V_O2 = 5 V (D2 = 0.42), V_O3 = 1.8V, $I_O1 = I_O2$ = 4 A, I_O3 = 6 A

Then, I_I(rms) = 3.44 A

On the contrary, if three SBRCs operate in a same phase the RMS current is calculated as follows.

$$I_I(rms) = \sqrt{(D1 \times I_O1^2) + (D2 \times I_O2^2) + (D3 \times I_O3^2) + (2D1 \times I_O1 \times I_O2) + (2D3 \times I_O3) \times \left(I_O1 + I_O2\right) - I_Ox^2}$$

Under the same operation condition, I_I(rms) = 5.13 A

Therefore, 180 degree out of phase operation is effective in reducing input RMS current, and it allows a smaller input capacitance value. The input capacitors must be chosen so that together they can safely handle the input ripple current. Depending on the input filtering and the dc input voltage source, not all the ripple current flows through the input capacitors, but some may be present on the input leads to the EVM.

SOFT START

The soft start timing can be adjusted by selecting the soft-start capacitor value. The equation is;

$$C(soft) = 2.3 \times 10^{-6} \times \frac{T(soft)}{0.85}$$

where C(soft) is the soft-start capacitor (μF) (C05, C07 and C10 in EVM design):

T(soft) is the start-up time (s).

Example: T(soft) = 5 ms, therefore, C(soft) = 0.0135 μF.

CURRENT PROTECTION

The current limit in TPS5130 is set using an internal current source and an external resistor (R17, R23 and R24). The current limit protection circuit compares the drain to source voltage of the high-side and low-side MOSFET(s) with respect to the set-point voltage. If the voltage up exceeds the limit during high-side conduction, the current limit circuit terminates the high-side driver pulse. If the set point voltage is exceeded during low-side conduction, the low side pulse is extended through the next cycle. Together this action has the effect of decreasing the output voltage until the under voltage protection circuit is activated and the fault latch is set and both the high-side and low-side MOSFET drivers are shut off. The equation below should be used for calculating the external resistor value for current protection set point:

$$R(cl) = \frac{r_{DS(on)} \times \left(I_{(trip)} + \frac{I_{(ripple)}}{2} \right)}{13 \times 10^{-6}}$$

where $R_{(cl)}$ is the external current limit resistor (R17, R23 and R24); $r_{DS(on)}$ is the low-side MOSFET(Q02, Q04 and Q06) on-time resistance. $I_{(trip)}$ is the required current limit.

Example: $r_{DS(on)}$ = 25 mΩ, $I_{(trip)}$ = 4 A, $I_{(ripple)}$ = 1.57 A, therefore, $R_{(cl)}$= 9.2 kΩ.

It should be noted that $r_{DS(on)}$ of a FET is highly dependent on temperature, so to insure full output at maximum operating temperature, the value of $r_{DS(on)}$ in the above equation should be adjusted. For maximum stability, it is recommended that the high-side MOSFET(s) has the same, or slightly higher $r_{DS(on)}$than the low-side MOSFET(s). If the low-side MOSFET(s) has a higher $r_{DS(on)}$, in certain low duty cycle applications it may be possible for the device to regulate at an output current higher than that set by the above equation by increasing the high-side conduction time to compensate for the missed conduction cycle caused by the extension of the previous low-side pulse.

TIMER-LATCH

The TPS5130 includes fault latch function with a user adjustable timer to latch the MOSFET drivers in case of a fault condition. When either the OVP or UVP comparator detect a fault condition, the timer starts to charge FLT capacitor (C42), which is connected with FLT pin. The circuit is designed so that for any value of FLT capacitor, the undervoltage latch time $t_{(uvplatch)}$ is about 50 times larger than the overvoltage latch time $t_{(ovplatch)}$. The equations needed to calculate the required value of the FLT capacitor for the desired over and undervoltage latch delay times are:

$$C_{(lat)} = 2.3 \times 10^{-6} \times \frac{t_{(uvplatch)}}{1.185} \quad \text{and}$$

$$C_{(lat)} = 125 \times 10^{-6} \times \frac{t_{(ovplatch)}}{1.185}$$

where $C_{(lat)}$ is the external capacitor, $t_{(uvplatch)}$ is the time from UVP detection to latch. $t_{(ovplatch)}$ is the time from OVP detection to latch.

For the EVM, $t_{(uvplatch)}$ = 5 ms and $t_{(ovplatch)}$ = 0.1 ms, so $C_{(lat)}$ = 0.01 μF. If the voltage on the FLT pin reaches 1.185 V, the fault latch is set, and the MOSFET drivers are set as follows:

Undervoltage Protection

The undervoltage comparator circuit continually monitors the voltage at the INV and INV_LDO pins. If the voltage at either pin falls below 65 % of the 0.85 V reference, the timer begins to charge the FLT capacitor. if the fault condition persists beyond the time $t_{(uvplatch)}$, the fault latch is set and both the high-side and low-side drivers, and LDO regulator drivers are forced OFF.

Short-Circuit Protection

The short-circuit protection circuitry uses the UVP circuit to latch the MOSFET drivers. When the current limit circuit limits the output current, then the output voltage goes below the target output voltage and UVP comparator detects a fault condition as described above.

Overvoltage Protection

The overvoltage comparator circuit continually monitors the voltage at the INV and INV_LDO pins. If the voltage at either pin rises above 112 % of the 0.85 V reference, the timer begins to charge the FLT capacitor. If the fault condition persists beyond the time $t^{(ovplatch)}$, the fault latch is set and the high-side drivers are forced OFF, while the low-side drivers are forced ON, and LDO regulator drivers are forced OFF.

CAUTION:

Do not set the FLT terminal to a lower voltage (or GND) while the device is timing out an OVP or UVP event. If the FLT terminal is manually set to a lower voltage during this time, output overshoot may occur. The TPS5130 must be reset by grounding SS_STBYx and STBY_LDO, or dropping down REG5V_IN.

Disablement of the Protection Function

If it is necessary to inhibit the protection functions of the TPS5130 for troubleshooting or other purposes, the OCP,OVP, and UVP circuits may be disabled.

- OCP(SBRC): Remove the current limit resistors R17, R23 and R24 to disable the current limit function.
- OCP(LDO): Short–circuit R21 to disable the current limit function.
- OVP, UVP: Grounding the FLT terminal can disable OVP and UVP.

LDO REGULATOR APPLICATION INFORMATION

Output Capacitor Selection

To keep stable operation of the LDO, capacitance of more than 33 μF and $R_{(esr)}$ of more than 30 mΩ are recommended for the output capacitor.

Power MOSFET Selection

Also, to keep stable operation of LDO, lower input capacitance is recommended for the external power MOSFET. However, input capacitance that is too small may lead the feedback loop into an unstable region. In this case, the gate resistor of several hundreds ohms keeps the LDO operation in the stable state.

Current Protection

If excess output current flows through sense resistor (R21) and the voltage drop exceeds 50 mV, the output voltage is reduced to approximately 22% of the nominal value, thus activates UVP to start the FLT latch timer.

When the set current is 3 A, the value of R21 is 16.7 mΩ.

Layout Guidelines

Good power supply results only occur when care is given to proper design and layout. Layout affects noise pickup and generation and can cause a good design to perform with less than expected results. With a range of currents from milliamps to tens amps, good power supply layout is much more difficult than most general PCB designs. The general design should proceed from the switching node to the output, then back to the driver section and, finally, parallel the low-level components. Below are specific points to consider before the layout of a TPS5130 design begins.

- A four-layer PCB design is recommended for design using the TPS5130. For the EVM design, the top layer contains the interconnection to the TPS5130, plus some additional signal traces. Layer2 is fully devoted to the ground plane. Layer3 has some signal traces. The bottom layer is almost devoted to ANAGND, and the rest is to other signal trace.
- All sensitive analog components such as INV, REF, CT, GND, FLT, and SS_STBY should be referenced to ANAGND.
- Ideally, all of the area directly under the TPS5130 chip should also be ANAGND.
- ANAGND and DRVGND should be isolated as much as possible, with a single point connection between them.

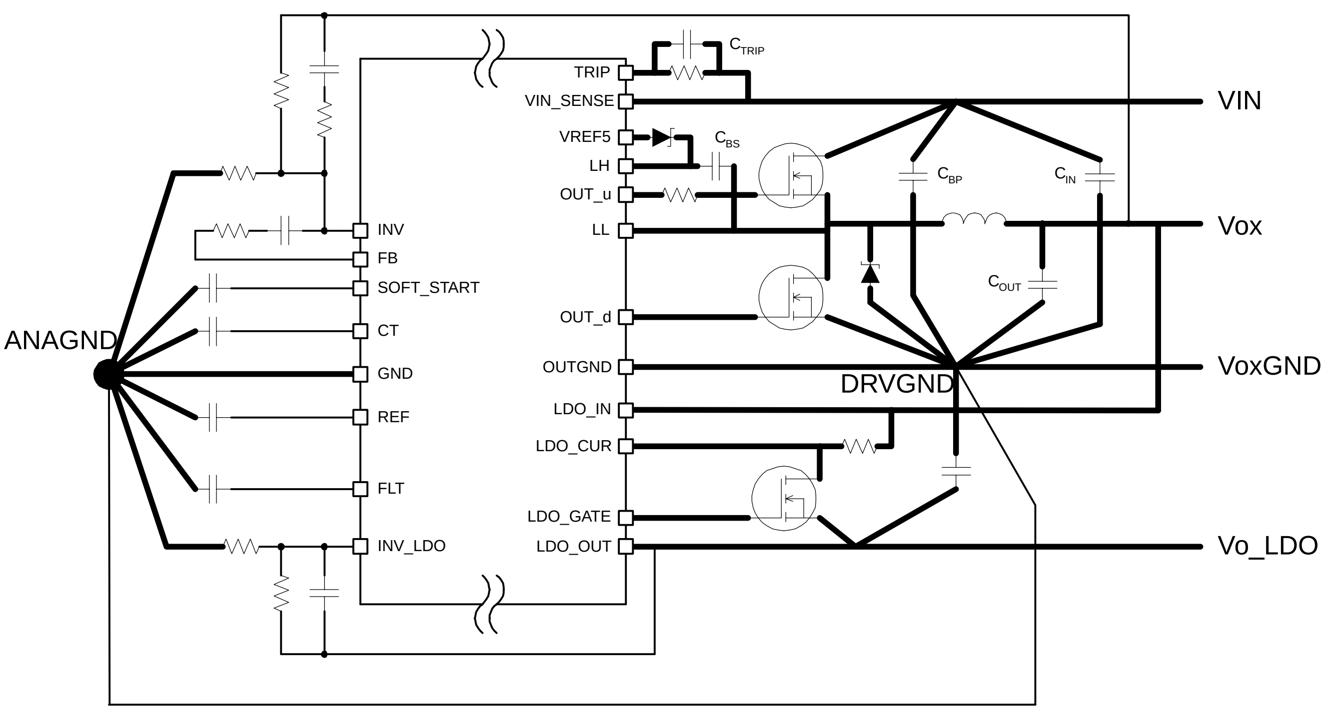


Figure 18. PCB Diagram

Low-Side MOSFET(s)

- The source of low-side MOSFET(s) should be referenced to DRVGND, otherwise ANAGND is subject to the noise of the outputs.
- DRVGND should be connected to the main ground plane close to the source of the low-side MOSFET.
- OUTGND should be placed close to the source of low side MOSFET(s).
- The Schottky diode anode, the returns for the high frequency bypass capacitor for the MOSFETs, and the source of the low-side MOSFET(s) traces should be routed as close together as possible.

Connections

- Connections from the drivers to the gate of the power MOSFETs should be as short and wide as possible to reduce stray inductance. This becomes more critical if external gate resistors are not being used. In addition, as for the current limit noise issue, use of a gate resistor on the high-side MOSFET(s) considerably reduces the noise at the LL node, improving the performance of the current limit function.
- The connection from LL to the power MOSFETs should be as short and wide as possible.

Bypass Capacitor

- The bypass capacitor for VIN_SENSE should be placed close to the TPS5130.
- The bulk storage capacitors across VIN should be placed close to the power MOSFETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side MOSFET(s) and to the source of the low-side MOSFET(s).
- For aligning phase between the drain of high-side MOSFET(s) and the trip-pin, and for noise reduction, a 0.1 μF capacitor $C_{(TRIP)}$ should be placed in parallel with the trip resistor.

Bootstrap Capacitor

- The bootstrap capacitor $C_{(BS)}$ (connected from LH to LL) should be placed close to the TPS5130.
- LH and LL should be routed close to each other to minimize noise coupling to these traces.
- LH and LL should not be routed near the control pin area (ex. INV, FB, REF, etc.).

Output Voltage

- The output voltage sensing trace should be isolated by either ground plane.
- The output voltage sensing trace should not be placed under the inductors on same layer.
- The feedback components should be isolated from output components, such as, MOSFETs, inductors, and output capacitors. Otherwise the feedback signal line is susceptible to output noise.
- The resistors for setup output voltage should be referenced to ANAGND.
- The INV trace should be as short as possible.

EFFICIENCY (PWM MODE) vs OUTPUT CURRENT

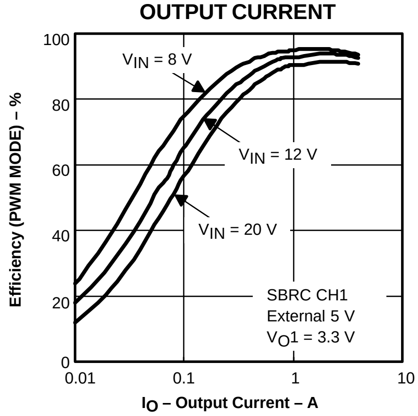


Figure 19

EFFICIENCY (PWM MODE) vs OUTPUT CURRENT

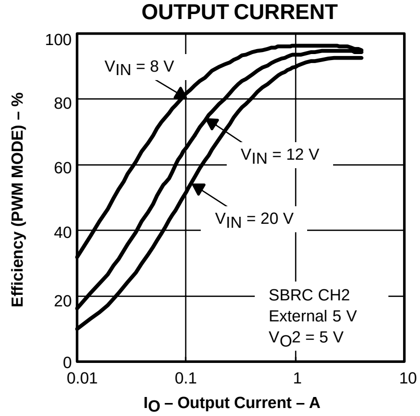


Figure 20

EFFICIENCY (PWM MODE) vs OUTPUT CURRENT

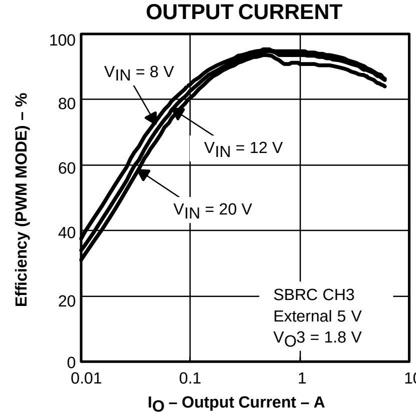


Figure 21

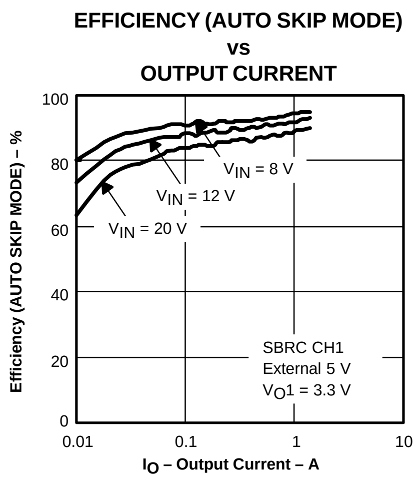


Figure 22

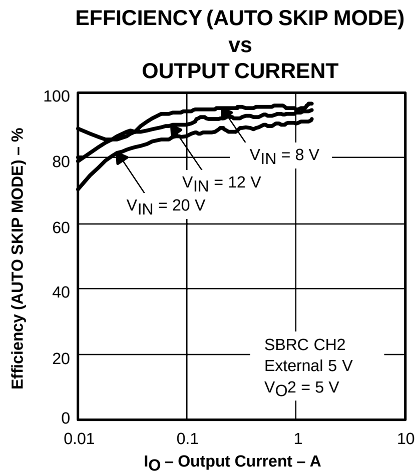


Figure 23

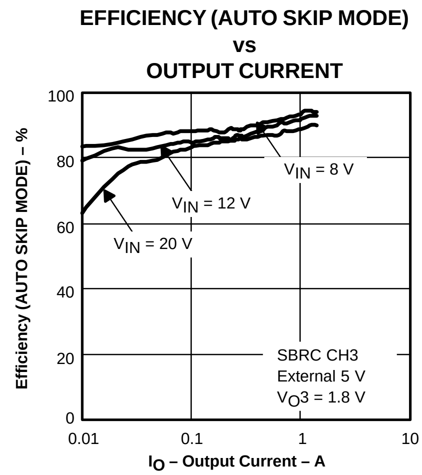


Figure 24

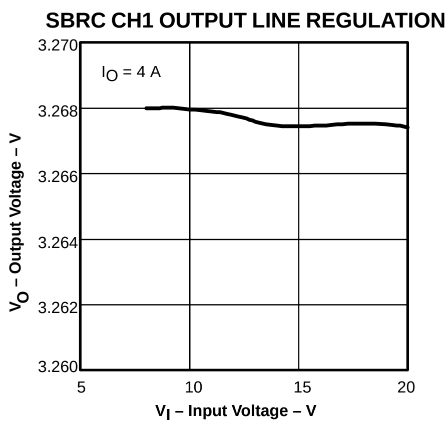


Figure 25

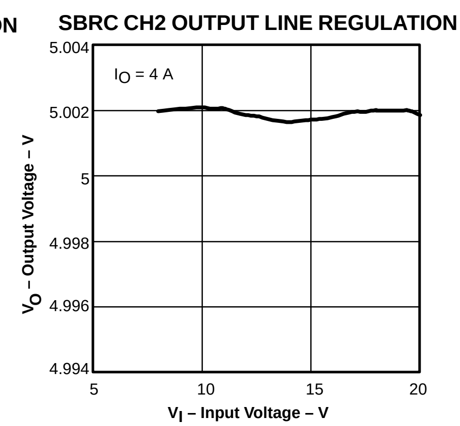


Figure 26

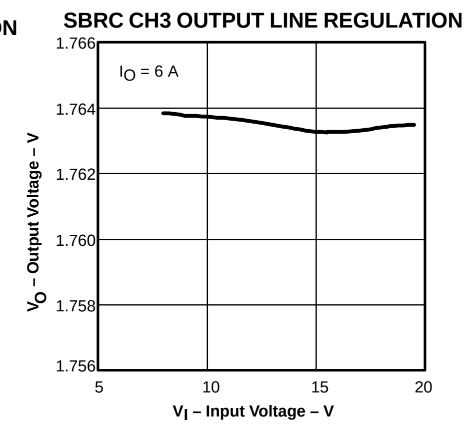


Figure 27

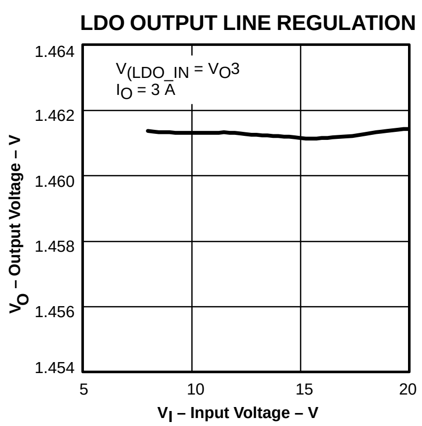


Figure 28

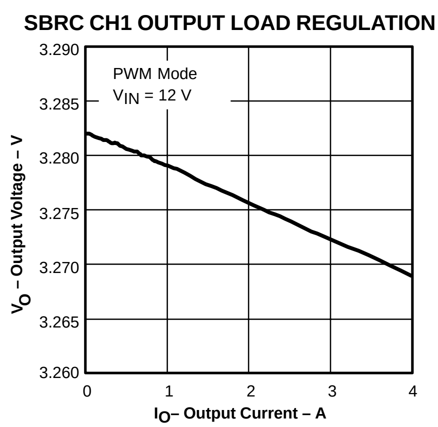


Figure 29

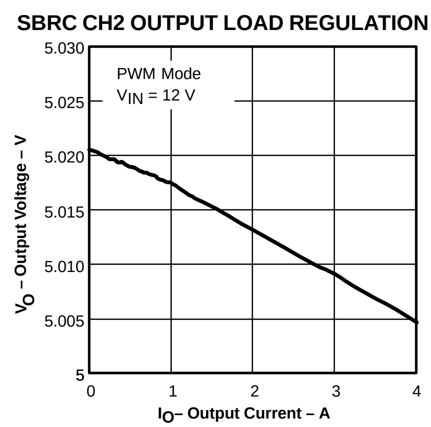


Figure 30

SBRC CH3 OUTPUT LOAD REGULATION

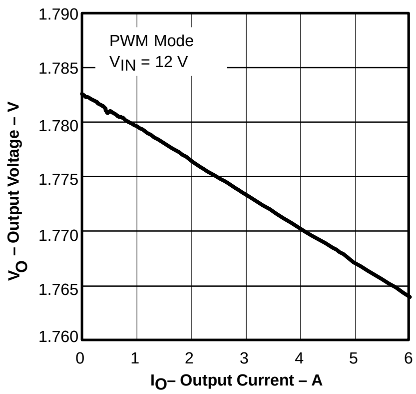


Figure 31

LDO OUTPUT LOAD REGULATION

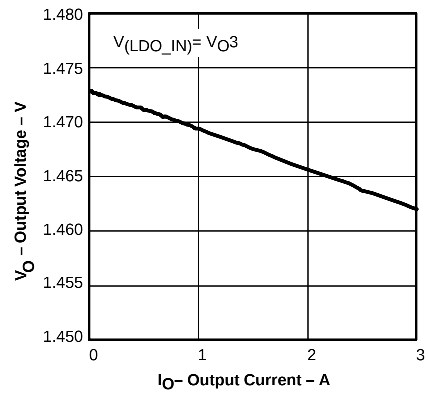


Figure 32

SBRC CH1 OUTPUT VOLTAGE RIPPLE

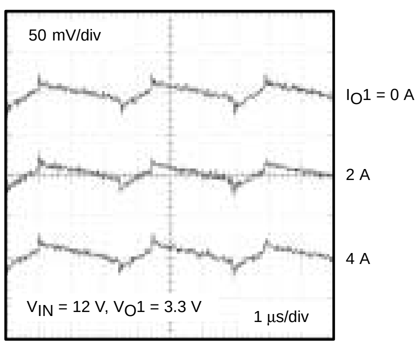


Figure 33

SBRC CH2 OUTPUT VOLTAGE RIPPLE

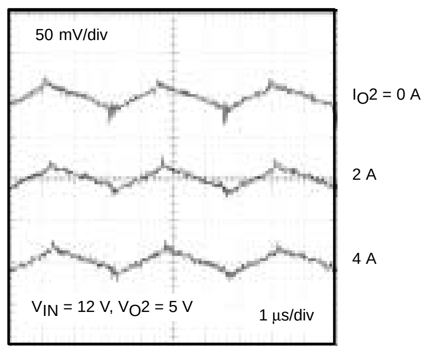


Figure 34

SBRC CH3 OUTPUT VOLTAGE RIPPLE

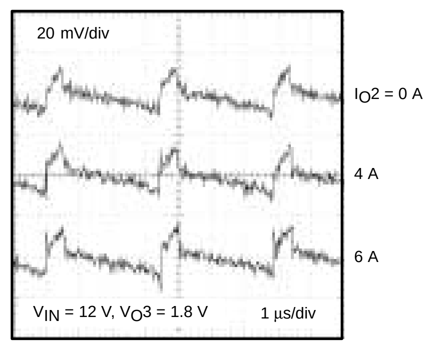


Figure 35

LDO OUTPUT VOLTAGE RIPPLE

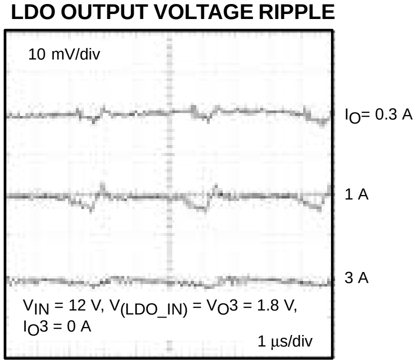


Figure 36

SBRC CH1 LOAD TRANSIENT RESPONSE

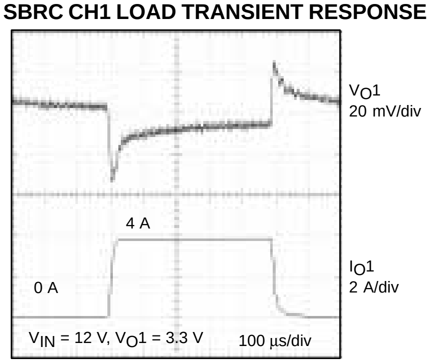


Figure 37

SBRC CH2 LOAD TRANSIENT RESPONSE

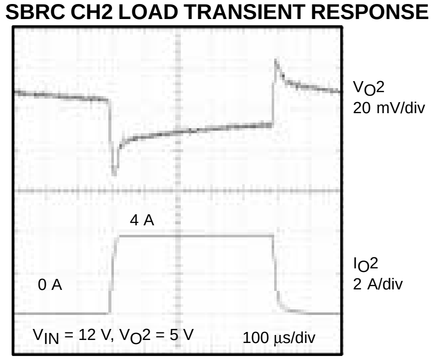


Figure 38

SBRC CH3 LOAD TRANSIENT RESPONSE

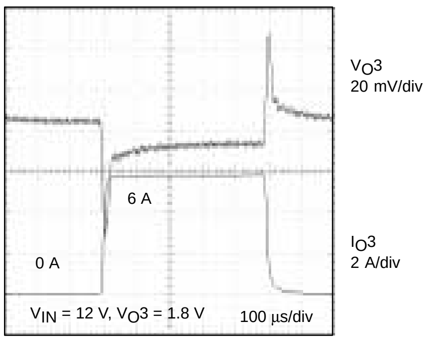


Figure 39

LDO LOAD TRANSIENT RESPONSE

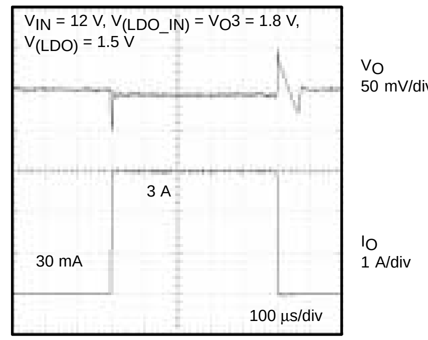


Figure 40

SBRC CH1 GAIN AND PHASE

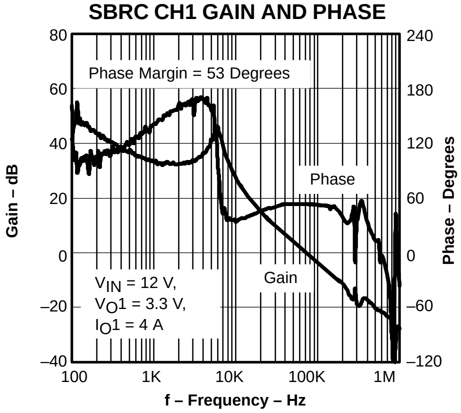


Figure 41

SBRC CH2 GAIN AND PHASE

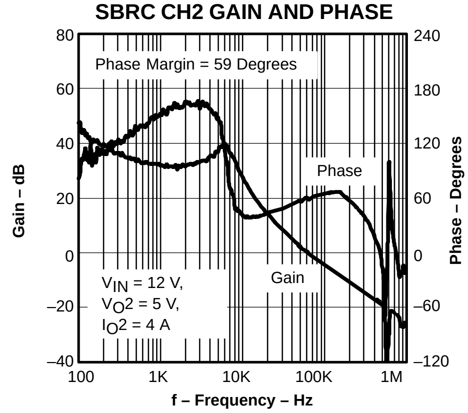


Figure 42

SBRC CH3 GAIN AND PHASE

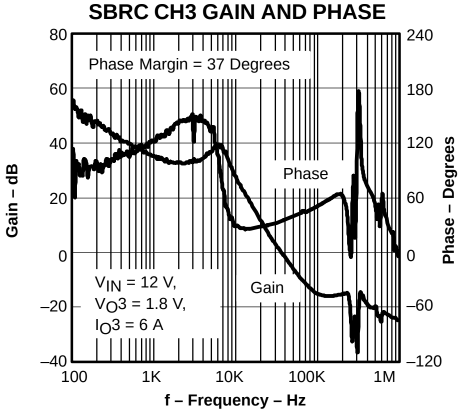


Figure 43

LDO GAIN AND PHASE

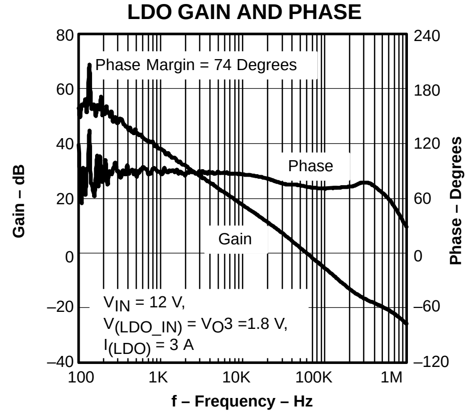
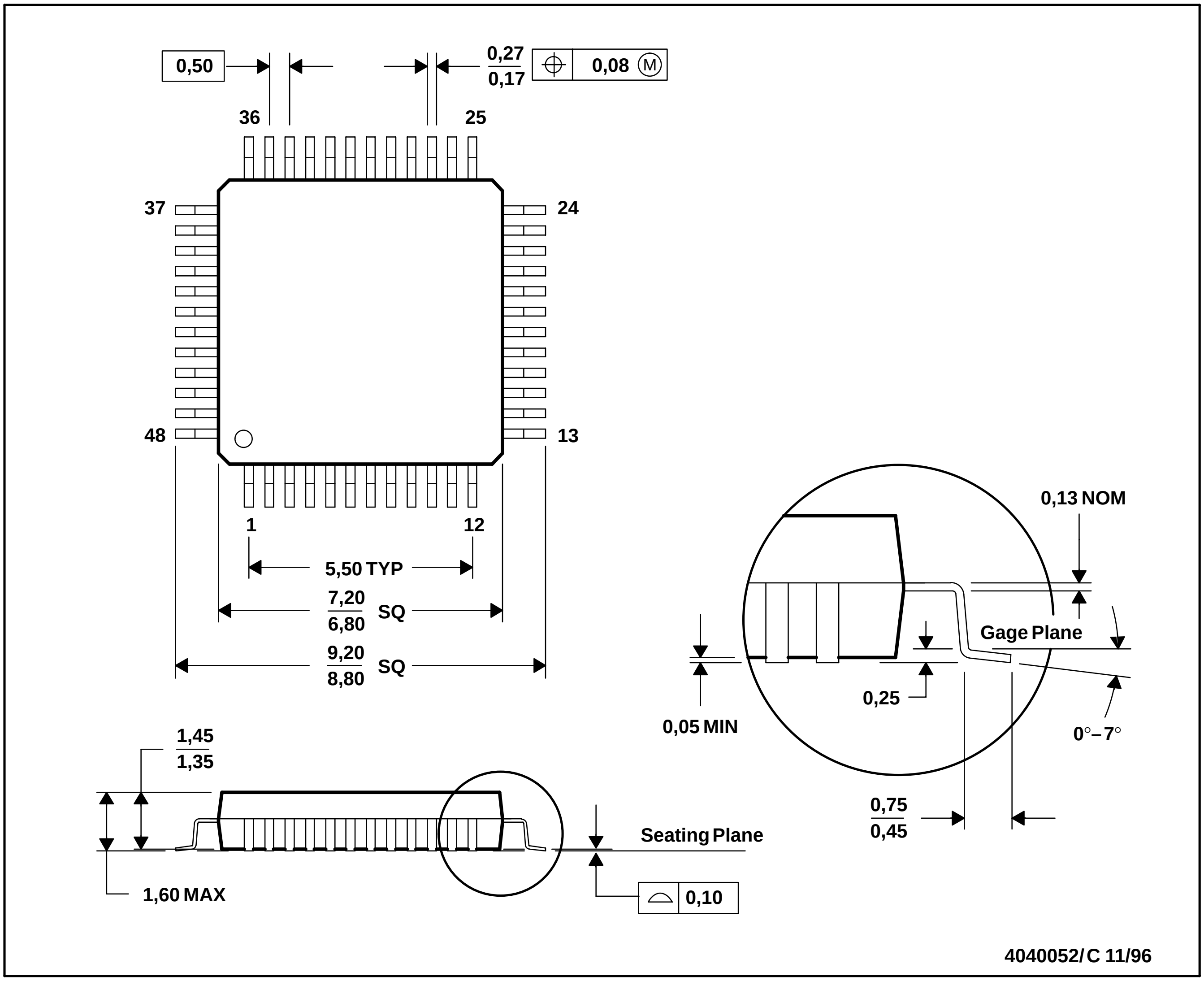


Figure 44

MECHANICAL DATA

PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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