Stereo 90W (4Ω) Class-T Digital Audio Amplifier using Digital Power Processing™ Technology TA2022

ADVANCED INFORMATION - December 2000

General Description

The TA2022 is an 90W continuous average, per channel, Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Applications

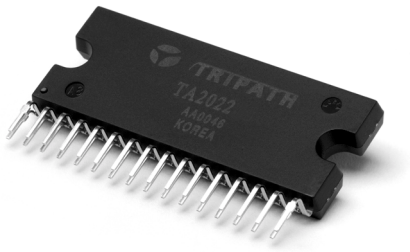
- DVD Players
- Mini/Micro Component Systems
- Home Theater
- Powered Speakers

Benefits

- Fully integrated solution with internal FETs
- Dramatically improves efficiency versus Class-AB
- Signal fidelity equal to high quality linear amplifiers
- High dynamic range compatible with digital media such as CD, DVD, and internet audio

Features

- Class-T architecture
- High Power
  - 100W @ 4Ω, 1.0% THD+N
  - 90W @ 4Ω, 0.1% THD+N
  - 60W @ 8Ω, 0.1% THD+N
- "Audiophile" Quality Sound
  - 0.015% THD+N @ 70W 4Ω
  - 0.015% THD+N @ 45W 8Ω
  - 0.10% IHF-IM @ 25W 4Ω
- High Efficiency
  - 92% @ 88W 8Ω
  - 87% @ 125W 4Ω
- Dynamic Range = 102 dB
- Mute Input
- Over-current protection
- Over and under-voltage protection
- Single ended outputs
- Outputs can be operated in bridged mode
- 32-pin SSIP package



Absolute Maximum Ratings (Note 1)

SYMBOL	PARAMETER	Value	UNITS
VPP, VNN	Supply Voltage (VPP1, VPP2, VNN1, VNN2)	+/-40	V
V5	Positive 5V Bias Supply Voltage at Input Pins (pins 18, 19, 23, 24, 26, 28, 29, 30, 31, 32)	6 -0.3V to (V5 +0.3V)	V V
VN10	Voltage for low-side FET drive	VNN + 13	V
T_{STORE}	Storage Temperature Range	-55° to 150°	C
T_A	Operating Free-air Temperature Range (Note 2)	-40° to 85°	C
T_J	Junction Temperature	150°	C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 3) All pins (except pin 27) Pin 27	 4000 1500	 V V
ESD_{MM}	ESD Susceptibility – Machine Model (Note 4) All pins	 200	 V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: This is a target specification. Characterization is still needed to validate this temperature range.
Note 3: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 4: Machine model, 220pF – 240pF discharged through all pins.

Operating Conditions (Note 5)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VPP, VNN	Supply Voltage (VPP1, VPP2, VNN1, VNN2)	+/-12	+/-31	+/-36	V
V5	Positive 5V Bias Supply	4.5	5	5.5	V
VN10	Voltage for low side FET drive (Volts above VNN)	9	11	12	V

Note 5: Recommended Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Thermal Characteristics

SYMBOL	PARAMETER	Value	UNITS
θ_{JC}	Junction-to-case Thermal Resistance	1.0°	C/W
θ_{JA}	Junction-to-ambient Thermal Resistance (still air)	20°	C/W

Electrical Characteristics (Notes 6, 7)

T_A = 25 °C. See Application/Test Circuit on page 7. Unless otherwise noted, the supply voltage is VPP=|VNN|=31V.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
I_q	Quiescent Current (No load, Mute = 0V)	VPP = +31V VNN = -31V (Note 8) V5 = 5V (Note 9) VN10 = 11V (Note 10)		20 55 45 65	 60 80	mA mA mA mA
I_{MUTE}	Mute Supply Current (No load, Mute = 5V)	VPP = +31V VNN = -31V (Note 8) V5 = 5V (Note 9)		0.5 2 20	 25	mA mA mA
V_{IH}	High-level input voltage (MUTE)		3.5			V
V_{IL}	Low-level input voltage (MUTE)				1.0	V
V_{OH}	High-level output voltage (HMUTE)	I_{OH} = 3mA	3.5			V
V_{OL}	Low-level output voltage (HMUTE)	I_{OL} = 3mA			1.0	V
V_{OFFSET}	Output Offset Voltage	No Load, MUTE = Logic low 0.1% R_{FBA}, R_{FBB}, R_{FBC} resistors	-750		750	mV
I_{OC}	Over Current Sense Threshold	TBD	TBD	TBD		A
$I_{VPPSENSE}$	VPPSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 138 62	162 154 79 72	178 87 	µA µA µA µA
$V_{VPPSENSE}$	Threshold Voltages with $R_{VPPSENSE}$ = 249KΩ (Note 11)	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 36.5 17.8	42.8 40.9 22.2 20.4	47.3 24.4 	V V V V
$I_{VNNSENSE}$	VNNSENSE Threshold Currents	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 152 65	174 169 86 77	191 95 	µA µA µA µA
$V_{VNNSENSE}$	Threshold Voltages with $R_{VNNSENSE}$ = 249KΩ (Note 11)	Over-voltage turn on (muted) Over-voltage turn off (mute off) Under-voltage turn off (mute off) Under-voltage turn on (muted)	 -36.2 -14.8	-42.1 -40.8 -20.2 -17.9	-46.8 -22.6 	V V V V

Performance Characteristics – Single Ended (Notes 6, 7)

T_A = 25 °C. Unless otherwise noted, the supply voltage is VPP=|VNN|=31V, the input frequency is 1kHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 7.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average/Channel) (Note 12)	VPP = |VNN| = +/-31V, R_L = 4Ω THD+N = 0.1% THD+N = 1.0% THD+N = 10% VPP = |VNN| = +/-35V, R_L = 8Ω THD+N = 0.1% THD+N = 10%	80	 90 100 125 60 88		 W W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 70W/Channel, R_L = 4Ω VPP = |VNN| = +/-31V P_{OUT} = 45W/Channel, R_L = 8Ω VPP = |VNN| = +/-35V		0.015 0.015		% %
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 4Ω P_{OUT} = 25W/Channel		0.1		%
SNR	Signal-to-Noise Ratio	A-Weighted 0dB = 90W/Channel, R_L = 4Ω		102		dB
CS	Channel Separation	0dB = 25W, R_L = 4Ω,		83		dB
A_V	Amplifier Gain	P_{OUT} = 10W/Channel, R_L = 4Ω, See Application / Test Circuit		18.1		V/V
A_{VERROR}	Channel to Channel Gain Error	P_{OUT} = 10W/Channel, R_L = 4Ω See Application / Test Circuit			0.5	dB
η	Power Efficiency	P_{OUT} = 88W/Channel, R_L = 8Ω P_{OUT} = 125W/Channel, R_L = 4Ω		92 87		% %
I_{SLOAD}	Source Current	P_{OUT} = 125W/Channel, R_L = 4Ω VPP = +31V VNN = -31V V5 = 5V		 4.59 4.61 45		 A A mA
e_{NOUT}	Output Noise Voltage	A-Weighted, input AC grounded		150		μV

Performance Characteristics – Bridged Tied Load (Notes 6, 7)

T_A = 25 °C. Unless otherwise noted, the supply voltage is VPP=|VNN|=30V, the input frequency is 1kHz and the measurement bandwidth is 20kHz.

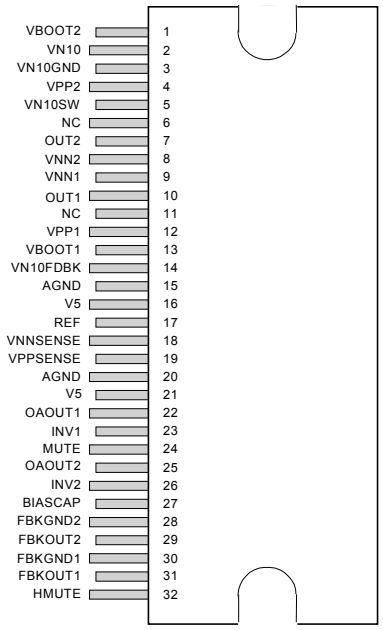
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average) (Note 12)	VPP = |VNN| = +/-30V, R_L = 8Ω THD+N = 0.1% THD+N = 10%		 150 235		 W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 100W, R_L = 8Ω		0.05		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 8Ω P_{OUT} = 25W		0.10		%
η	Power Efficiency	P_{OUT} = 225W, R_L = 8Ω		87		%
SNR	Signal-to-Noise Ratio	A-Weighted, R_L = 8Ω 0dB = 150W		104		dB
e_{NOUT}	Output Noise Voltage	A-Weighted, input AC grounded		220		μV

Note 6: Minimum and maximum limits are guaranteed but may not be 100% tested.
Note 7: For operation in ambient temperatures greater than 25°C, the device must be derated based on the maximum junction temperature and the thermal resistance determined by the mounting technique.
Note 8: This specification includes the current draw from the internal buck regulator.
Note 9: This specification includes the current draw from both the TA2022 and the external feedback biasing.
Note 10: This is the current draw of the VN10 pin if an external “floating” 11V supply is used instead of the internal buck regulator. If an external floating supply is used, the idle current draw of the VNN supply will be approximately 20mA.
Note 11: These supply voltages are calculated using the IVPPSENSE AND IVNNSENSE values shown in the Electrical Characteristics table. The typical voltage values shown are calculated using a RVPPSENSE and RVNNSENSE value of 249kohm without any tolerance variation. The minimum and maximum voltage limits shown include either a +1% or –1% (+1% for Over-voltage turn on and Under-voltage turn off, -1% for Over-voltage turn off and Under-voltage turn on) variation of RVPPSENSE or RVNNSENSE off the nominal 249kohm value. These voltage specifications are examples to show both typical and worst case voltage ranges for a given RVPPSENSE and RVNNSENSE resistor value of 249kohm. Please refer to the Application Information section for a more detailed description of how to calculate the over and under voltage trip voltages for a given resistor value.
Note 12: The supply voltage limitation for 4 ohm single ended (+/-31V), or 8 ohm bridged (+/-30V), is based on the current limit protection circuitry. The current limit circuitry may be activated during large output excursions if the recommended supply voltage ranges are exceeded. This will result in the amplifier being muted.

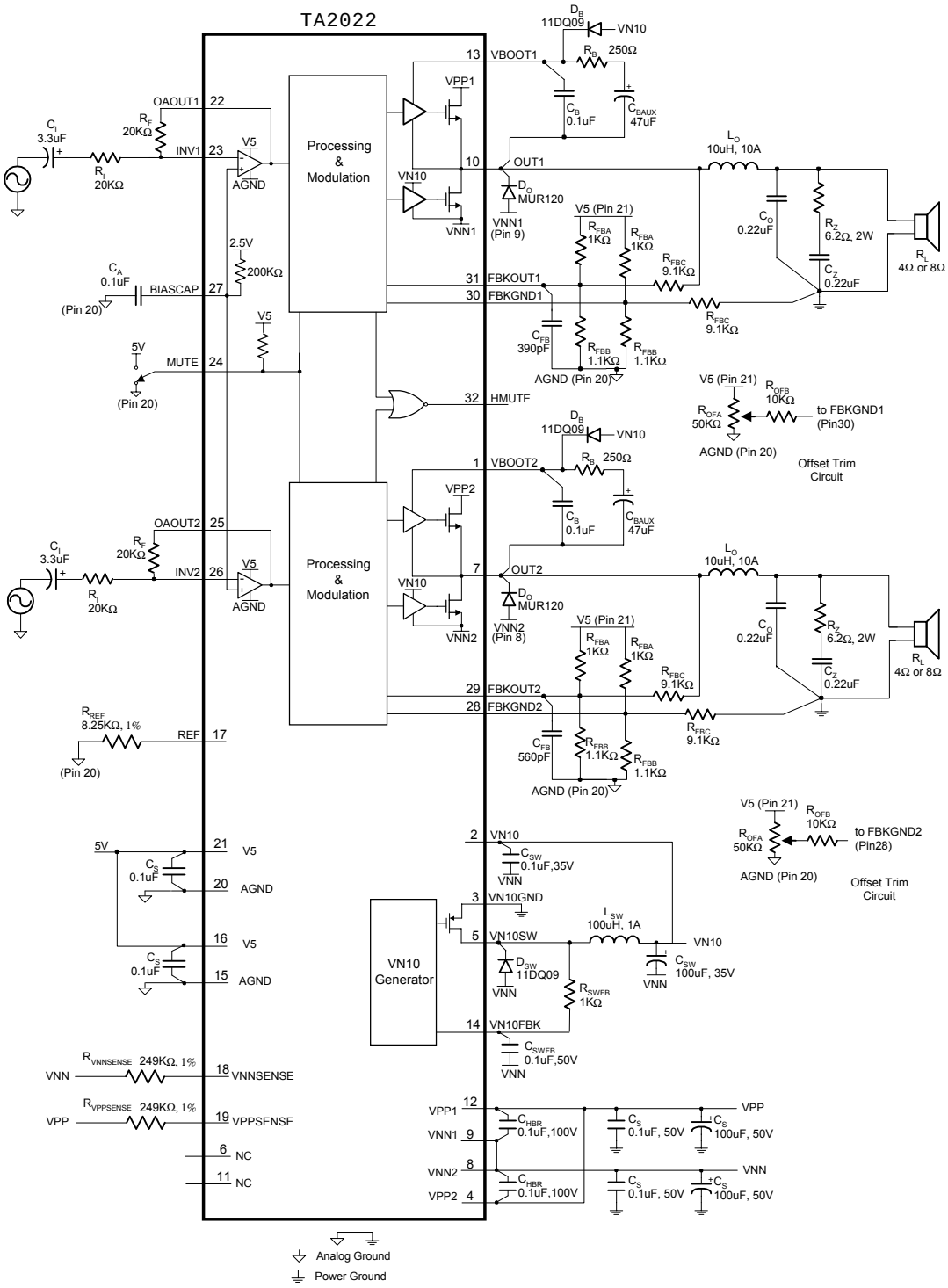
Pin Description

Pin	Function	Description
1, 13	VBOOT2, VBOOT1	Bootstrap voltages for gate drive of high side MOSFET's
2	VN10	"Floating" supply input. Normally connected to the output of onboard VN10 buck converter. This voltage must be stable and referenced to VNN.
3	VN10GND	Power ground for onboard VN10 generator. Electrically tied to the TA2022 case.
4, 12	VPP2, VPP1	Positive power supply input pins.
5	VN10SW	Switching output voltage for onboard VN10 generator (buck converter).
6	NC	Not connected internally. May be connected to pin 7 without any loss of functionality or performance.
7,10	OUT2, OUT1	Power amplifier outputs.
8, 9	VNN2, VNN1	Negative power supply inputs.
11	NC	Not connected internally. May be connected to pin 10 without any loss of functionality or performance.
14	VN10FDBK	Feedback for onboard VN10 generator (nominally 11V above VNN)
15, 20	AGND	Analog Ground.
16, 21	V5	5V power supply input.
17	REF	Used to set internal bias. Typically 1.1V
18	VNNSENSE	Negative supply voltage sense input.
19	VPPSENSE	Positive supply voltage sense input.
22, 25	OAOUT1, OAOUT2	Outputs of Input Stage op amps.
23, 26	INV1, INV2	Inverting inputs of Input Stage op amps.
24	MUTE	Logic input. A logic high puts the amplifier in mute mode. Ground if not used.
27	BIASCAP	Bandgap reference times two (typically 2.5VDC).
28, 29	FBKGND2, FBKOUT2	Output voltage differential feedback for channel 2.
30,31	FBKGND1, FBKOUT1	Output voltage differential feedback for channel 1.
32	HMUTE	Logic Output. A logic high indicates both amplifiers are muted, due to the mute pin state, or a "fault" such as an overcurrent, undervoltage, or overvoltage condition.

32-pin SSIP Package
(Front View)



Application / Test Diagram

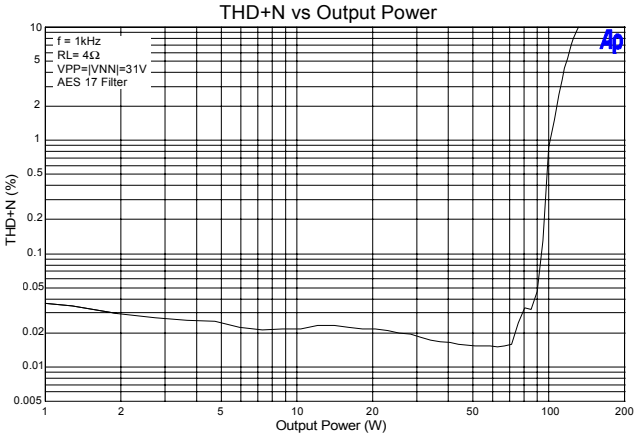


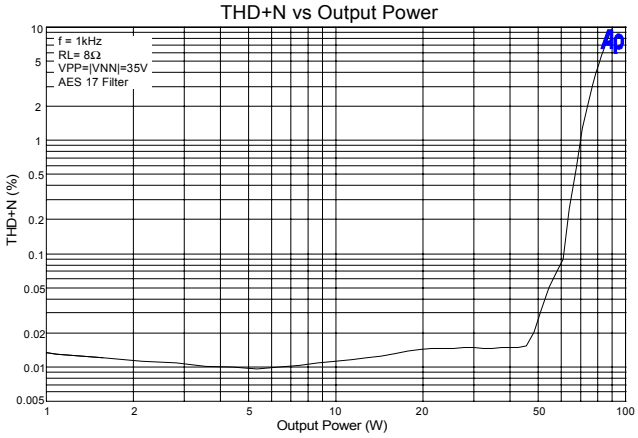
External Components Description (Refer to the Application/Test Circuit)

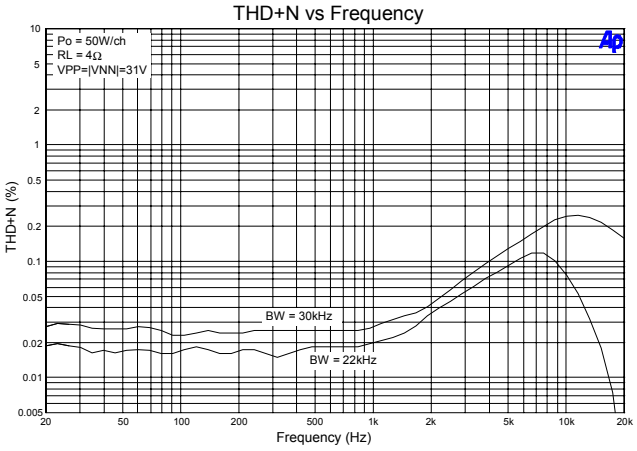
Components	Description
R_I	Inverting input resistance to provide AC gain in conjunction with R_F. This input is biased at the BIASCAP voltage (approximately 2.4VDC).
R_F	Feedback resistor to set AC gain in conjunction with R_I. Please refer to the Amplifier Gain paragraph, in the Application Information section.
C_I	AC input coupling capacitor which, in conjunction with R_I, forms a highpass filter at $f_C = 1/(2\pi R_I C_I)$
R_{FBA}	Feedback divider resistor connected to V5. This resistor is normally set at 1kΩ.
R_{FBB}	Feedback divider resistor connected to AGND. This value of this resistor depends on the supply voltage setting and helps set the TA2022 gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBC}. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
R_{FBC}	Feedback resistor connected from either the OUT1(2) to FBKOUT1(2) or speaker ground to FBKGND1(2). The value of this resistor depends on the supply voltage setting and helps set the TA2022 gain in conjunction with R_I, R_F, R_{FBA}, and R_{FBB}. It should be noted that the resistor from OUT1(2) to FBKOUT1(2) must have a power rating of greater than $P_{DISS} = VPP^2/(2R_{FBC})$. Please see the Modulator Feedback Design paragraphs in the Application Information Section.
C_{FB}	Feedback delay capacitor that both lowers the idle switching frequency and filters very high frequency noise from the feedback signal, which improves amplifier performance. The value of C_{FB} should be offset between channel 1 and channel 2 so that the idle switching difference is greater than 40kHz. Please refer to the Application / Test Circuit.
R_{OFA}	Potentiometer used to manually trim the DC offset on the output of the TA2022.
R_{OFB}	Resistor that limits the manual DC offset trim range and allows for more precise adjustment.
R_{REF}	Bias resistor. Locate close to pin 17 and ground at pin 20.
C_A	BIASCAP decoupling capacitor. Should be located close to pin 27 and grounded at pin 20.
C_B	High frequency bootstrap capacitor, which filters the high side gate drive supply. This capacitor must be located as close to pin 13 (VBOOT1) or pin1 (VBOOT2) for reliable operation. The “negative” side of C_B should be connected directly to OUT1 (pin 10) or OUT2 (pin 7). Please refer to the Application / Test Circuit.
C_{BAUX}	Bulk bootstrap capacitor that supplements C_B during “clipping” events, which result in a reduction in the average switching frequency.
R_B	Bootstrap resistor that limits C_{BAUX} charging current during TA2022 power up (bootstrap supply charging).
D_B	Bootstrap diode that charges C_B, and C_{BAUX} via R_B, when the output is low (at VNN).
C_{SW}	VN10 generator filter capacitors. The high frequency capacitor (0.1uF) must be located close to pin 2 (VN10) to maximize device performance. The bulk capacitor (100uF) should be sized appropriately such that the VN10 voltage does not overshoot with respect to VNN during TA2022 turn on.
L_{SW}	VN10 generator filter inductor. This inductor should be sized appropriately so that L_{SW} does not saturate, and VN10 does not overshoot with respect to VNN during TA2022 turn on.
D_{SW}	Flywheel diode for the internal VN10 buck converter. This diode also prevents VN10SW from going more than one diode drop negative with respect to VNN.
C_{SWFB}	VN10 generator feedback capacitor. This capacitor, in conjunction with R_{SWFB}, filters

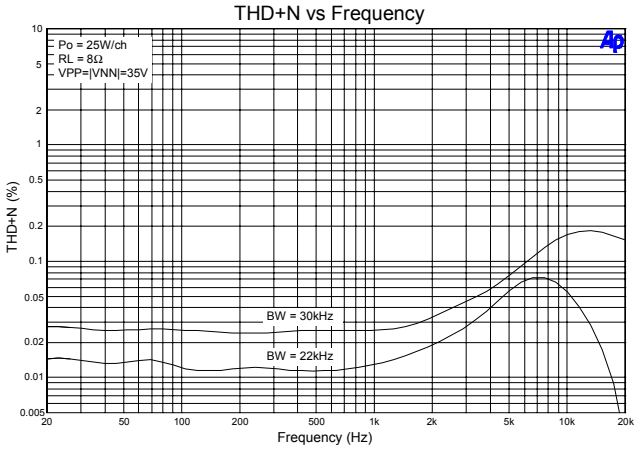
	the VN10 feedback signal such that the loop is unconditionally stable.
R_{SWFB}	VN10 generator feedback resistor. This resistor sets the nominal VN10 voltage. With R_{SWFB} equal to 1kΩ, the internally VN10 voltage will typically be 11V above VNN.
C_S	Supply decoupling for the power supply pins. For optimum performance, these components should be located close to the TA2022 and returned to their respective ground as shown in the Application/Test Circuit.
$R_{VNNSNESE}$	Overvoltage and undervoltage sense resistor for the negative supply (VNN). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band.
$R_{VPPSENSE}$	Overvoltage and undervoltage sense resistor for the positive supply (VPP). Please refer to the Electrical Characteristics Section for the trip points as well as the hysteresis band.
C_{HBR}	Supply decoupling for the high current Half-bridge supply pins. These components must be located as close to the device as possible to minimize supply overshoot and maximize device reliability. These capacitors should have good high frequency performance including low ESR and low ESL. In addition, the capacitor rating must be twice the maximum VPP voltage.
C_Z	Zobel capacitor, which in conjunction with R_Z, terminates the output filter at high frequencies. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs.
R_Z	Zobel resistor, which in conjunction with C_Z, terminates the output filter at high frequencies. The combination of R_Z and C_Z minimizes peaking of the output filter under both no load conditions or with real world loads, including loudspeakers which usually exhibit a rising impedance with increasing frequency. Depending on the program material, the power rating of R_Z may need to be adjusted. The typical power rating is 2 watts.
D_O	Fast Recovery diodes that minimize undershoots of the outputs with respect to power ground during switching transitions as well as output shorts to ground. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective VNN. Please see Application/Test Circuit for VNN return pin.
L_O	Output inductor, which in conjunction with C_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order filter with a cutoff frequency of and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$.
C_O	Output capacitor, which, in conjunction with L_O, demodulates (filters) the switching waveform into an audio signal. Forms a second order low-pass filter with a cutoff frequency of $f_C = 1/(2\pi\sqrt{L_O C_O})$ and a quality factor of $Q = R_L C_O / \sqrt{L_O C_O}$. Use a high quality film capacitor capable of sustaining the ripple current caused by the switching outputs

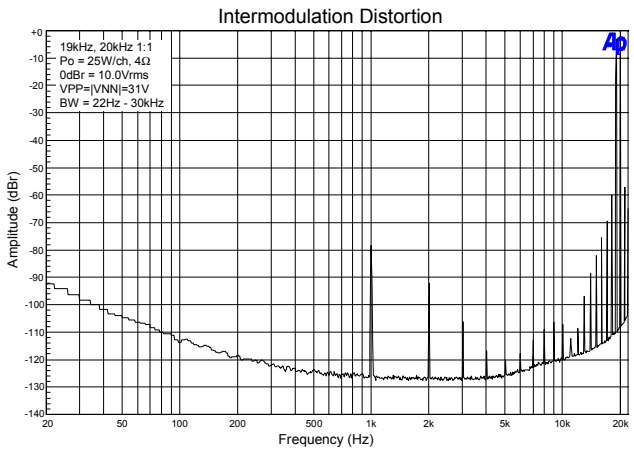
Typical Performance Characteristics – Single Ended

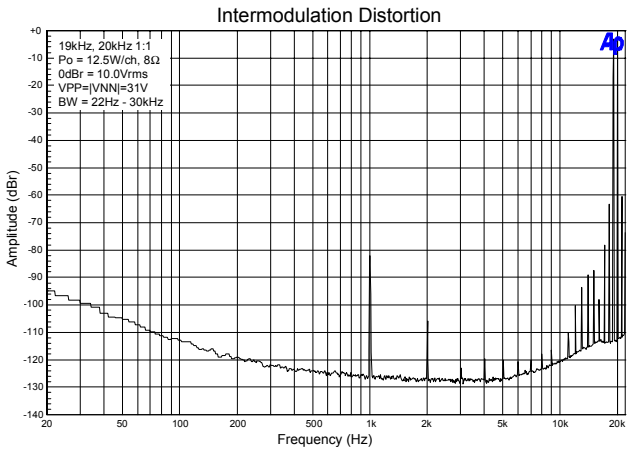






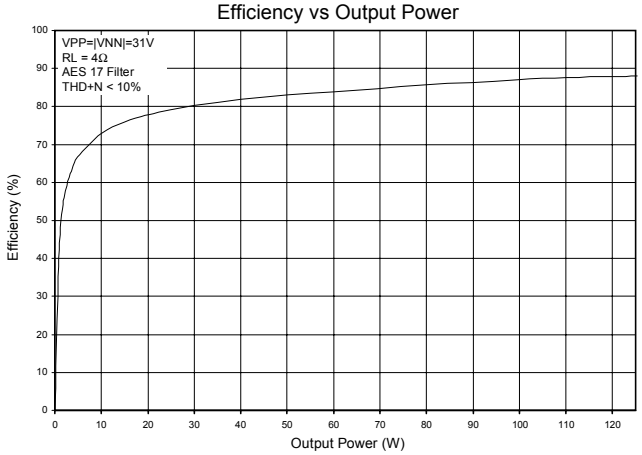




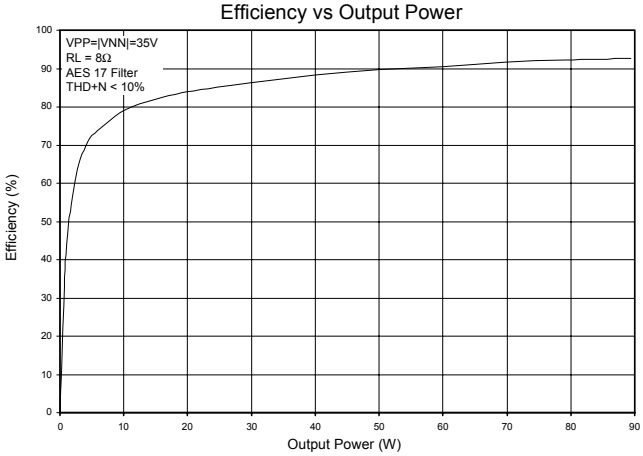


Typical Performance Characteristics – Single Ended

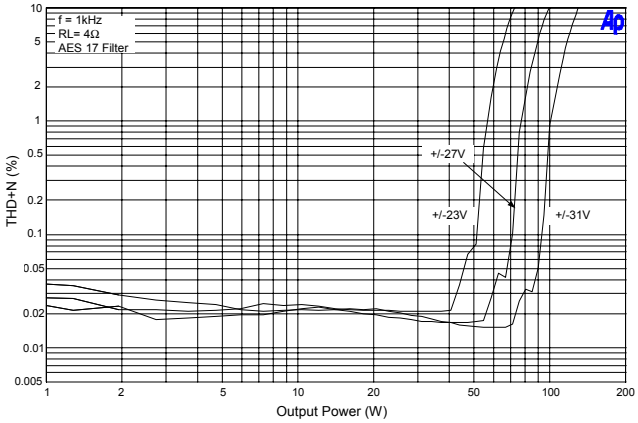
Efficiency vs Output Power



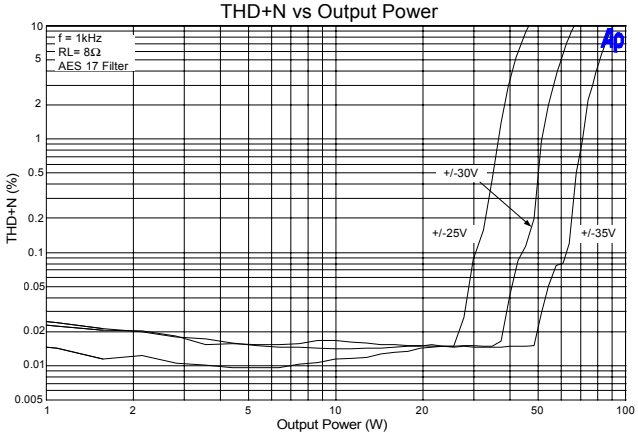
Efficiency vs Output Power



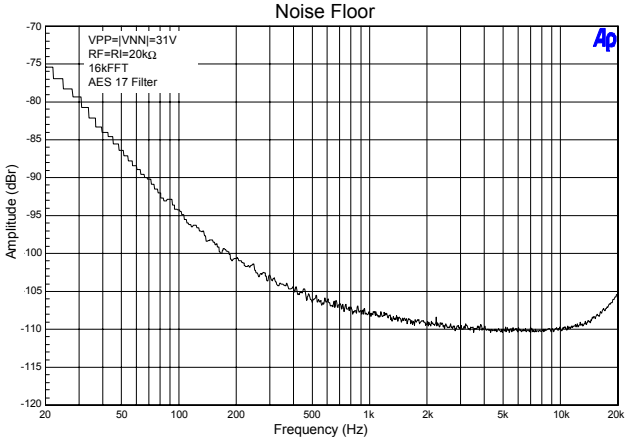
THD+N vs Output Power



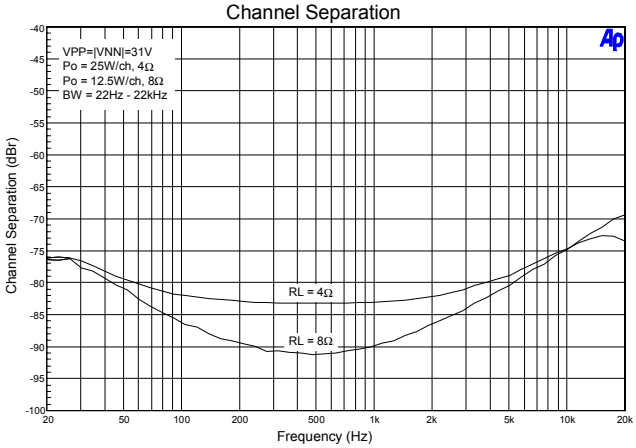
THD+N vs Output Power



Noise Floor

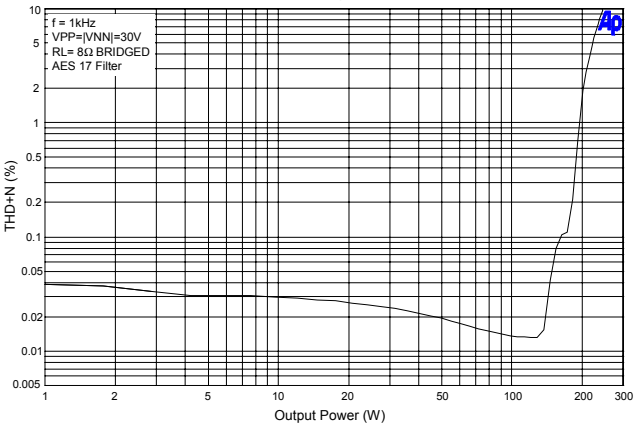


Channel Separation

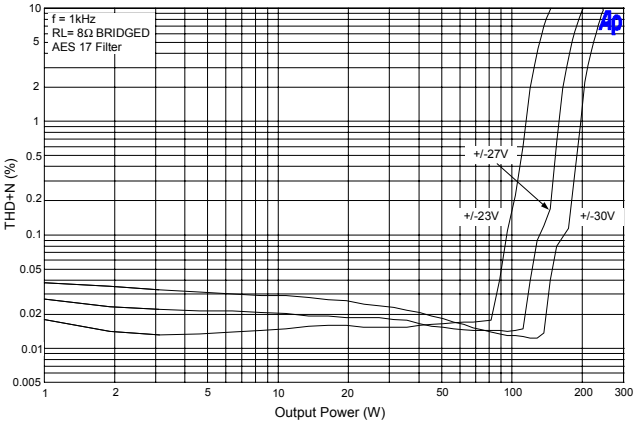


Typical Performance Characteristics - Bridged

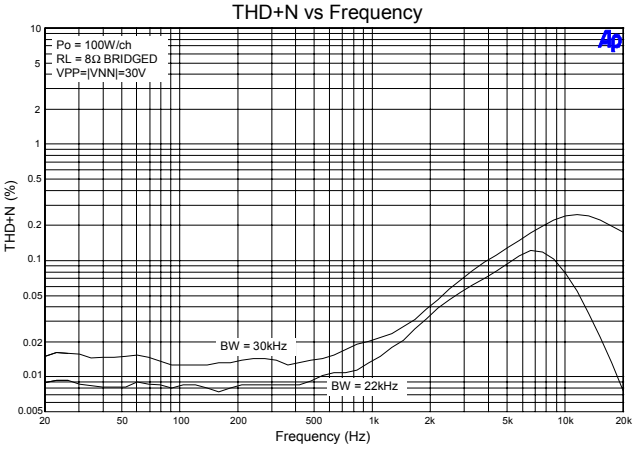
THD+N vs Output Power



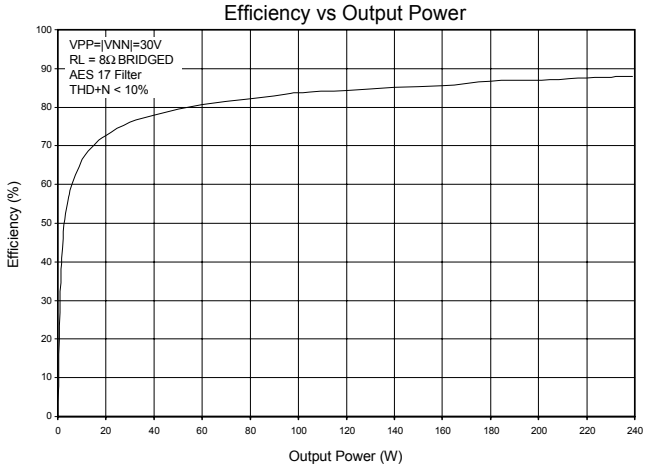
THD+N vs Output Power



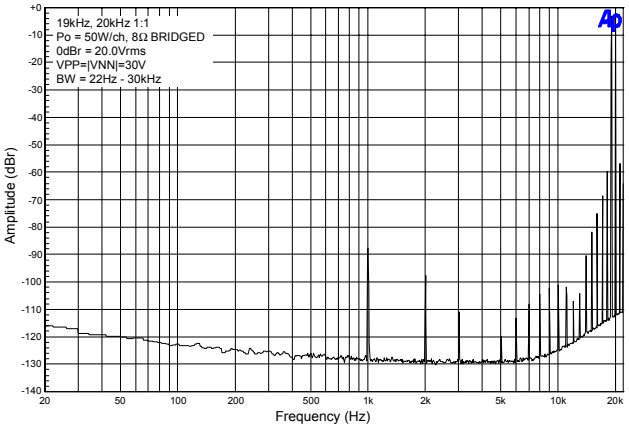
THD+N vs Frequency



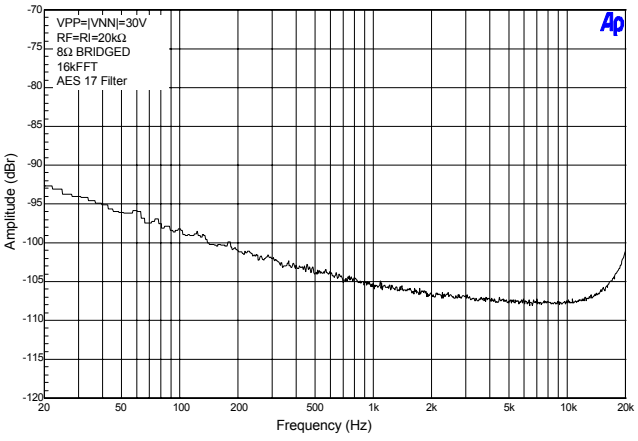
Efficiency vs Output Power



Intermodulation Distortion



Noise Floor



Application Information

TA2022 Basic Amplifier Operation

The TA2022 has three major operational blocks: the signal processor, the MOSFET driver, and the power MOSFETs. The signal processor is a 5V CMOS block that amplifies the audio input signal and converts the audio signal to a switching pattern. This switching pattern is spread spectrum with a typical idle switching frequency of about 650kHz. The switching patterns for the two channels are not synchronized and the idle switching frequencies should differ by at least 40kHz to avoid increasing the audio band noise floor. The idle frequency difference can be accomplished by offsetting the value of C_{FB} for each channel. Typical values of C_{FB} are 390pF for channel 1 and 560pF for channel 2.

The MOSFET driver level-shifts the signal processor's 5V switching patterns to the power supply voltages and drives the power MOSFETs. The MOSFET driver includes a switching power supply integrated to generate the VN10 supply. Special "bootstrapped" supplies (VBOOT1 and VBOOT2) are used to power the high side MOSFET drivers. VN10 must be stable (regulated) at 10V to 12V above VNN. The VN10 circuitry shown in the Application / Test Circuit typically produces 11V above VNN.

The power MOSFETs are N-channel devices configured in half-bridges and are used to supply power to the output load. The outputs of the power MOSFETs (OUT1 and OUT2) must be low pass filtered to remove the high frequency switching pattern. A residual voltage from the switching pattern will remain on the speaker outputs when the recommended output LC filter is used, but this signal is outside of the audio band and will not affect audio performance.

Circuit Board Layout

The TA2022 is a power (high current) amplifier that operates at relatively high switching frequencies. The output of the amplifier switches between VPP and VNN at high speeds while driving large currents. This high-frequency digital signal is passed through an LC low-pass filter to recover the amplified audio signal. Since the amplifier must drive the inductive LC output filter and speaker loads, the amplifier outputs can be pulled above the supply voltage and below ground by the energy in the output inductance. To avoid subjecting the TA2022 to potentially damaging voltage stress, it is critical to have a good printed circuit board layout. It is recommended that Tripath's layout and application circuit be used for all applications and only be deviated from after careful analysis of the effects of any changes.

The following components are important to place near their associated TA2022 pins and are ranked in order of layout importance, either for proper device operation or performance considerations.

- The capacitors C_{HBR} provide high frequency bypassing of the amplifier power supplies and will serve to reduce spikes across the supply rails. C_{HBR} should be kept within 1/8" (3mm) of the VNN(8,9) and VPP(4,12) pins. Please note that both VNN1 and VPP1 as well as VNN2 and VPP2 must be decoupled separately. In addition, the voltage rating for C_{HBR} should be 100V as this capacitor is exposed to the full supply range, VPP-VNN.

- D_O, fast recovery PN junction diodes minimize undershoots of the outputs with respect to power ground during switching transitions and abnormal load conditions such as output shorts to ground. For maximum effectiveness, these diodes must be located close to the output pins and returned to their respective VNN1(2). Please see Application/Test Circuit for ground return pin.

- C_{FB} removes very high frequency components from the amplifier feedback signals and lowers the output switching frequency by delaying the feedback signals. In addition, the value of C_{FB} is different for channel 1 and channel 2 to keep the average switching frequency difference greater than 40kHz. This minimizes in-band audio noise.

- C_B provides high frequency bypassing for the VN10 (pin 2) and bootstrap supplies. Very high currents are present on these supplies.

- C_{SWFB} filters the feedback signal (VN10FDBK) for the hysteretic VN10 buck converter. The feedback signal is noise sensitive and the trace from C_{SWFB} to VNN should be kept short.

- D_{SW} is the flywheel diode for the VN10 buck converter and prevents VN10SW(pin 5) from going more than one diode drop below VNN.

- To minimize noise pickup and minimize THD+N, R_{FBC} should be located as close to the TA2022 as possible.

In general, to enable placement as close to the TA2022, and minimize PCB parasitics, the capacitors listed above should be surface mount types, located on the “solder” side of the board.

Some components are not sensitive to location but are very sensitive to layout and trace routing.

- To maximize the damping factor and reduce distortion and noise, the modulator feedback connections should be routed directly to the inputs of the output inductors. L_O. This was done on the EB-TA2022 board.

- The output filter capacitor, C_O, and zobel capacitor, C_Z, should be star connected with the load return. The output ground feedback signal should be taken from this star point. This is suggested by the routing on the Application/Test schematic, but, for space/layout reasons, this was not fully implemented on the EB-2022.

- The modulator feedback resistors, R_{FBA}, R_{FBB}, and $R_{FBC,}$ should all be grounded and attached to 5V together. These connections will serve to minimize common mode noise via the differential feedback. Please refer to the EB-TA2022 evaluation board for more information.

TA2022 Grounding

Proper grounding techniques are required to maximize TA2022 functionality and performance. Parametric parameters such as THD+N, Noise Floor and Crosstalk can be adversely affected if proper grounding techniques are not implemented on the PCB layout. The following discussion highlights some recommendations about grounding both with respect to the TA2022 as well as general “audio system” design rules.

The TA2022 is divided into two sections: the input section, which spans pin 15 through pin 32, and the output (high power) section, which spans pin 1 through pin 14. On the TA2022 evaluation board, the ground is also divided into distinct sections, one for the input and one for the output. To minimize ground loops and keep the audio noise floor as low as possible, the input and output ground must be only connected at a single point. Depending on the system design, the single point connection may be in the form of a ferrite bead or a PCB trace.

The analog grounds, pin 15 and pin 20 must be connected locally at the TA2022 for proper device functionality. On the TA2022 evaluation board, Tripath has used an analog ground plane to minimize the impedances between pin 15 and pin 20 as well as the other analog ground connections, such as V5 supply bypassing, and feedback divider networks. The ground for the V5 power supply should connect directly to pin 20. Additionally, any external input circuitry such as preamps, or active filters, should be referenced to pin 20.

For the power section, Tripath has traditionally used a "star" grounding scheme. Thus, the load ground returns and the power supply decoupling traces are routed separately back to the power supply. In addition, any type of shield or chassis connection would be connected directly to the ground star located at the power supply. These precautions will both minimize audible noise and enhance the crosstalk performance of the TA2022.

The TA2022 incorporates a differential feedback system to minimize the effects of ground bounce and cancel out common mode ground noise. As such, the feedback from the output ground for each channel needs to be properly sensed. This can be accomplished by connecting the output ground "sensing" trace directly to the star formed by the output ground return, output capacitor, C_O, and the zobel capacitor, C_Z. Refer to the Application / Test Circuit for a schematic description.

Pin 3, VN10GND, is used for the VN10 buck converter. Pin 3 can be connected to the main power supply decoupling ground trace (or plane) without any loss in functionality or reduction of performance. This pins is electrically shorted to the copper heat sink (case) of the TA2022. Even if the internal VN10 regulator is not being used, VN10GND should still be connected to PGND.

TA2022 Amplifier Gain

The gain of the TA2022 is the product of the input stage gain and the modulator gain. Please refer to the sections, Input Stage Design, and Modulator Feedback Design, for a complete explanation of how to determine the external component values.

$$A_{V\,TA2022} = A_{VINPUTSTAGE} * A_{V\,MODULATOR}$$

$$A_{VTA2022} \approx -\frac{R_F}{R_I}\left(\frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1\right)$$

For example, using a TA2022 with the following external components,

R_I = 20kΩ
R_F = 20kΩ
R_{FBA} = 1kΩ
R_{FBB} = 1.13kΩ
R_{FBC} = 9.09kΩ

$$A_{VTA2022} \approx -\frac{20k\,\Omega}{20k\,\Omega}\left(\frac{9.09k\,\Omega * (1.0k\,\Omega + 1.13k\,\Omega)}{1.0k\,\Omega * 1.13k\,\Omega} + 1\right) = 18.13\ \frac{V}{V}$$

Input Stage Design

The TA2022 input stage is configured as an inverting amplifier, allowing the system designer flexibility in setting the input stage gain and frequency response. Figure 1 shows a typical

application where the input stage is a constant gain inverting amplifier. The input stage gain should be set so that the maximum input signal level will drive the input stage output to 4Vpp.

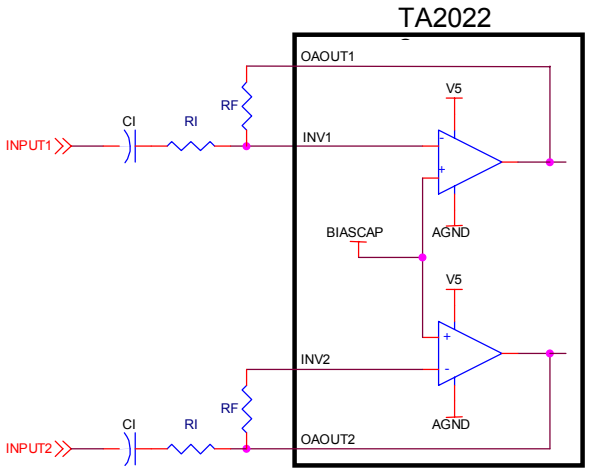


Figure 1: Input Stage

The gain of the input stage, above the low frequency high pass filter point, is that of a simple inverting amplifier:

$$A_{VINPUTSTAGE} = -\frac{R_F}{R_I}$$

Modulator Feedback Design

The modulator converts the signal from the input stage to the high-voltage output signal. The optimum gain of the modulator is determined from the maximum allowable feedback level for the modulator and maximum supply voltages for the power stage. Depending on the maximum supply voltage, the feedback ratio will need to be adjusted to maximize performance. The values of RFBA, RFBB and RFBC (see explanation below) define the gain of the modulator. Once these values are chosen, based on the maximum supply voltage, the gain of the modulator will be fixed even with as the supply voltage fluctuates due to current draw.

For the best signal-to-noise ratio and lowest distortion, the maximum modulator feedback voltage should be approximately 4Vpp. This will keep the gain of the modulator as low as possible and still allow headroom so that the feedback signal does not clip the modulator feedback stage.

Figure 2 shows how the feedback from the output of the amplifier is returned to the input of the modulator. The input to the modulator (FBKOUT1/FBKGND1 for channel 1) can be viewed as inputs to an inverting differential amplifier. R_{FBA} and R_{FBB} bias the feedback signal to approximately 2.5V and R_{FBC} scales the large OUT1/OUT2 signal to down to 4Vpp.

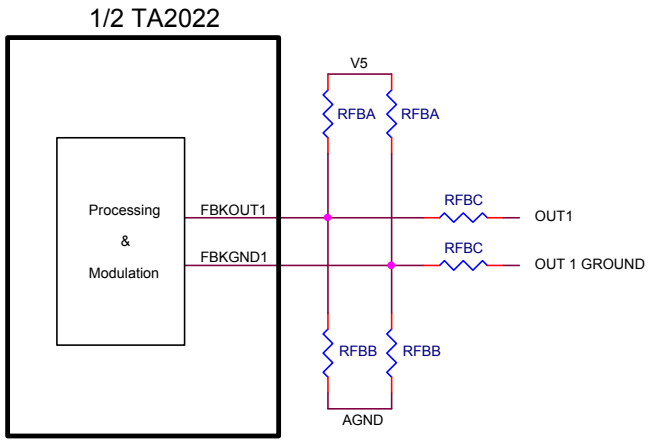


Figure 2: Modulator Feedback

The modulator feedback resistors are:

$$R_{FBA} = \text{User specified, typically } 1K\Omega$$

$$R_{FBB} = \frac{R_{FBA} * VPP}{(VPP - 4)}$$

$$R_{FBC} = \frac{R_{FBA} * VPP}{4}$$

$$A_{V\text{ - MODULATOR}} \approx \frac{R_{FBC} * (R_{FBA} + R_{FBB})}{R_{FBA} * R_{FBB}} + 1$$

The above equations assume that VPP=|VNN|.

For example, in a system with VPP_{MAX}=36V and VNN_{MAX}=-36V,

R_{FBA} = 1kΩ, 1%
R_{FBB} = 1.125kΩ, use 1.13kΩ, 1%
R_{FBC} = 9.0kΩ, use 9.09kΩ, 1%

The resultant modulator gain is:

$$A_{V\text{ - MODULATOR}} \approx \frac{9.09k\ \Omega * (1.0k\ \Omega + 1.13k\ \Omega)}{1.0k\ \Omega * 1.13k\ \Omega} + 1 = 18.13V/V$$

Input Capacitor Selection

C_I can be calculated once a value for R_I has been determined. C_I and R_I determine the input low frequency pole. Typically this pole is set below 10Hz. C_I is calculated according to:

$$C_I = \frac{1}{2\pi f_P R_I}$$

where:
R_I = Input resistor value in ohms.
f_P = Input low frequency pole (typically 10Hz or below).

Mute Control

The mute pin must be driven to a logic low or logic high state for proper operation. The state of the mute pin is “latched in” to minimize the effects of noise on this pin, which could cause the TA2022 to switch state unintentionally. Controlling the mute pin with a push-pull output from a mircocontroller, or a physical switch between V5 and AGND, works well as both solutions have low impedance drive capability. In some cases, it may be desirable to drive the mute pin with an alternative approach. When the device is in mute, the pin must be “pulled low” via approximately 1kohm to overcome the internal latch and change the TA2022 state (i.e. out of mute). When the device is not in mute, the mute pin must be “pulled high” via approximately 2kohm to overcome the internal latch and change the TA2022 state (i.e. into mute). Figure 3 shows a simple control circuit that buffers a Mute Control signal that is not capable of driving the Mute pin of the TA2022 directly. When the Mute Control signal is high, the Mute pin will be driven low and theTA2022 will be on. If the Mute Control signal is low, the 2k resistor will pull the Mute pin high and the TA2022 will be muted.

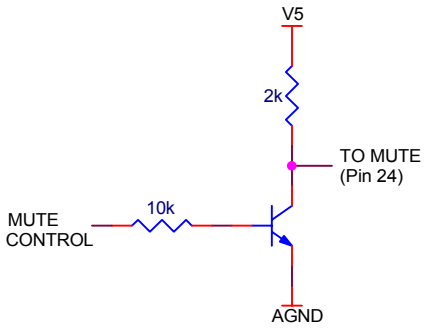


Figure 3: Low impedance drive for Mute Pin

To ensure proper device operation, including minimization of turn on/off transients that can result in undesirable audio artifacts, Tripath recommends that the TA2022 device be muted prior to power up or power down of the 5V supply. The “sensing” of the V5 supply can be easily accomplished by using a “mircocontroller supervisor” or equivalent to drive the TA2022 mute pin high when the V5 voltage is below 4.5V. This will ensure proper operation of the TA2022 input circuitry. A micro-controller supervisor such as the MCP101-450 from Microchip Corporation has been used by Tripath to implement clean power up/down operation.

If turn-on and/or turn-off noise is still present with a TA2022 amplifier, the cause is may be other circuitry external to the TA2022. While the TA2022 has circuitry to suppress turn-on and turn-off transients, the combination of power supply and other audio circuitry with the TA2022 in a particular application may exhibit audible transients. One solution that will completely eliminate turn-on and turn-off pops and clicks is to use a relay to connect/disconnect that amplifier from the speakers with that appropriate timing during power on/off.

TA2022 Output Capability

The TA2022 can output 100 watts into a 4ohm load at 1% THD+N. The maximum amplifier output power is determined by a number of factors including the TA2022 junction temperature, the load impedance and the power supply voltage.

Tripath does not recommend driving loads below 4 ohm as the amplifier efficiency will be seriously reduced and the amplifier may prematurely current limit.

Bridging the TA2022

The TA2022 is can be bridged by returning the signal from OAOUT1 to the input resistor at INV2. OUT1 will then be a gained version of OAOUT1, and OUT2 will be a gained and inverted version of OAOUT1 (see Figure 3). When the two amplifier outputs are bridged, the apparent load impedance seen by each output is halved, so the minimum recommended impedance for bridged operation is 8 ohms. Due to the internal current limit setting, the maximum supply voltage recommended for bridged operation is +/-30V. Bridged operation into loads below 8ohms is possible, but, as mentioned above, the amplifier efficiency will be reduced and the amplifier may prematurely current limit.

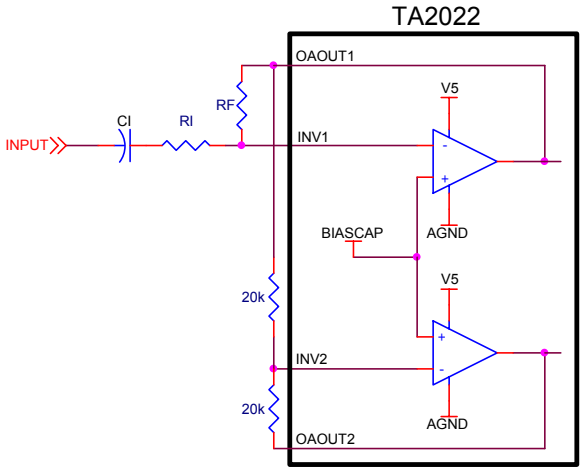


Figure 4: Input Stage Setup for Bridging

The switching outputs, OUT1 and OUT2, are not synchronized, so a common inductor may not be used with a bridged TA2022. For this same reason, individual zobel networks must be applied to each output to load each output and lower the Q of each common mode differential LC filter.

Output Voltage Offset

The output offset voltage of the TA2022 is largely determined by the matching of the respective R_{FBA}, R_{FBB}, and R_{FBC} networks for FBKOUT1(2) and FBKGND1(2). Thus, the intrinsic offset of the TA2022 can be altered by the external feedback network resistor matching. To minimize the nominal untrimmed offset voltage, 1% tolerance resistors are recommended.

In most applications, the output offset voltage will need to be trimmed via an external circuit (either passive or active). The output offset voltage of the TA2022 can be nulled by modifying the

modulator feedback as shown in Figure 4. Potentiometer R_{OFA} is used to trim the effective resistance seen by the output ground, and therefore the output offset. ROFB limits the trim range.

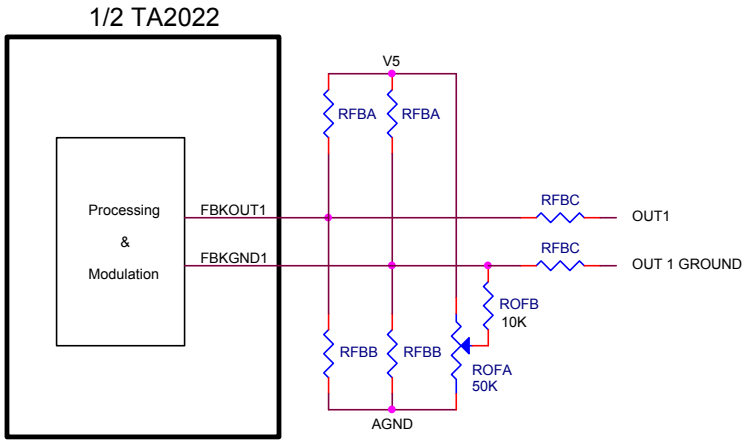


Figure 5: Manual Output Offset Trim Circuit

A DC servo can also be used to automatically null any offset voltage. Please see the EB-2022 documentation.

Output Filter Design

Tripath amplifiers generally have a higher switching frequency than PWM implementations allowing the use of higher cutoff frequency filters, reducing the load dependent peaking/drooping in the 20kHz audio band. This is especially important for applications where the end customer may attach any speaker to the amplifier (as opposed to a system where speakers are shipped with the amplifier), since speakers are not purely resistive loads and the impedance they present changes over frequency and from speaker model to speaker model. An RC network, or "zobel" (R_Z, C_Z) should be placed at the filter output to control the impedance "seen" by the TA2022. The TA2022 works well with a 2nd order, 80kHz LC filter with L_O = 10uH and C_O = 0.22uF and R_Z = 6ohm and C_Z = 0.22uF.

Output inductor selection is a critical design step. The core material and geometry of the output filter inductor affects the TA2022 distortion levels, efficiency, power dissipation and EMI output. The inductor should have low loss at 700kHz with 80Vpp. Tripath has used:

- Micrometals (www.micrometals.com) type-2 toroidal iron powder cores, which have low loss, good linearity and low EMI radiation. The specific core was a T106-2 wound to 11uH with 16AWG wire. Tripath has also used T94-2 cores wound to 11uH with good success.

- JWMiller 5502 10uH rod core inductors, which have excellent linearity, approximately 1 watt of core loss and high EMI radiation.

- ISI RPC-100-10 10uH vertical rod core inductors, which have good linearity, medium core loss and high EMI radiation.

Power Supplies

The TA2022 requires the split supply rails VPP1(VPP2) and VNN1(VNN2), and V5. It also uses some additional voltages, VN10, VBOOT1 and VBOOT2 that are generated internally. The selection of components for the switching regulator is shown in the Application / Test Diagram.

Minimum and Maximum Supply Voltage Operating Range

The TA2022 can operate over a wide range of power supply voltages from +/-12V to +/-36V. In order to optimize operation for either the low or high range, the user must select the proper values for $R_{VNNSENSE}$, $R_{VPPSENSE}$, R_{FBA}, R_{FBB}, and R_{FBC}. Please refer to the Modulator Feedback Design and Over/Under-voltage Protection sections for more additional information.

VN10 (Pin 2)

The TA2022 has an internal hysteretic buck converter, which, in conjunction with a handful of passive components, generates the necessary floating power supply for the mosfet driver stage (nominally 11V with the external components shown in Application / Test Circuit). The performance curves shown in the data sheet as well as efficiency measurements were done using the internal VN10 generator. Tripath recommends that the internal VN10 generator be used.

In some cases, though, a designer may wish to use an external VN10 generator. The specification for VN10 quiescent current (65mA typical, 80mA maximum) in the Electrical Characteristics section states the amount of current needed when an external floating supply is used. If the internal VN10 generator is not used, Tripath recommends shorting VN10SW(pin 5) to VN10GND(pin 3) and VN10FDBK(pin 14) to VN10GND(pin 3). VN10GND should still be connected to the system power (high current) ground star for noise reasons.

The external VN10 supply must be able to source a maximum of 80mA into the VN10 pin. Thus, a positive supply must be used. In addition, this supply must be referenced to the VNN rail. If the external VN10 supply does not track fluctuations in the VNN supply or is not able to source current into the VN10 pin, the TA2022 will, at the very least, not work, but more likely, be permanently damaged.

Figure 6 shows a simple circuit for an external VN10 supply. Though simple, there is one problem with this circuit; the maximum input voltage of the 7810. If the maximum input voltage of the 7810 is exceeded (typically this voltage is 35V), then the 7810 will be damaged which will likely cause damage to the TA2022. Thus, this circuit should only be used where the VNN power supply is well regulated even under heavy load conditions (including the effects of power supply pumping).

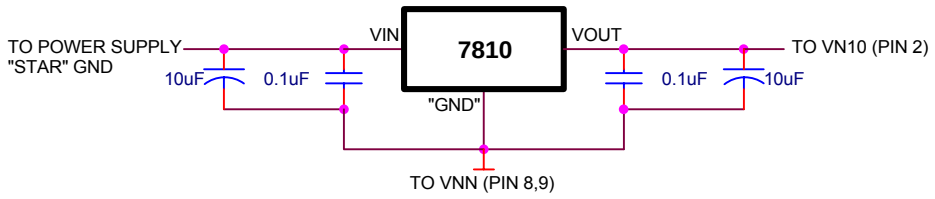


Figure 6: Simple External VN10 Supply

Figure 7 shows a much more robust VN10 supply. In this case, the maximum supply differential the LM317 experiences is the input voltage minus the output voltage. The maximum differential specification is 40V for the LM317. When used as the VN10 supply for the TA2022, the maximum differential the LM317 will experience is 25V, even at maximum operating voltage of 36V for the TA2022. As configured, VOUT will be about 10.63V above VNN.

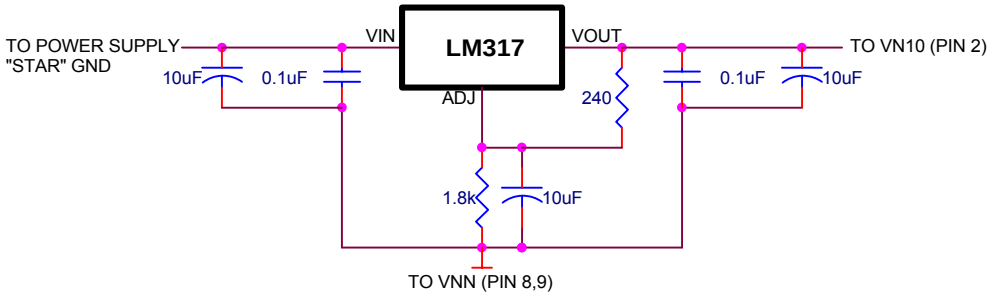


Figure 7: Robust External VN10 Supply

It should be noted that the maximum power dissipation for either Figure 6 or Figure 7 is:

$$PD_{MAX} = (VIN - VOUT) \times IOUT \approx (31V - 11V) \times 80mA(max.) = 1.6W$$

Thus, the LM7810 or LM317 must be sufficiently heat sinked to sustain 80mA in the system ambient temperature. In the case where multiple TA2022's are run off the same VN10 generator, the power dissipation may be prohibitively large for the linear regulator in conjunction with allowable heat sink. In these cases, a more sophisticated scheme using an additional transformer secondary winding referenced to VNN may be necessary to minimize the linear regulator power dissipation.

Protection Circuits

The TA2022 is guarded against over-current, over / under-voltage and over-temperature conditions. If the device goes into an over-current or over / under-voltage condition, the HMUTE goes to a logic HIGH indicating a fault condition. When this occurs, the amplifier is muted, all outputs are TRI-STATED, and will float to approximately 2.5VDC.

Over-current Protection

An over-current fault occurs if more than approximately 8 amps of current flows from any of the amplifier output pins. This can occur if the speaker wires are shorted together or if one side of the speaker is shorted to ground. An over-current fault sets an internal latch that can only be cleared if the MUTE pin is toggled or if the part is powered down. See the over-current curves in the Typical Characteristics section for more information.

Over / Under-voltage Protection

The TA2022 has built-in over and under voltage protection for both the VPP and VNN supply rails. The nominal operating voltage will typically be chosen as the supply "center point." This allows the supply voltage to fluctuate, both above and below, the nominal supply voltage.

VPPSENSE (pin 19) performs the over and undervoltage sensing for the positive supply, VPP. VNNSENSE (pin 18) performs the same function for the negative rail, VNN. In the simplest implementation, the supply is done via a single, external resistor per sense pin. When the current through $R_{VPPSENSE}$ (or $R_{VNNSENSE}$) goes below or above the values shown in the Electrical Characteristics section (caused by changing the power supply voltage), the TA2022 will be muted. VPPSENSE is internally biased at 2.5V and VNNSENSE is biased at 1.25V. For the single resistor sense case (as shown in the Application / Test Diagram), these bias points must be taken into consideration when calculating the $R_{VPPSENSE}$ or $R_{VNNSENSE}$ resistor.

Once the supply comes back into the supply voltage operating range (as defined by the supply sense resistors), the TA2022 will automatically be unmuted and will begin to amplify. There is a hysteresis range on both the VPPSENSE and VNNSENSE pins. If the amplifier is powered up in the hysteresis band the TA2022 will be muted. Thus, the usable supply range is the difference between the over-voltage turn-off and under-voltage turn-off for both the VPP and VNN supplies. It should be noted that there is a timer of approximately 200mS with respect to the over and under voltage sensing circuit. Thus, the supply voltage must be outside of the user defined supply range for greater than 200mS for the TA2022 to be muted.

The equation for calculating $R_{VPPSENSE}$ is as follows:

$$R_{VPPSENSE} = \frac{VPP - 2.5V}{I_{VPPSENSE}}$$

The equation for calculating $R_{VNNSENSE}$ is as follows:

$$R_{VNNSENSE} = \frac{1.25V - VNN}{I_{VNNSENSE}}$$

where $I_{VPPSENSE}$ or $I_{VNNSENSE}$ can be any of the currents shown in the Electrical Characteristics table for VPPSENSE and VNNSENSE, respectively.

Example: Nominal supply voltage – +/-32.5V +/-10%

From this information, a value of $R_{VPPSENSE}$ and $R_{VNNSENSE}$ can be calculated using the above formulas.

$$VPP_{MAX} = 32.5V \times 1.1 = 35.75V \quad \text{use } 36V$$

$$VNN_{MAX} = -32.5V \times 1.1 = -35.75V \quad \text{use } -36V$$

$$R_{VPPSENSE} = \frac{36V - 2.5V}{138\ \mu A} = 242.75\ k\Omega \quad \text{use } 243\ k\Omega, 1\%$$

where $I_{VPPSENSE}$ is the minimum over-voltage turn off current for VPPSENSE.

$$R_{VNNSENSE} = \frac{1.25V - -36V}{152\ \mu A} = 245.1\ k\Omega \quad \text{use } 249\ k\Omega, 1\%$$

where $I_{VNNSENSE}$ is the minimum over-voltage turn off current for VNNSENSE.

Using the resistor values from above, the actual minimum over voltage turn off points will be:

$$VPP_{MIN\_OV\_TUR\ N\_OFF} = 243\,k\Omega \times 138\,\mu A + 2.5V = 36.03V$$
$$VNN_{MIN\_OV\_TUR\ N\_OFF} = 1.25V - 249\,k\Omega \times 152\,\mu A = -36.60V$$

The other three trip points can be calculated using the same formula but inserting the appropriate $I_{VPPSENSE}$ (or $I_{VNNSENSE}$) current value. As stated earlier, the usable supply range is the difference between the minimum overvoltage turn off and maximum under voltage turn-off for both the VPP and VNN supplies.

$$VPP_{RANGE} = VPP_{MIN\_OV\_TUR\ N\_OFF} - VPP_{MAX\_UV\_TUR\ N\_OFF}$$
$$VNN_{RANGE} = VNN_{MIN\_OV\_TUR\ N\_OFF} - VNN_{MAX\_UV\_TUR\ N\_OFF}$$

Using the resistor values from above, and the maximum under voltage trip currents shown in the Electrical Characteristics table, the maximum under voltage turn off points will be:

$$VPP_{MAX\_UV\_TUR\ N\_OFF} = 243\,k\Omega \times 87\,\mu A + 2.5V = 23.64V$$
$$VNN_{MAX\_UV\_TUR\ N\_OFF} = 1.25V - 249\,k\Omega \times 95\,\mu A = -22..41V$$

and the resultant supply ranges will be:

$$VPP_{RANGE} = 36.03 - 23.64V = 12.39V$$
$$VNN_{RANGE} = -36.60 - -22.41V = -14.19V$$

It should also be noted that the tolerance of the $R_{VPPSENSE}$ (or $R_{VNNSENSE}$) resistors will effect the trip voltages and thus, the usable supply range. To minimize the additional variance Tripath recommends 1% tolerance resistors.

As a matter of completeness, the formulas below include the effect of resistor tolerance assuming a known value of $R_{VPPSENSE}$ or $R_{VNNSENSE}$.

$$VPP_{MIN\_OV\_TUR\ N\_OFF} = (R_{VPPSENSE} \times I_{TRIP}) \div (1 + TOL/100) + 2.5V$$
$$VPP_{MAX\_UV\_TUR\ N\_OFF} = (R_{VPPSENSE} \times I_{TRIP}) \times (1 + TOL/100) + 2.5V$$

$$VNN_{MIN\_OV\_TUR\ N\_OFF} = 1.25 - (R_{VNNSENSE} \times I_{TRIP}) \div (1 + TOL/100)$$
$$VNN_{MAX\_UV\_TUR\ N\_OFF} = 1.25 - (R_{VNNSENSE} \times I_{TRIP}) \times (1 + TOL/100)$$

Using a value of 243kΩ for $R_{VPPSENSE}$ and a value of 249kΩ for $R_{VNNSENSE}$, assuming 5% tolerance, along with the appropriate value of I_{TRIP}, the trip voltages and supply ranges can be calculated.

$$VPP_{MIN\_OV\_TUR\ N\_OFF} = (243\,k\Omega \times 138\,\mu A) \div (1 + 5/100) + 2.5V = 34.44V$$
$$VPP_{MAX\_UV\_TUR\ N\_OFF} = (243\,k\Omega \times 87\,\mu A) \times (1 + 5/100) + 2.5V = 24.70V$$
$$VPP_{RANGE} = 34.44 - 24.70V = 9.74V$$

$$VNN_{MIN\_OV\_TURN\_OFF} = 1.25 - (249\,k\Omega \times 152\,\mu A) \div (1 + 5/100) \quad = -34.80V$$
$$VNN_{MAX\_UV\_TURN\_OFF} = 1.25 - (249\,k\Omega \times 95\,\mu A) \times (1 + 5/100) \quad = -23.59V$$
$$VNN_{RANGE} = -34.80 - -23.59V \quad = \quad -11.21V$$

Thus, by using 5% resistors, the supply range for the VPP has been reduced by 2.65V while the VNN range has been reduced by approximately 3.0V (as compared to resistors with no tolerance variation). In actuality, if a 5% resistor was to be used, then the initial value of $R_{VPPSENSE}$ and $R_{VNNSENSE}$ would have had to be adjusted such that the minimum over voltage turn off points would have never been less than +/-36V as defined by the supply voltage and tolerance specification.

It should be noted that the values for $V_{VPPSENSE}$ and $V_{VNNSENSE}$ shown in the Electrical Characteristics table were calculated using a value of 249kΩ for both $R_{VPPSENSE}$ and $R_{VNNSENSE}$. In addition, for the maximum and minimum values, as opposed to the typical ones, a 1% tolerance resistor value around 249kΩ was chosen to show the effect on supply range. Thus, the minimum and maximum values would be “worst case” assuming a supply voltage of 5V for the input section of the TA2022.

Over-temperature Protection

An over-temperature fault occurs if the junction temperature of the part exceeds approximately 165°C. The thermal hysteresis of the part is approximately 30°C, therefore the fault will automatically clear when the junction temperature drops below 135°C.

HMUTE (pin 32)

The HMUTE pin is a 5V logic output that indicates various fault conditions within the device. These conditions include: over-current, overvoltage and undervoltage. The HMUTE output is capable of directly driving an LED through a series 2kΩ resistor.

Heat Sink Requirements

In most applications it will be necessary to fasten the TA2022 to a heat sink. The determining factor is that the 150°C maximum junction temperature, T_J(max) cannot be exceeded, as specified by the following equation:

$$P_{DISS} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

where:

P_{DISS} = maximum power dissipation
T_{JMAX} = maximum junction temperature of TA2022
T_A = operating ambient temperature
θ_{JA} = junction-to-ambient thermal resistance
$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$

Example:

What size heat sink is required to operate the TA2022 at 80W per channel continuously in a 70ºC ambient temperature?

P_{DISS} is determined by:

$$\text{Efficiency} = \eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} - P_{DISS}}$$

$$P_{DISS}\ (\text{per channel}) = \frac{P_{OUT}}{\eta} - P_{OUT} = \frac{80}{0.85} - 80 = 14.12\text{W}$$

Thus, P_{DISS} for two channels = 28.24W

$$\theta_{JA} = \frac{(T_{J(MAX)} - T_A)}{P_{DISS}} = \frac{150 - 70}{28.24} = 2.83°\text{C/W}$$

The θ_{JC} of the TA2022 is 1.0°C/W, so a heat sink of 1.63°C/W is required for this example (assuming a θ_{CS} = 0.2°C/W). In actual applications, other factors such as the average P_{DISS} with a music source (as opposed to a continuous sine wave) and regulatory agency testing requirements will determine the size of the heat sink required.

TECHNICAL INFORMATION

Performance Measurements of the TA2022

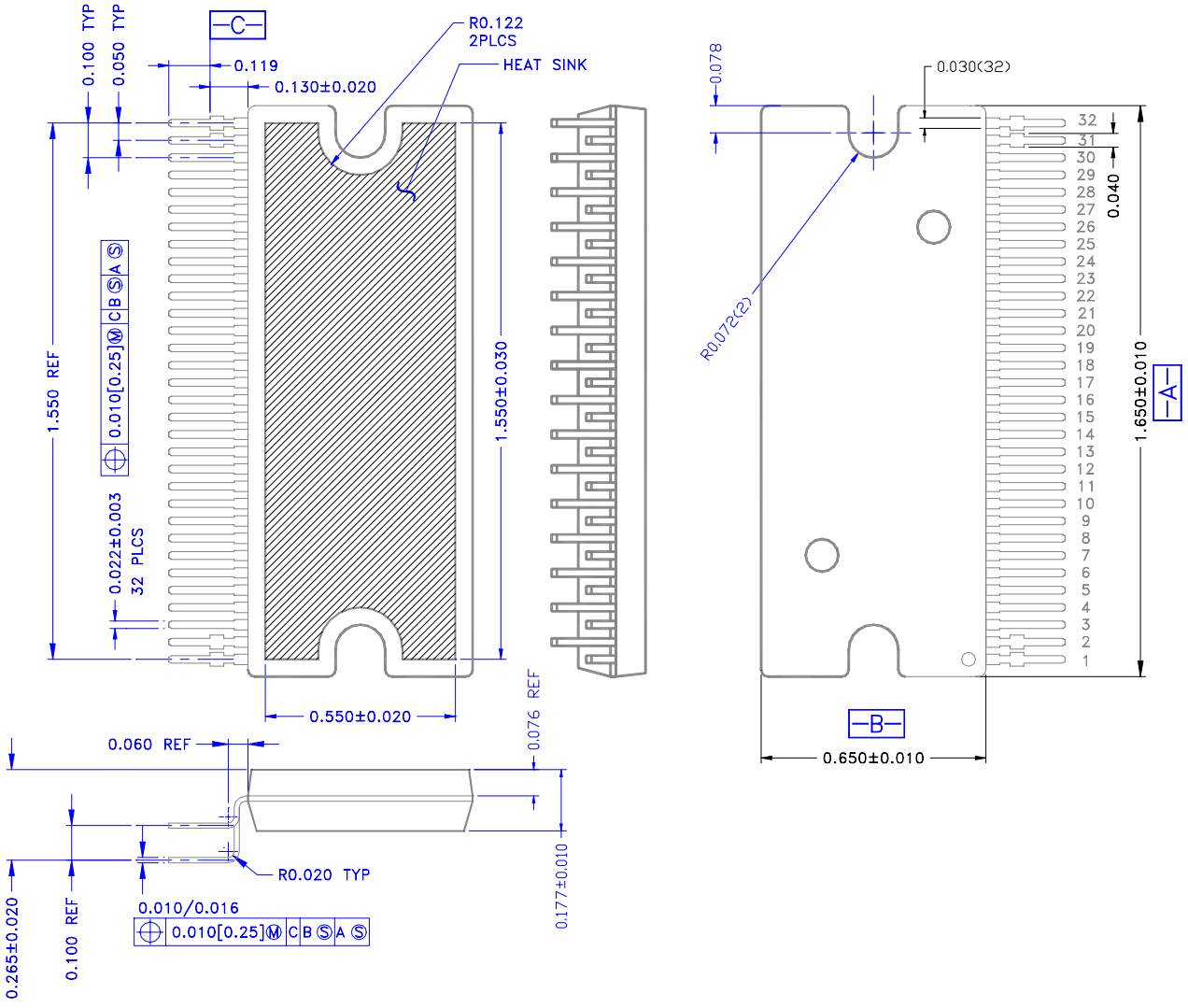
The TA2022 operates by generating a high frequency switching signal based on the audio input. This signal is sent through a low-pass filter (external to the Tripath amplifier) that recovers an amplified version of the audio input. The frequency of the switching pattern is spread spectrum in nature and typically varies between 100kHz and 1MHz, which is well above the 20Hz – 20kHz audio band. The pattern itself does not alter or distort the audio input signal, but it does introduce some inaudible components.

The measurements of certain performance parameters, particularly noise related specifications such as THD+N, are significantly affected by the design of the low-pass filter used on the output as well as the bandwidth setting of the measurement instrument used. Unless the filter has a very sharp roll-off just beyond the audio band or the bandwidth of the measurement instrument is limited, some of the inaudible noise components introduced by the TA2022 amplifier switching pattern will degrade the measurement.

One feature of the TA2022 is that it does not require large multi-pole filters to achieve excellent performance in listening tests, usually a more critical factor than performance measurements. Though using a multi-pole filter may remove high-frequency noise and improve THD+N type measurements (when they are made with wide-bandwidth measuring equipment), these same filters degrade frequency response. The TA2022 Evaluation Board uses the Application/Test Circuit of this data sheet, which has a simple two-pole output filter and excellent performance in listening tests. Measurements in this data sheet were taken using this same circuit with a limited bandwidth setting in the measurement instrument.

Package Information

32-pin SSIP Package:



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