

COMPLIANT HALOGEN

FREE

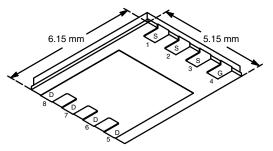
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**Vishay Siliconix** 

# N-Channel Reduced Q<sub>g</sub>, Fast Switching MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)			
30	0.00975 at V <sub>GS</sub> = 10 V	15			
	0.01375 at V <sub>GS</sub> = 4.5 V	13			

#### PowerPAK SO-8



Bottom View

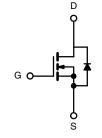
Ordering Information: Si7392DP-T1-E3 (Lead (Pb)-free) Si7392DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low  $Q_{gd}$  for Low Switching Losses TrenchFET<sup>®</sup> Power MOSFET RoHS
- New Low Thermal Resistance PowerPAK<sup>®</sup> Package with Low 1.07 mm Profile
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Complaint to RoHS Directive 2002/95/EC

#### APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook - Server



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b>	$(T_A = 25 \ ^{\circ}C, unle$	ess otherwise i	noted)			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30		V	
Gate-Source Voltage		V <sub>GS</sub>	± 20			
	T <sub>A</sub> = 25 °C	– I <sub>D</sub>	15	9		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 70 °C		12	7		
Pulsed Drain Current		I <sub>DM</sub>	± 50		А	
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	4.1	1.5	mJ	
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	30			
Single-Pulse Avalanche Energy	L = 0.1 mH	H E <sub>AS</sub> 45		45		
	T <sub>A</sub> = 25 °C	– P <sub>D</sub>	5	1.8	W	
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 70 °C		3.2	1.1		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		00	
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 s	R <sub>thJA</sub>	20	25	°C/W	
Maximum Junction-to-Ambient (MOSFET) <sup>a</sup>	Steady State		53	70		
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	3.5	4.5		

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.



Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.0		3.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 V, V_{GS} = 0 V$			1		
		$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 70 ^{\circ}\text{C}$			5	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	40			Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 15 \text{ A}$		0.008	0.00975	Ω	
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 13 \text{ A}$		0.011	0.01375		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		40		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 4.1 A, V <sub>GS</sub> = 0 V		0.75	1.1	V	
Dynamic <sup>b</sup>				•			
Total Gate Charge	Qg			10	15		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 15 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 15 \text{ A}$		3.5		nC	
Gate-Drain Charge	Q <sub>gd</sub>			2.6			
Gate Resistance	R <sub>g</sub>			1.6	2.7	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			15	25		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		7	15	ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong \text{1}$ A, $\text{V}_\text{GEN}=\text{10}$ V, $\text{R}_\text{g}=\text{6}~\Omega$		46	70		
Fall Time	t <sub>f</sub>			9	17		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.7 A, dI/dt = 100 A/μs		30	60		

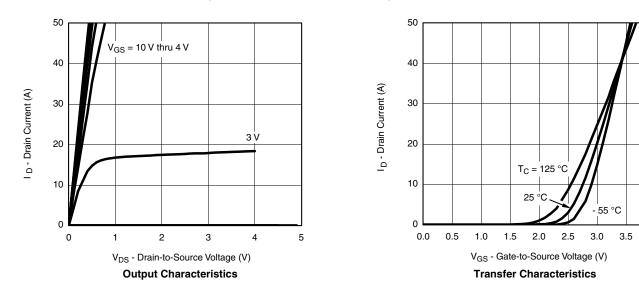
Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



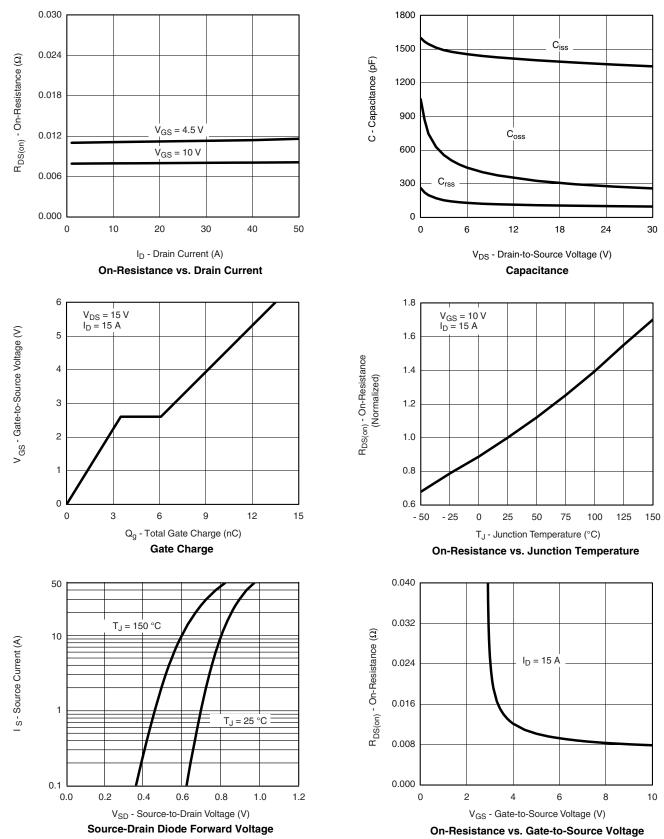
4.0



## Si7392DP

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#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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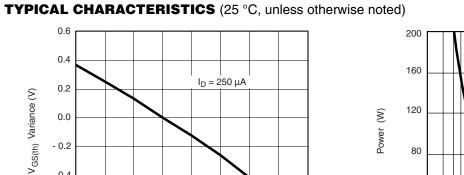
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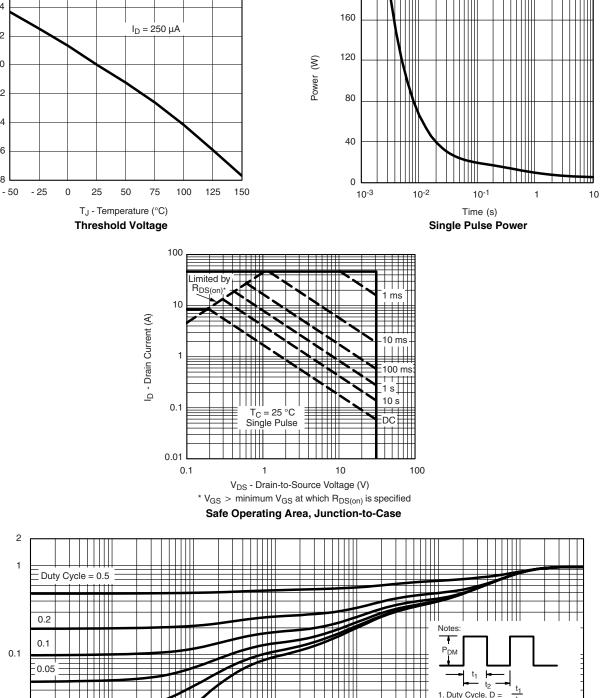
- 0.2

- 0.4

- 0.6

- 0.8





1. Duty Cycle, D = 1. Duty Cycle, D =  $\frac{t_2}{t_2}$ 2. Per Unit Base = R<sub>thJA</sub> = 125 °C/W 0.02 Tt 3.  $T_{JM}$  -  $T_A = P_{DM}Z_{thJA}^{(t)}$ Single Pulse 4. Surface Mounted 0.01 10-4 10<sup>-3</sup> 10-10<sup>-1</sup> 1 10 100 600 Square Wave Pulse Duration (s) Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Effective Transient Thermal Impedance

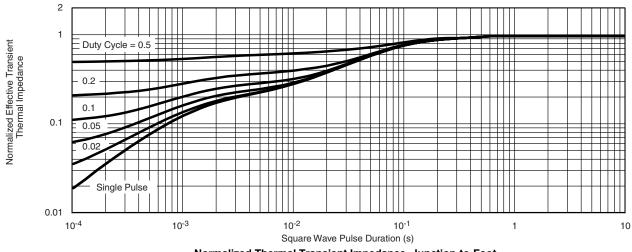




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#### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?72165">www.vishay.com/ppg?72165</a>.



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