Synchronous Buck Controller with 2-Bit VID Inputs to Select Among User Programmable Output Voltages

NCP81269

NCP81269 is a synchronous buck controller that is optimized for converting the battery voltage or adaptor voltage into power supply rails required in notebook and desktop system. NCP81269 is designed for applications requiring dynamically selected slew−rate controlled output voltages. The soft−start is programmed by a single capacitor. Voltage identification logic−inputs select among 0 V and three other voltages which are programmed via external resistors. NCP81269 supports high efficiency, fast transient response and provides power good signal. ON Semiconductor proprietary adaptive−ripple control enables seamless transition from CCM to DCM, where converter runs at reduced switching frequency with much higher efficiency. The part operates with input voltage ranging from 3.3 V to 24 V. NCP81269 is available in a 20−pin 3 mm x 3 mm QFN package.

Features

- Wide Input Voltage Range: from 3.3 V to 24 V
- Three Selectable Fixed Frequency 300 kHz, 400 kHz or 600 kHz
- 2−Bit VID Selects Among 0 V and Three User Programmed Voltages
- ±1.0% System Accuracy
- Differential Remote Output Voltage Sensing
- Soft Transient Control Reduces Inrush Current and Audio Noise
- Build−in Power−Good Masking Supports Voltage Identification (VID) On−The−Fly Transients
- Simple Resistor Programming Voltage Levels
- Programmable Soft−Start through a Single Capacitor
- User Programmable Load Line Option
- Automatic Power−Saving Mode
- Input Supply Voltage Feed Forward Control
- Resistive or Lossless Inductor's DCR Current Sensing
- Over−Temperature Protection
- Built−in Adaptive Gate Drivers
- Output Discharge Operation
- Built−in Over−Voltage, Under−Voltage and Over−Current Protection and Power Good Output
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Notebooks, Desktops & Servers
- I/O Supplies
- System Power Supplies
- Graphic Cards

ON Semiconductor®

www.onsemi.com

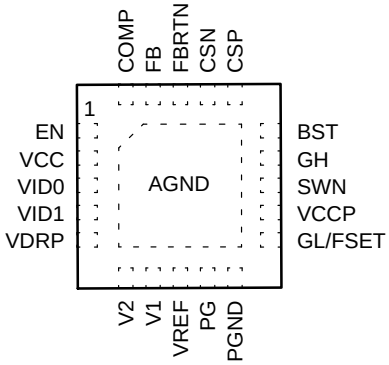
20 PIN QFN, 3x3
MN SUFFIX
CASE 485BC

MARKING DIAGRAM

81269	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81269MNTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

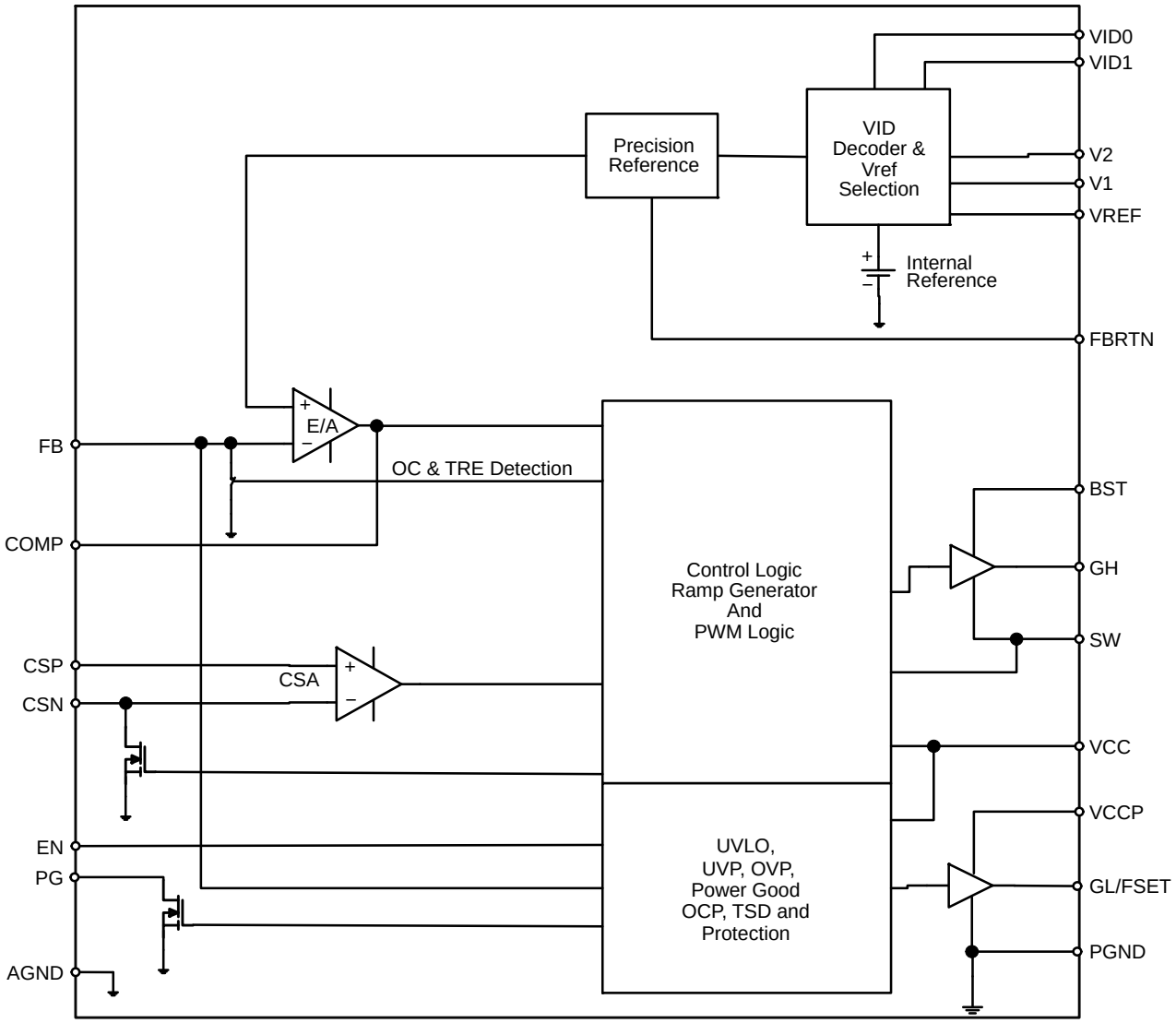


Figure 1. Block Diagram

Table 1. PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	EN	Logic control for enabling the switcher. Applying greater than 1.4 V will turn on the part. Connect to GND to disable.
2	VCC	Supply for analog circuit.
3	VID0	Logic input for reference voltage selector. Use in conjunction with the VID1 pin to select among four set−point reference voltages.
4	VID1	Logic input for reference voltage selector. Use in conjunction with the VID0 pin to select among four set−point reference voltages.
5	VDRP	Reserved for loadline programming. A resistor between VDRP and FB pins programs output voltage loadline.
6	V2	Voltage set−point programming resistor input.
7	V1	Voltage set−point programming resistor input.
8	VREF	Soft−start programming capacitor input. Set-point reference voltage programming resistor input. Connects internally to the inverting input of the VSET voltage set-point amplifier.
9	PG	Power good indicator of the output voltage. Open−drain output.
10	PGND	Ground reference and high−current return path for the bottom gate driver.
11	GL/FSET	Gate driver output of bottom N−channel MOSFET. And it is also used to set up switching frequency by connecting a resistor from this pin to ground.
12	VCCP	Power supply for MOSFET gate drive
13	SWN	Switch node between the top MOSFET and bottom MOSFET.
14	GH	Gate driver output of the top N−channel MOSFET.
15	BST	Top gate driver input supply, a bootstrap capacitor connection between SWN and this pin.
16	CSP	Inductor current differential sense non−inverting input.
17	CSN	Inductor current differential sense inverting input. It also discharges VOUT during soft−stop.
18	FBRTN	Feedback Return Input/Output. This pin remotely senses the output voltage. It is also used as the ground return for the VID reference voltage and the voltage error amplifier blocks.
19	FB	Output voltage feed back.
20	COMP	Output of the error amplifier.
	AGND	Analog ground. Bottom thermal pad.

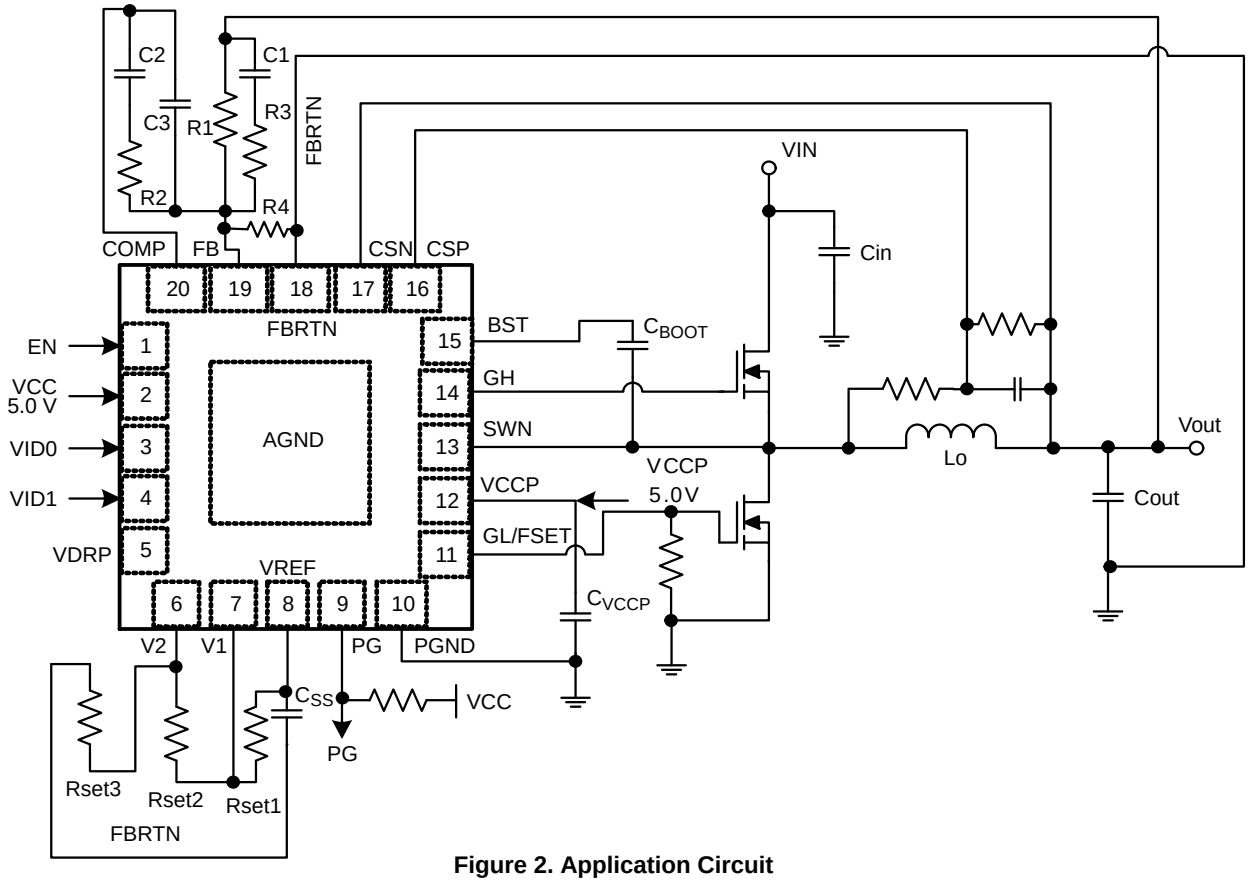


Figure 2. Application Circuit

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Value
VCC to AGND	−0.3 V (DC) to 6.5 V
FBRTN, PGND	−0.3 V to +0.3 V
SWN to PGND	−5.0 V to 30 V, −10.0 V for T < 100 ns
BST to GND	−0.3 V to 34 V
BST to SWN, BST to GH, VCCP to PGND	−0.3 V to 6.5 V
GL to PGND	−0.3 V to Min (VCCP + 0.3 V, 6.5 V)
GH to SWN	−0.3 V to BST + 0.3 V
All other pins	−0.3 V to Min (VCC + 0.3 V, 6.5 V)
Operating Temperature Range, T_A	−40°C to +125°C
Junction Temperature, T_J	−40°C to +125°C
Storage Temperature Range, T_S	−55°C to +150°C
Package Characteristic Thermal Resistance from Junction−to−Ambient (T_A = +25°C), R_{thja}	35 °C/W (Note 1)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This data is for solder on 4−layer board with 2 oz. copper.

Table 3. ELECTRICAL CHARACTERISTICS
(V_{CC} = V_{CCP} = 5.0 V, V_{out} = 1.0 V, T_A = +25°C for typical value; −40°C < T_A = T_J < 125°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
POWER SUPPLY						
VCC Operation Voltage	V_{CC}		4.5	5	5.5	V
VCCP Operation Voltage	V_{CCP}		4.5	5	5.5	V
VOLTAGE MONITORING & PROTECTION						
VCC Start Threshold			3.9	4.2	4.45	V
VCC UVLO Hysteresis			320	365	420	mV
Power Good Low Voltage		$I_{PG(sink)}$ = 4 mA		230	340	mV
Power Good High Leakage Current					1.0	μA
Power Good Startup Delay (Note 2)		Measure from SSEND to PG pos edge		3.8		ms
Power Good Propagation Delay		Delay for power good in		3.4		ms
		Delay for power good out		0.35		μs
Power Good Threshold		Power Good in from high	105	110	115	%
		Power Good in from low	91	95	99	%
		PG hysteresis		15		%
Power Good Masking Time		Triggered by any VID Change		425		μs
FB Overvoltage Threshold	V_{OVFB}−VID	Relative to nominal VID Voltage	250	300	350	mV
Overvoltage Propagation Delay				2.0		μs
FB Over Voltage Threshold During Soft−Start (Note 2)				2.0		V
FB Under−Voltage Trip Threshold	V_{UVFB}−VID	Relative to nominal VID Voltage	−360	−300	−240	mV
Undervoltage Protection Blanking Time				3		μs
SUPPLY CURRENT						
VCC Quiescent Current	I_{VCC}	V_{FB} = 1.5 V, EN = 5.0 (No Switching), GH and GL are open		4.0	5.5	mA
VCC Quiescent Current at zero VID	I_{VCC_00}	EN = 5 V, VID0 = VID1 = 0 V		520	800	μA
VCC Shutdown Supply Current	I_{VCC_SD}	EN = 0 V			3.4	μA
VCCP Quiescent Current	I_{VCCP}	V_{FB} = 1.5 V, EN = 5.0 (No Switching), GH and GL are open			0.3	mA
VCCP Quiescent Current at zero VID	I_{VCCP_00}	EN = 5 V, VID0 = VID1 = 0 V		0.5	1	μA
VCCP Shutdown Supply Current	I_{VCCP_SD}	EN = 0 V			0.3	μA
BST Quiescent Current	I_{BST}	V_{FB} = 1.5 V, EN = 5.0 (No Switching), GH and GL are open			0.33	mA
BST Shutdown Supply Current	I_{BST_SD}	EN = 0, BST = 5 V, SWN = 0			1	μA
FEEDBACK VOLTAGE						
Reference Voltage	V_{REF}			0.65		V
System Accuracy		VID0 = VID1 = High, PWM in CCM mode, −40°C < T_A < 100°C	−1.0		+1.0	%
		T_A = 25°C	−0.35		+0.35	%
Feedback Voltage Line Regulation		Vcc = 4.5 V ~ 5.5 V			0.8	%/V

2. Guaranteed by characterization or design, not production tested

Table 3. ELECTRICAL CHARACTERISTICS
(V_{CC} = V_{CCP} = 5.0 V, V_{out} = 1.0 V, T_A = +25°C for typical value; −40°C < T_A = T_J < 125°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VOLTAGE ERROR AMPLIFIER						
Open Loop DC Gain (Note 2)			80			dB
Open Loop Unity Gain Bandwidth (Note 2)	$F_{0dB,EA}$			20		MHz
FB Input Voltage Range (Note 2)			0		2.0	V
FB Bias Current (Note 2)		Relative to CSN = VID	−1		1	μA
Slew Rate (Note 2)		COMP pin to GND = 10 pF		10		V/μs
Maximum Output Voltage		10 mV of overdrive, I_{SOURCE} = 2.0 mA		V_{CC}		
Minimum Output Voltage		10 mV of overdrive, I_{SINK} = 2.0 mA		0.2	0.3	V
Output Source Current		10 mV of overdrive, V_{out} = 3.5 V	2			mA
Output Sink Current		10 mV of overdrive, V_{out} = 1.0 V	2			mA
DIFFERENTIAL CURRENT SENSE AMPLIFIER						
CSP and CSN Common−mode Input Voltage Range		Refer to AGND	−0.2		2.0	V
Differential Input Voltage Range			−30		30	mV
OVER CURRENT PROTECTION						
OCP Threshold		V(CSP)−V(CSN), Vo = 0.5 V ~ 1.5 V	25	30	35	mV
LOADLINE						
Loadline Signal Amplification		$(V_{VDRP} - V_{VREF}) / (V_{CSP} - V_{CSN})$		6		−
2_BITS VID						
VID0, VID1 High Threshold Voltage			0.65			V
VID0, VID1 Low Threshold Voltage					0.34	V
VID0, VID1 Input Bias Current		VID = 0 V		1		nA
VID0, VID1 Pull Down Current				2.5		μA
VID Delay time (Note 2)		Any VID edge to 10% of FB change	200			ns
EN						
EN High Threshold Voltage			1.4			V
EN Low Threshold Voltage					0.4	V
EN Input Bias Current	I_{EN}	EN = 5 V			1.0	μA
EN Input Voltage					5.5	V
PWM						
Minimum Controllable ON Time (Note 2)				35		ns
Minimum OFF Time (Note 2)			300	400	500	ns
PWM Ramp Amplitude (Note 2)		V_{IN} = 5 V		1.25		V
		V_{IN} = 12 V		3		V

2. Guaranteed by characterization or design, not production tested

Table 3. ELECTRICAL CHARACTERISTICS
(V_{CC} = V_{CCP} = 5.0 V, V_{out} = 1.0 V, T_A = +25°C for typical value; −40°C < T_A = T_J < 125°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
INTERNAL BST DIODE						
Forward Voltage Drop		I_F = 10 mA, T_A = 25°C		0.5		V
Forward Voltage Drop		I_F = 100 μA, T_A = 25°C		0.3		V
Reverse−bias Leakage Current		V_{BST} = 34 V, V_{SW} = 28 V, T_A = 25°C		0.1	1	μA
SOFT STOP						
Output Discharge On−Resistance		EN = 0, V_{out} = 0.65 V		14	30	Ω
SOFT START						
Soft Start Current	I_{SA1}			20		μA
SOFT TRANSIENT						
Soft Transient Source Current out of V_{REF} pin	I_{SA2+}	V_{REF} = 0.5 V	75	83	90	μA
Soft Transient Sink Current into V_{REF} pin	$I_{SA2−}$	V_{REF} = 2 V	60	80	105	μA
OSCILLATOR AND FREQUENCY DETECTION						
Oscillator Freq.	F_{SW}	R_{set} = 2K	270	300	330	KHz
Oscillator Freq. Accuracy					±10	%
Oscillator Freq. Detection Current	I_{FDECT}			50		μA
Oscillator Freq. Detection Time	t_{FDECT}			200		μs
Freq. Dect Threshold 300 kHz (Note 2)	$V_{FD300kHz}$				150	mV
Freq. Dect Threshold 400 kHz (Note 2)	$V_{FD400kHz}$		250		350	mV
Freq. Dect Threshold 600 kHz (Note 2)	$V_{FD600kHz}$		450			mV
GATE DRIVER						
GH Pull−High Resistance	RH_GH	Source, V(BST−GH) = 0.1		1.3	2.2	Ω
GH Pull−Low Resistance	RL_GH	Sink, V(GH−SWN) = 0.1 V		1.1	1.5	Ω
GL Pull−High Resistance	RH_GL	Source, V(VCC−GL) = 0.1 V		1.1	2.2	Ω
GL Pull−Low Resistance	RL_GL	Sink, V(GL−PGND) = 0.1 V		0.5	0.9	Ω
GH Source Current (Note 2)				2		A
GH Sink Current (Note 2)				2		A
GL Source Current (Note 2)				2		A
GL Sink Current (Note 2)				4		A
Dead Time		GL off to GH on	8	20	30	ns
		GH off to GL on	9	20	30	
THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 2)				150		°C
Thermal Shutdown Hysteresis (Note 2)				25		°C

2. Guaranteed by characterization or design, not production tested

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DETAILED DESCRIPTION

Overview

NCP81269 is designed for applications requiring dynamically selected slew−rate controlled output voltages. It provides a synchronous PWM controller that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. The NCP81269 PWM controller employs adaptive ripple control to provide seamless transition between CCM and DCM while maintain high efficiency during light load. It also provides fast transient response and excellent stability. The features of the NCP81269 include a 2 bits VID selectable and external programmable reference, fixed three preset switching frequency, an error amplifier, adaptive gate driver, programmable soft−start, and very low shutdown current. The protection features of the NCP81269 include over−current protection, power good monitor, over voltage and under voltage protection, built in output discharge and thermal shutdown.

Reference Voltage Programming

The NCP81269 incorporates 2−bits VID, which selects four user−programmed reference voltages that reflect on Vref pin. NCP81269 measures VFB and VREF pin voltage relative to FBRTN pin. An internal reference that allows output voltages as low as 0.65 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents. The VID truth tables for each part are listed below.

Table 4. NCP81269 VID TRUTH TABLE

VID STATE		RESULTS		
VID1	VID0	CLOSE	V_{REF}	V_{OUT}
0	0		0 V	0 V
0	1	SW0	Vset0	V_{OUT1}
1	0	SW1	Vset1	V_{OUT2}
1	1	SW2	Vset2	V_{OUT3}

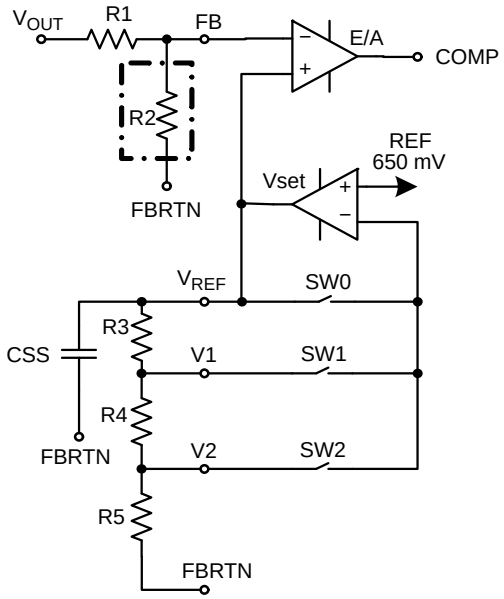


Figure 3.

External Reference Voltage and Output Voltage Setting

Vset0, Vset1, Vset2 and Vset3 can be calculated based on the following equations:

$$V_{set0} = V_{INREF}$$

$$V_{set1} = V_{INREF} \cdot \left(1 + \frac{R_3}{R_4 + R_5}\right)$$

$$V_{set2} = V_{INREF} \cdot \left(1 + \frac{R_3 + R_4}{R_5}\right)$$

And $V_{set2} > V_{set1} > V_{set0}$

Vset0, Vset1 and Vset2 are in the range of 0.65 V~1.5 V. If the required output voltage is higher than 0.65 V~1.5 V, a feedback voltage divider (a resistor R2 is added from FB pin to FBRTN) can be used to boost the output voltage up. So the output voltage can be calculated based on the following equations:

$$V_{OUT1} = V_{set0} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT2} = V_{set1} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$V_{OUT3} = V_{set2} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

And $V_{OUT3} > V_{OUT2} > V_{OUT1}$

Differential Sensing of Output Voltage

The NCP81269 combines differential sensing with a high accuracy VID DAC, referenced by a precision band gap source and a low offset error amplifier, to provide accurate output voltage. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the positive regulation point. FBRTN should be connected directly to the negative remote sensing point.

External Soft−Start and VID Change Slew Rate

To limit the start−up inrush current, a capacitor can be connected from Vref pin to ground to ramp up reference voltage slowly. During this period, the set amplifier output 20 μA current to charge capacitor C_{SS}. The soft start period can be calculated by the following equation:

$$t_{SS} = -R_A \cdot C_{SS} \cdot LN\left(1 - \frac{V_O}{I_{SA1} \cdot R_A}\right)$$

Where:

- RA is the sum of the series resistors from VREF to ground. $R_A = R_3 + R_4 + R_5$
- I_{SA1} is soft start current 20 μA.
- Vo is the initial output voltage set by VID

The output current of the set amplifier will change to +83 μA /− 80 μA after soft start period. So during voltage steps due to VID bit change, the slew rate of output voltage can be calculated as follows:

$$t_{SL} = -R_A \cdot C_{SS} \cdot LN\left(1 - \frac{V_{O2} - V_{O1}}{I_{SA2} \cdot R_A}\right)$$

Where:

- I_{SA2} is the source/sink current limit of set amplifier during VID changing, which is 83/80 μA.
- VO1 and VO2 are the voltages selected by VID inputs

Since the CSS capacitance programs the VOUT slew rate during VID transient, please use a high tolerance type MLCC, such as X7R or NPO.

Output Decay to Zero

When both VID0 and VID1 pins input signals are changed to low, the NCP81269 decays the output voltage toward zero. Both GH and GL outputs are low, so that output voltage is discharged by load current.

Oscillator Frequency and Its Detection

A fixed precision oscillator is provided. The actual switching frequency is set at 300 KHz, 400 KHz or 600 KHz by the resistor on GL/FSET pin. The resistor and frequency can be referred to in the table below.

GL/FSET Resistor	2K	6K	15K
Switching Frequency	300 KHz	400 KHz	600 KHz

The recommended GL/FSET resistors above work with low−side MOSFETs whose total gate capacitance is 10 nF or less. For low−side MOSFETs whose total gate capacitance is over 10 nF, user needs to know the frequency detection details below.

After the NCP81269 is enabled, but before the soft−start ramp up, the oscillator frequency is detected on the GL/FSET pin. A 50 μA current I_{FDECT} is sourced out of the GL/FSET pin, and at the end of 200 μS detection time T_{FDECT}, the voltage on the GL/FSET is measured. Comparing the measured GL/FSET pin voltage against the frequency detection thresholds $V_{FD300kHz}$ and $V_{FD400kHz}$ and $V_{FD600kHz}$, the NCP81269 sets switching frequency 300 kHz, 400 kHz and 600 kHz respectively. When low−side MOSFET has more than 10 nF gate capacitance, it takes a relatively long time for the 50 μA I_{FDECT} current to charge up the GL/FSET pin. Therefore, the user needs to factor in the rising time of GL/FSET voltage, and make sure GL/FSET pin voltage rises into the desired frequency detection voltage range within 200 μs.

Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 15 MHz, with open loop gain of at least 80 dB. The COMP output voltage is clamped to a level above the oscillator ramp in order to improve large−scale transient response.

Soft Stop

Soft−Stop or discharge mode is always on during faults or disable. In this mode, a fault (UVP, OVP, OCP, TSD) or disable (EN) causes the output to be discharged through an internal 20−ohm transistor inside of the CSN Pin. The time constant of soft−stop is a function of output capacitance and the resistance of the discharge transistor.

Adaptive Non−Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET free-wheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP81269 implements adaptive dead time control to minimize the dead time, as well as preventing shoot through from happening.

Automatic Power Saving Mode

If the load current decreases, the converter will enter power save mode operation. During power save mode, the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintains high efficiency.

EN Pin Input Signal

When the EN pin voltage goes beyond VCC pin voltage, the NCP81269 may enter into test mode, which is reserved for factory usage, but not for customer application. Therefore, please always keep EN pin voltage below VCC pin voltage, such as using 3.3 V digital signal, or having resistor divider down from VCC pin voltage, or down from a 5.0 V digital signal.

PROTECTIONS

Under Voltage Lockout (UVLO)

There is under-voltage lock out protections (UVLO) for VCC in NCP81269, which has a typical trip threshold

voltage 4.2 V and trip hysteresis 300 mV. If UVLO is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

Over Voltage Protection (OVP)

When VFB voltage is 300 mV (typical) above V_{REF} voltage for over 2 µs blanking time, an OV fault is set. At that moment, the top gate driver is turned off and the bottom gate driver is turned on trying to discharge the output. The bottom gate driver will be turned off when VFB drops below under voltage threshold. EN resets or power recycle the device can exit the fault. OVP is disabled during VID changes and when V_{OUT} = 0 V.

Under Voltage Protection (UVP)

An UVP circuit monitors the VFB voltage to detect under voltage event. The under voltage limit is 300 mV (typical) below V_{REF} voltage. If the VFB voltage is below this threshold over 3.3 µs, an UV fault is set and the device is latched off such that both top and bottom gate drives are off. EN resets or power recycle the device can exit the fault. UVP is delayed for soft start after EN goes high. UVP is disabled during VID changes and when V_{OUT} = 0 V.

Power Good Monitor (PG)

NCP81269 provides window comparator to monitor the FB voltage. The target voltage window and transition delay times of the PGOOD comparator are ±5% (typ.) and 3.3−ms delay for assertion (low to high), and ±10% (typ) and 1.5−µs delay for de−assertion (high to low) during running. The PG pin is open drain 5−mA pull down output. During startup, PG stays low until the feedback voltage is within the specified range for about 3.3 ms. To prevent a false alarm; the power−good circuit is masked during any VID change. The duration of the PG mask is set to approximately 425 µs by an internal timer.

As indicated in Table 2 Absolute Maximum Ratings, PG pin cannot be pulled to a voltage higher than VCC pin voltage.

Over Current Protection (OCP)

The NCP81269 protects converter if over−current occurs. The current through inductor is continuously monitored with differential current sense. Current limit threshold Vth_OC between CS+ and CS− is internally fixed to 30 mV. The current limit can be programmed by inductor's DCR and current sensing resistor divider with Rs1 and Rs2.

The Rs1, Rs2 and C can be calculated as:

$$C \cdot \left(R_{S1} // R_{S2}\right) = \frac{L}{DCR}$$

The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{th\_DC}}{k \cdot DCR}, \text{where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} - \frac{V_O \cdot \left(V_{in} - V_O\right)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$

where Vin is the input supply voltage of the power stage, and fsw is normal switching frequency.

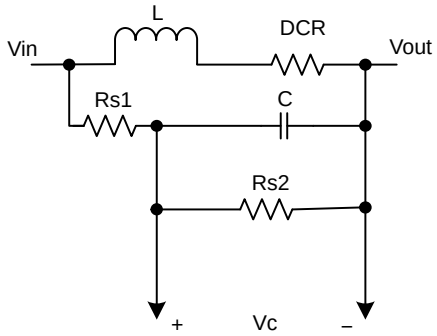


Figure 4. Inductor DCR Current Sensing Circuit

Figure 5 shows NTC resistor network to compensate the temperature drift of DCR.

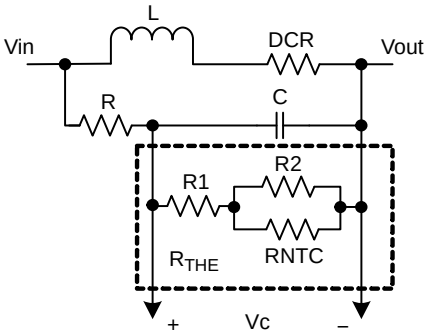


Figure 5. Inductor DCR Current Sensing Circuit with Temperature Compensation Network

If inductor current exceeds the current threshold, the high−side gate driver will be turned off cycle−by−cycle. In the mean time, an internal OC fault timer will be triggered. If the fault still exists after about 8 clock cycles, the part latches off, both the high−side MOSFET and the low−side MOSFET are turned off. The fault remains set until the system has shutdown and re−applied VCC and/or the enable signal EN is toggled.

User Programmable Loadline

NCP81269 allows user to program loadline via the VDRP pin. As illustrated in Figure 6, the NCP81269 outputs a differential signal between VDRP and VREF pins, with its amplitude six times as that of differential signal across CSP and CSN pins.

Consequently, user can program a loadline with a resistor, R_{DRP}, between VDRP pin and FB pin, as shown in the following equation. R_{S1} and R_{S2} are the resistors divider on CSP and CSN pins, as illustrated in Figure 4.

$$\text{Loadline} = 6 \times \frac{R_{FB}}{R_{DRP}} \times \frac{R_{S2}}{R_{S1} + R_{S2}} \times \text{DCR(inductor)}$$

When loadline feature is not needed, please simply leave the VDRP pin open.

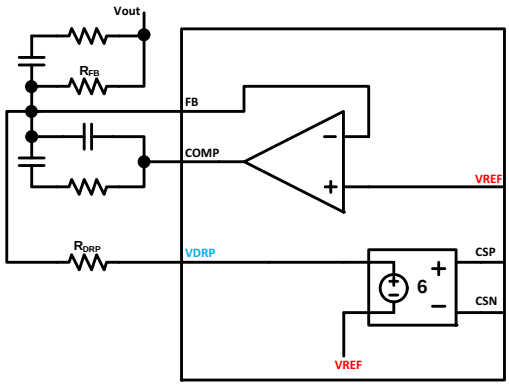


Figure 6. Programming Loadline

Pre−Bias Startup

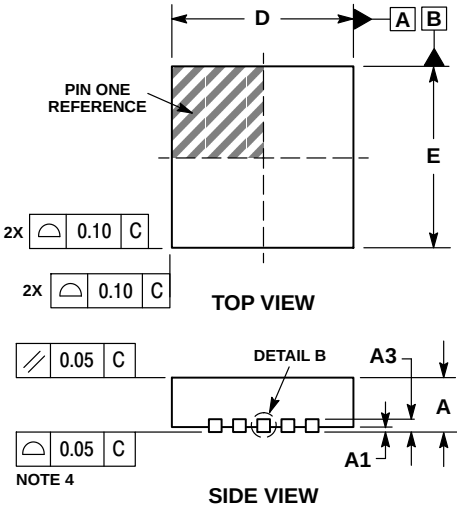
In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP81269 supports pre−bias start up by holding Low side FETs off till soft start ramp reaches the FB pin voltage. OCP is disabled when V_{OUT} = 0 V.

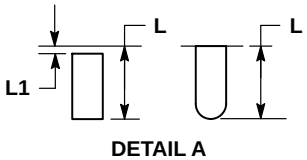
Thermal Shutdown

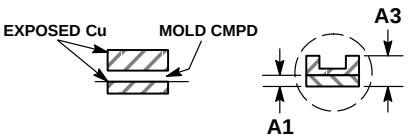
The NCP81269 protects itself from over heating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold, an internal resistor will discharge Vref and the voltage at the COMP pin will be pulled to GND, and both the upper and lower MOSFETs will be shut OFF. When temperature drops below threshold, the part will auto restart with soft− start feature.

PACKAGE DIMENSIONS

QFN20 3x3, 0.4P
CASE 485BC
ISSUE O

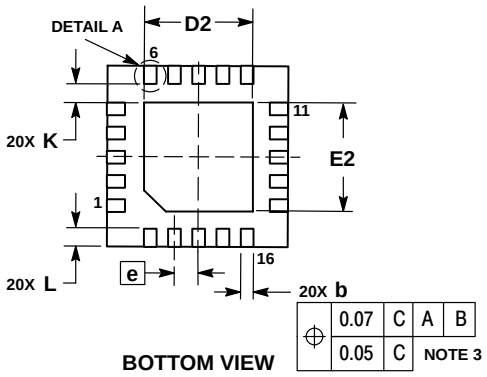




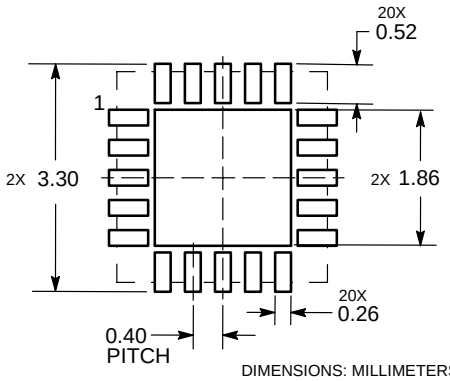


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	3.00 BSC	
D2	1.70	1.90
E	3.00 BSC	
E2	1.70	1.90
e	0.40 BSC	
K	0.30 REF	
L	0.20	0.40
L1	0.00	0.15



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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