LH5P8129

CMOS 1M (128K × 8)
CS-Control Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Single +5 V power supply
- Pin compatible with 1M standard SRAM
- Power consumption:
  Operating: 572/385/275 mW (MAX.)
  Standby (TTL level): 5.5 mW (MAX.)
  Standby (CMOS level): 1.1 mW (MAX.)
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)

DESCRIPTION

The LH5P8129 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while considering the pinout compatibility with industry standard SRAMs. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8129 PSRAM has a built-in oscillator, which makes it easy to refresh memories without external clocks.

PIN CONNECTIONS

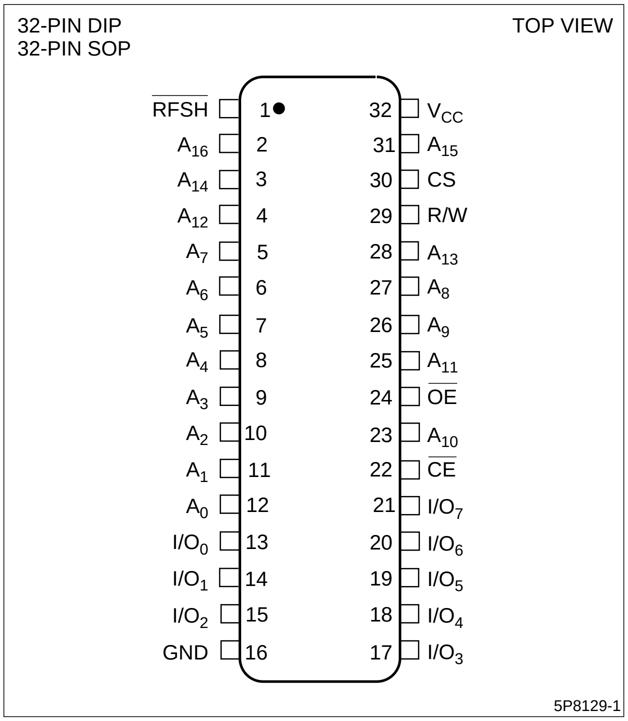
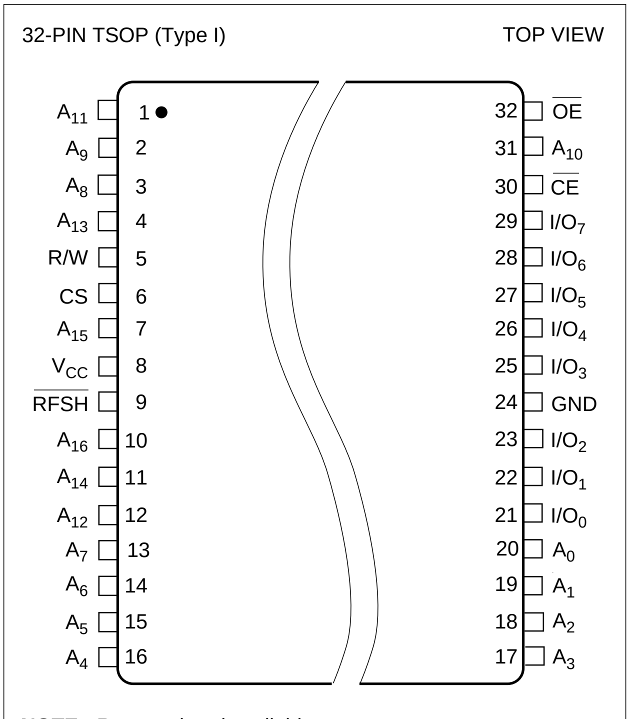


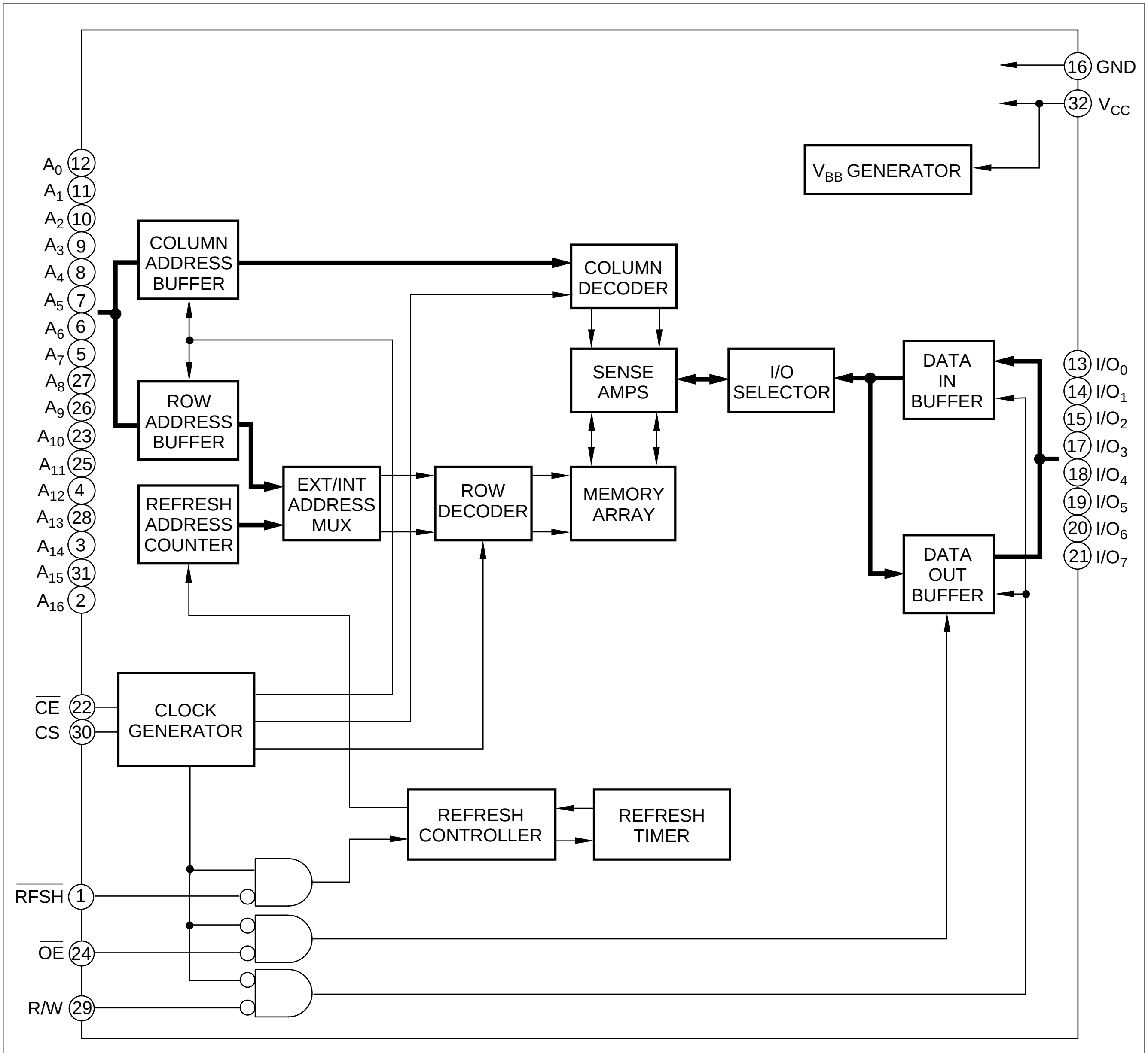
Figure 1. Pin Connections for DIP and SOP Packages



NOTE: Reverse bend available on request.

5P8129-2

Figure 2. Pin Connections for TSOP Package



NOTE: Pin numbers apply to 32-pin DIP or SOP.

Figure 3. LH5P8129 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{\text{OE}}$	Output Enable input
$\overline{\text{CE}}$	Chip Enable input

SIGNAL	PIN NAME
CS	Chip Select input
$\overline{\text{RFSH}}$	Refresh input
I/O_0 - I/O_7	Data input/output

TRUTH TABLE

$\overline{\mathrm{CE}}$	CS	$\overline{\mathrm{OE}}$	R/W	$\overline{\mathrm{RFSH}}$	A_0 - A_{16}	I/O_1 - I/O_8	MODE
L	H	L	H	X	VX	D_{OUT}	Read
L	H	X	L	X	VX	D_{IN}	Write
L	H	H	H	X	VY	High-Z	$\overline{\mathrm{CE}}$ only refresh
L	L	X	X	X	X	High-Z	CS standby
H	X	X	X	L	X	High-Z	Auto/Self refresh
H	X	X	X	H	X	High-Z	Standby

NOTES:

H = High at V_{IN} = V_{CC} + 0.3 V to V_{IH} (MIN.)

L = Low at V_{IN} = V_{IL} (MAX.) to -1.0 V

X = Don't care at V_{CC} + 0.3 V to -1.0 V

VX = A_0-A_{16} address input when $\overline{\mathrm{CE}}$ = L, then Don't Care

VY = A_0-A_8 address input when $\overline{\mathrm{CE}}$ = L, then Don't Care,
and A_9-A_{16} address = Don't Care at V_{CC} + 0.3 V to -1.0 V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1 MHz, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, OE	C_{IN2}		5	pF
	$\overline{\mathrm{CE}}$, CS	C_{IN3}		5	pF
	RFSH	C_{IN4}		5	pF
Input/output capacitance	I/O_1 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8129-60	I_{CC1}	$t_{RC} = t_{RC}$ (MIN.)		104	mA	1, 2
	LH5P8129-80				70		
	LH5P8129-10				50		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.2		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.2		1, 6
Input leakage current		I_{LI}	$0 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$ 0 V except on test pins	-10	10	µA	
I/O leakage current		I_{LO}	$0 \text{ V} \leq V_{OUT} \leq V_{CC} + 0.3 \text{ V}$ Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = -1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:

1. Specified values are with outputs open.
2. I_{CC1} depends on the cycle time
3. $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IH}$
4. $\overline{CE} = V_{CC} - 0.2$ V, $\overline{RFSH} = V_{CC} - 0.2$ V
5. $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IL}$
6. $\overline{CE} = V_{CC} - 0.2$ V, $\overline{RFSH} = 0.2$ V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	LH5P8129-60		LH5P8129-80		LH5P8129-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	165		195		235		ns	
CE pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
CE precharge time	t_P	40		40		50		ns	
CS setup time	t_{CSS}	0		0		0		ns	
CS hold time	t_{CSH}	15		20		25		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
CE access time	t_{CEA}		60		80		100	ns	5
OE access time	t_{OEA}		25		30		35	ns	5
CE to output in Low-Z	t_{CLZ}	20		20		20		ns	
OE to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
OE setup time	t_{OES}	0		0		0		ns	
OE hold time	t_{OEH}	10		10		10		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from CE	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from CE	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from CE	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
CE delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, an initial pause of 100 µs with CE = V_{IH}, RFSH = V_{IH} after power-up, followed by at least 8 dummy cycles.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Measured with a load equivalent to 2TTL + 100 pF.
5. Address is latched at the negative edge of CE.
6. Data is latched at the positive edge of R/W or at the positive edge of CE.

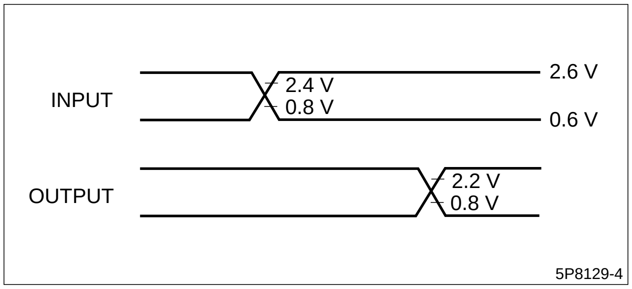


Figure 4. AC Characteristics

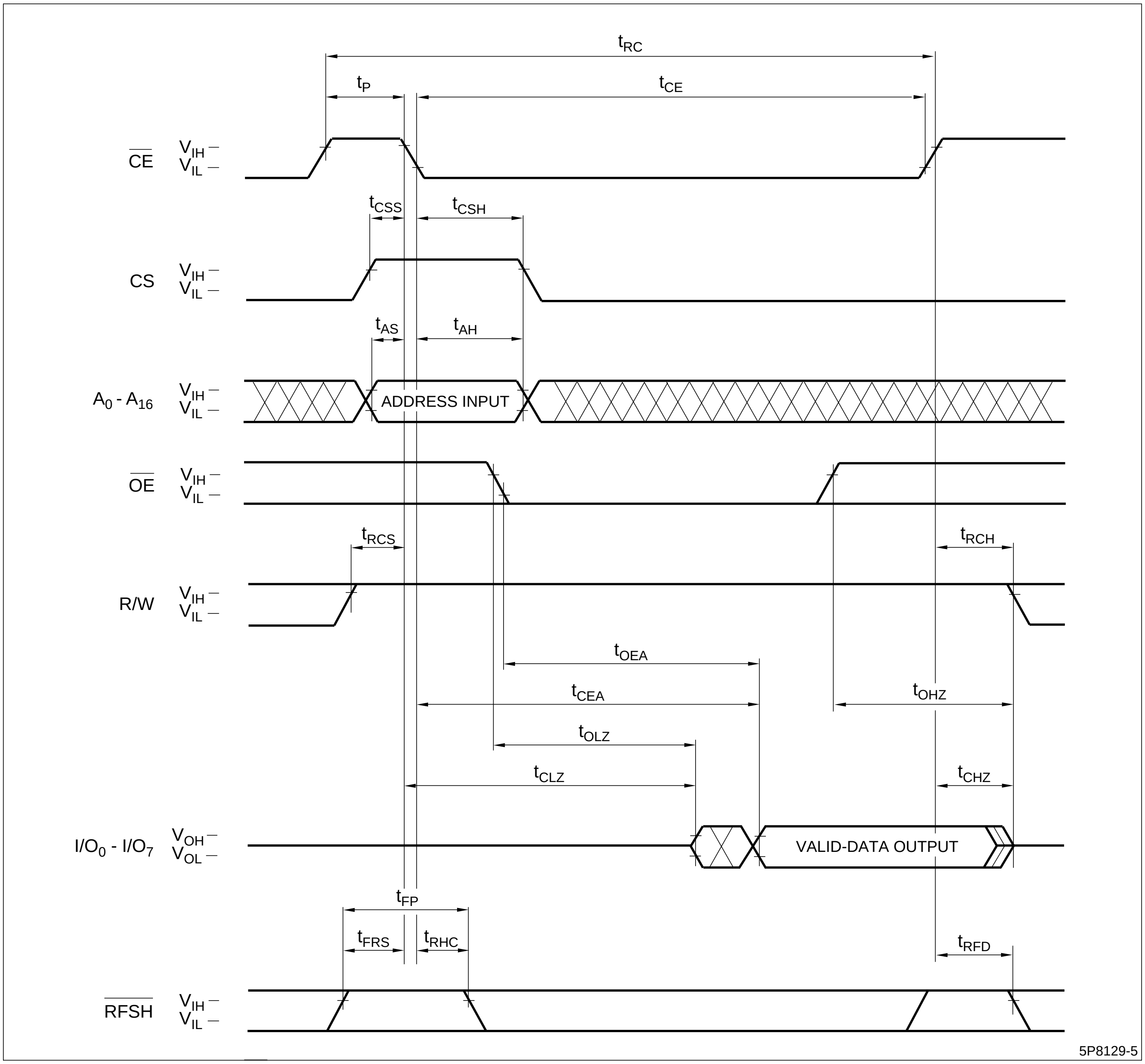


Figure 5. Read Cycle

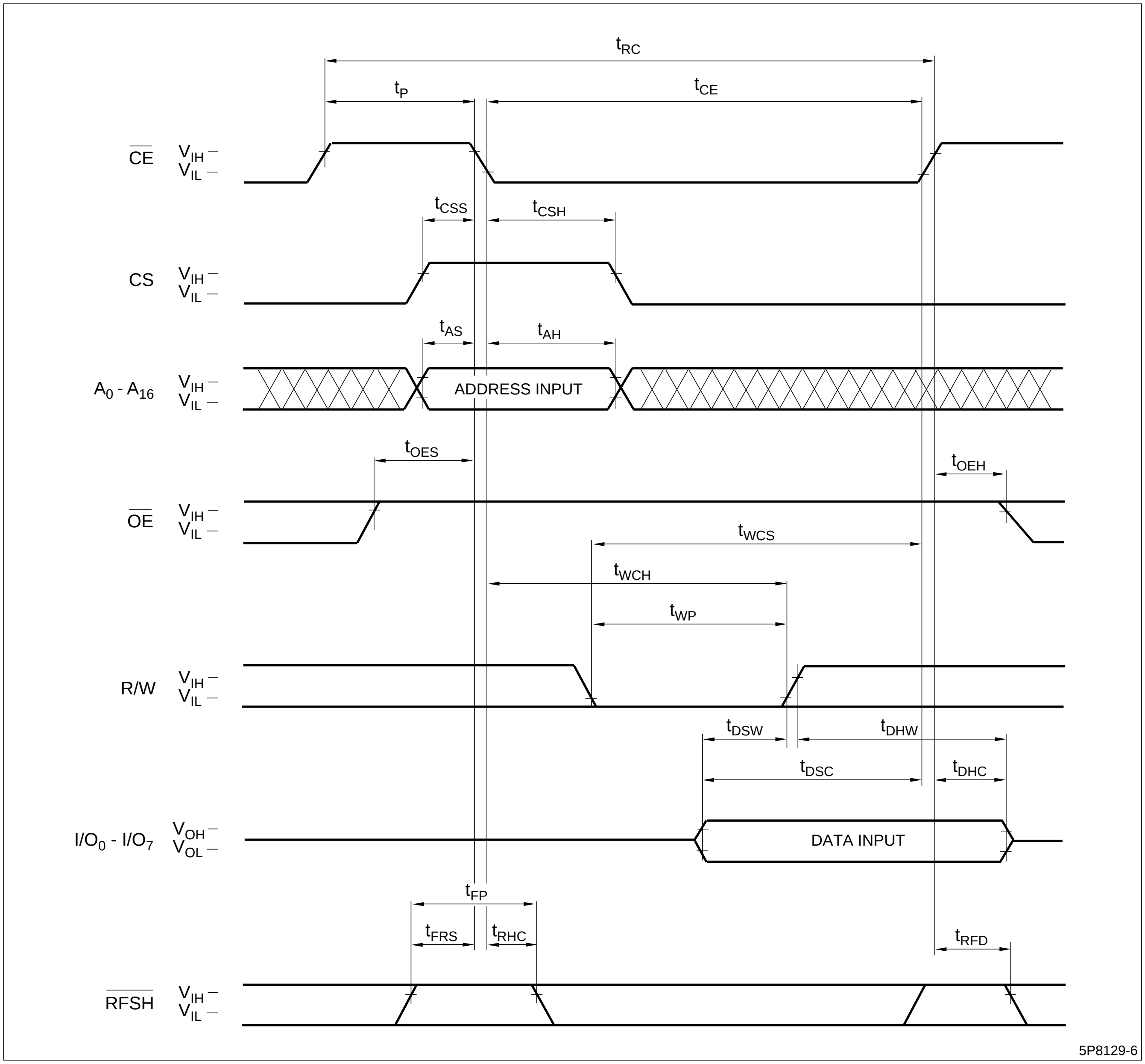


Figure 6. Write Cycle 1 ($\overline{OE}$ = HIGH)

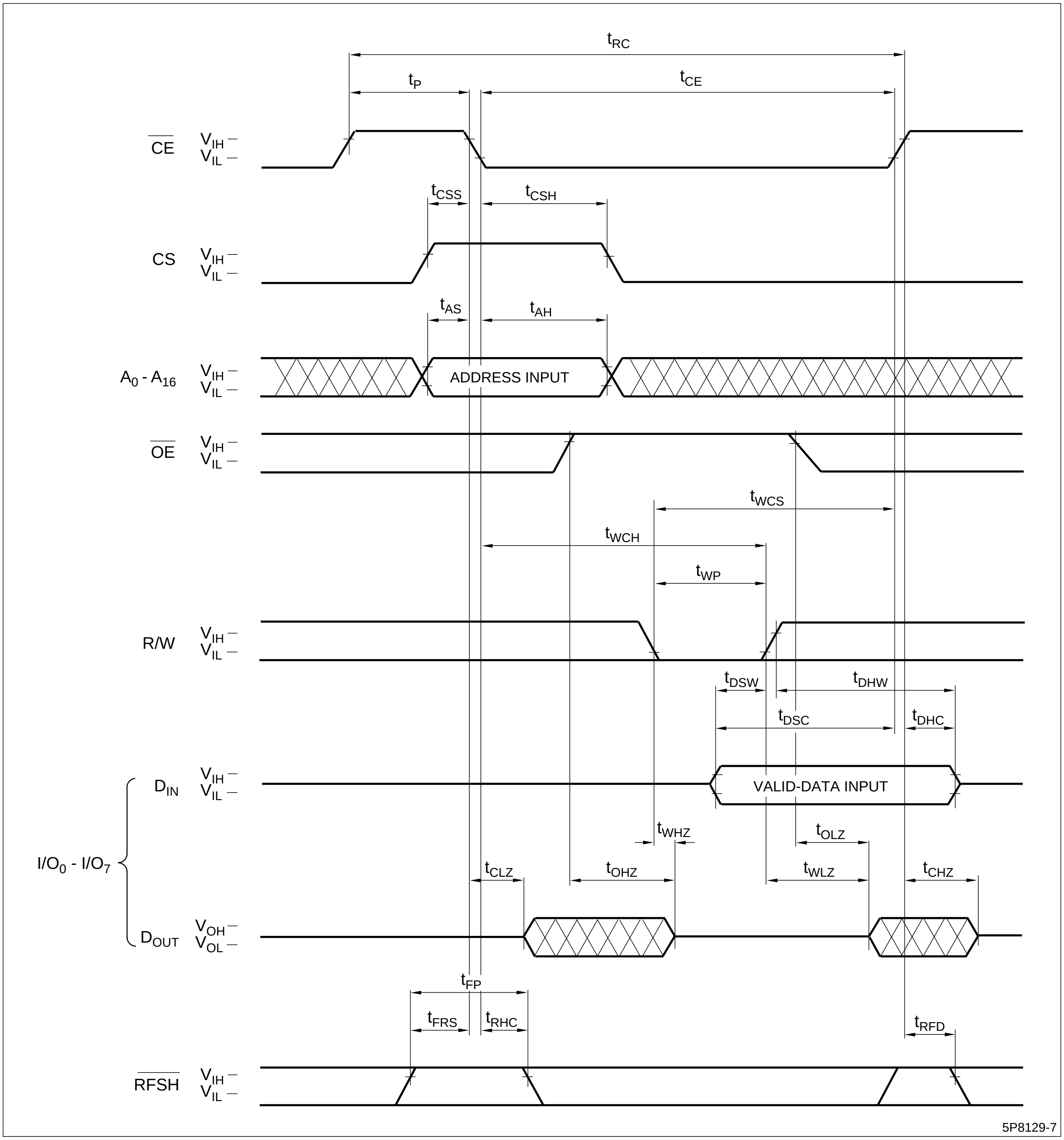


Figure 7. Write Cycle 2 (OE Clock)

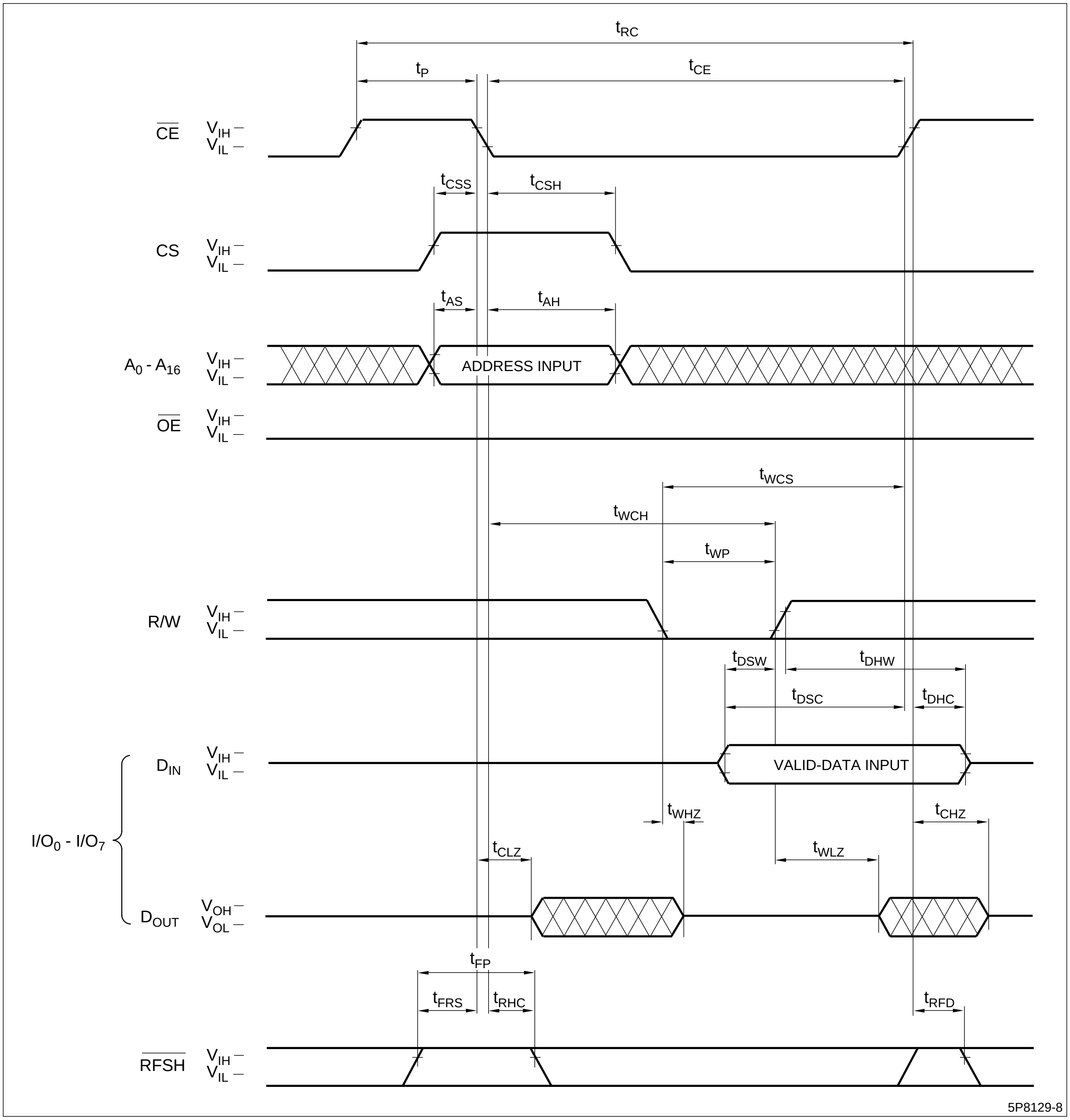


Figure 8. Write Cycle 3 (OE = LOW)

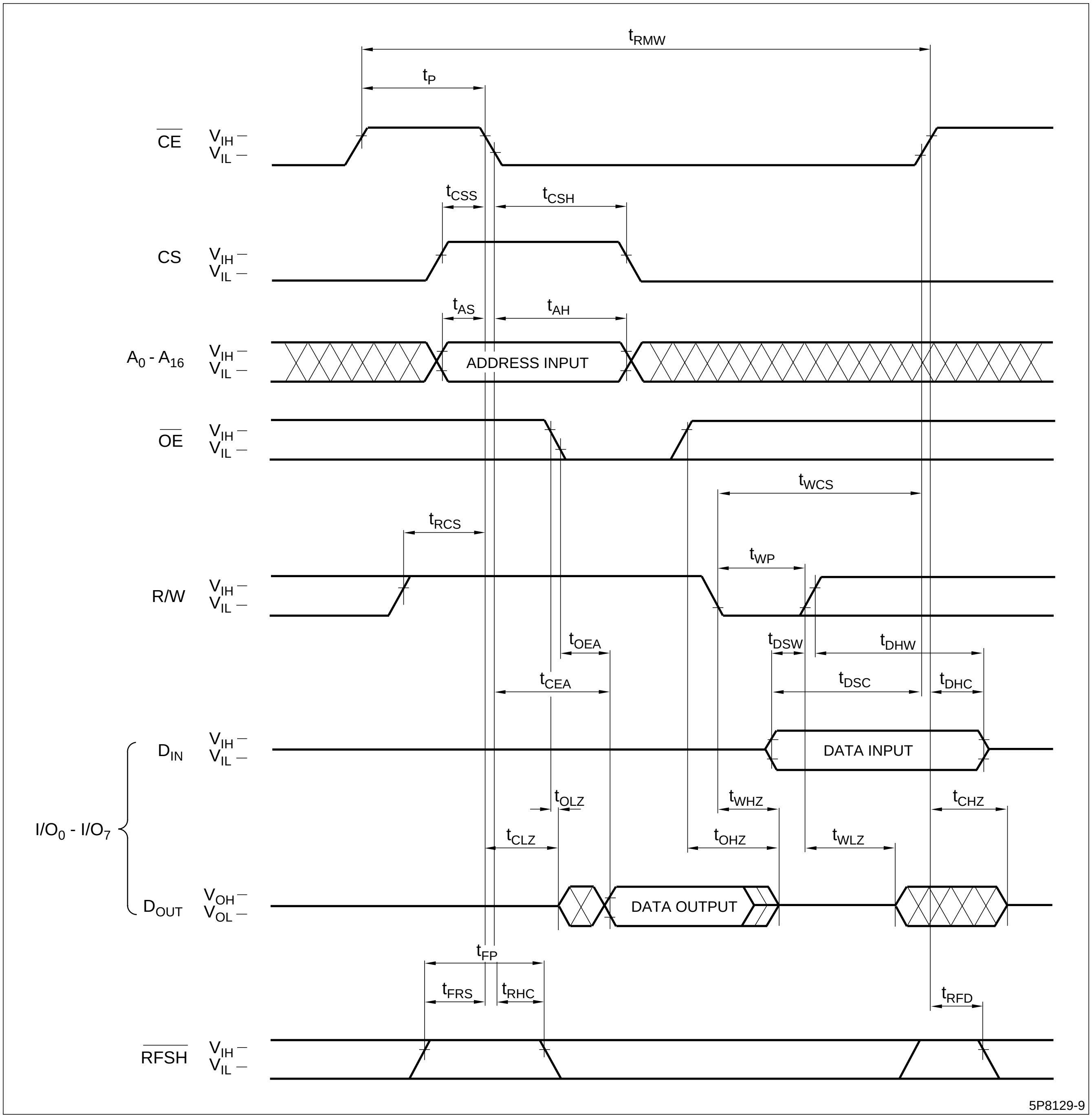
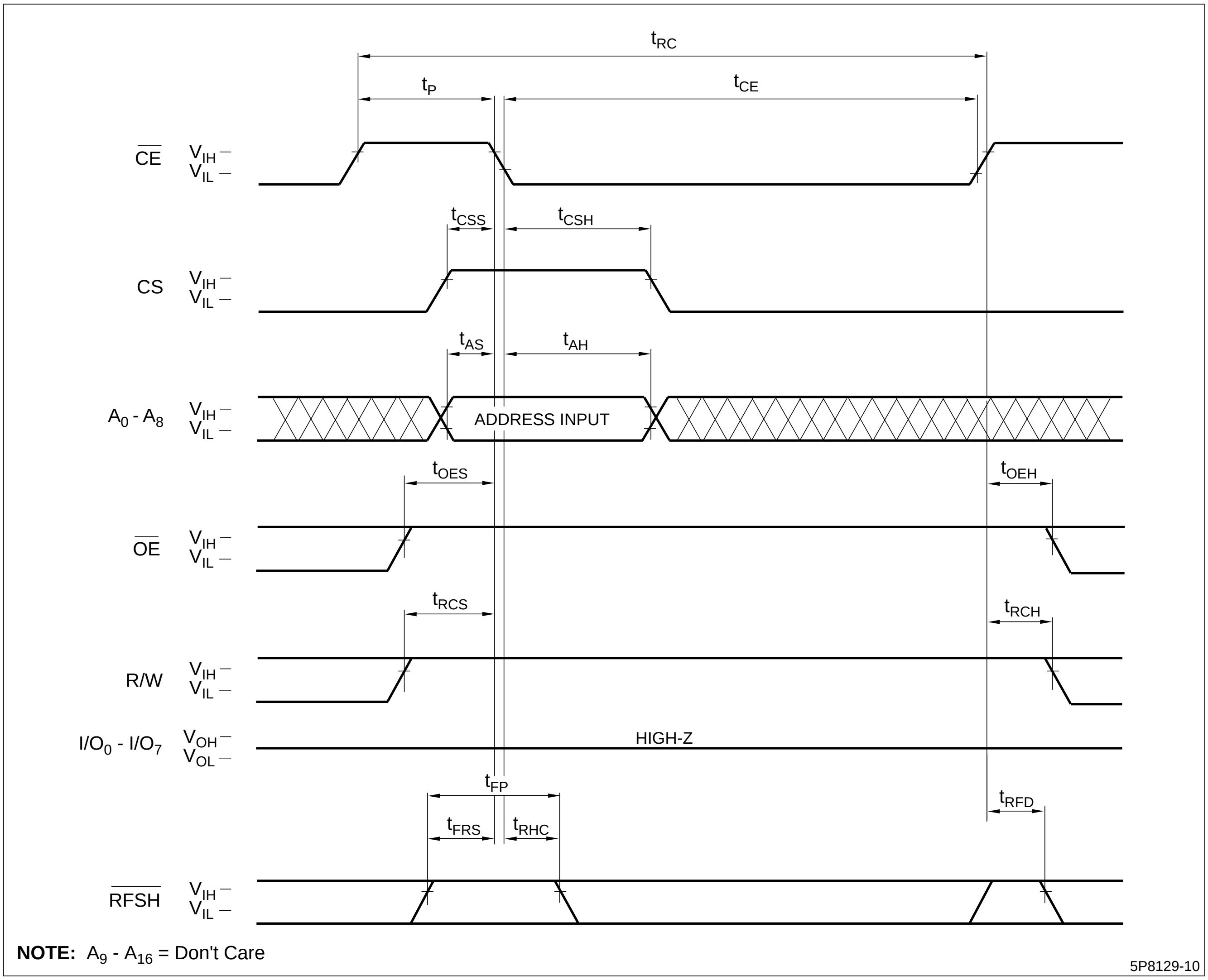
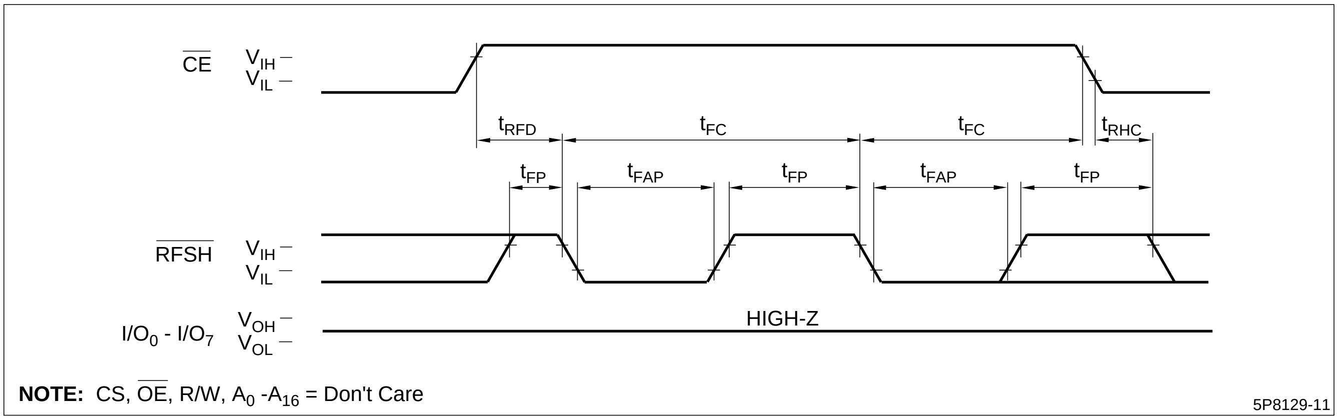


Figure 9. Read-Modify-Write Cycle



NOTE: A_9 - A_{16} = Don't Care

Figure 10. $\overline{\text{CE}}$ Only Refresh



NOTE: CS, $\overline{OE}$, R/W, A_0 -A_{16} = Don't Care

Figure 11. Auto Refresh Cycle

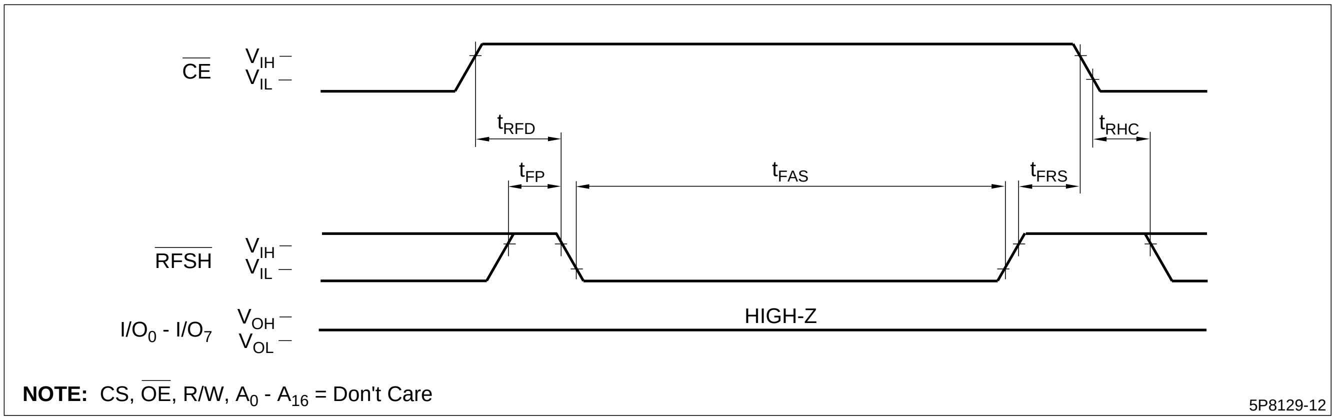


Figure 12. Self Refresh Cycle

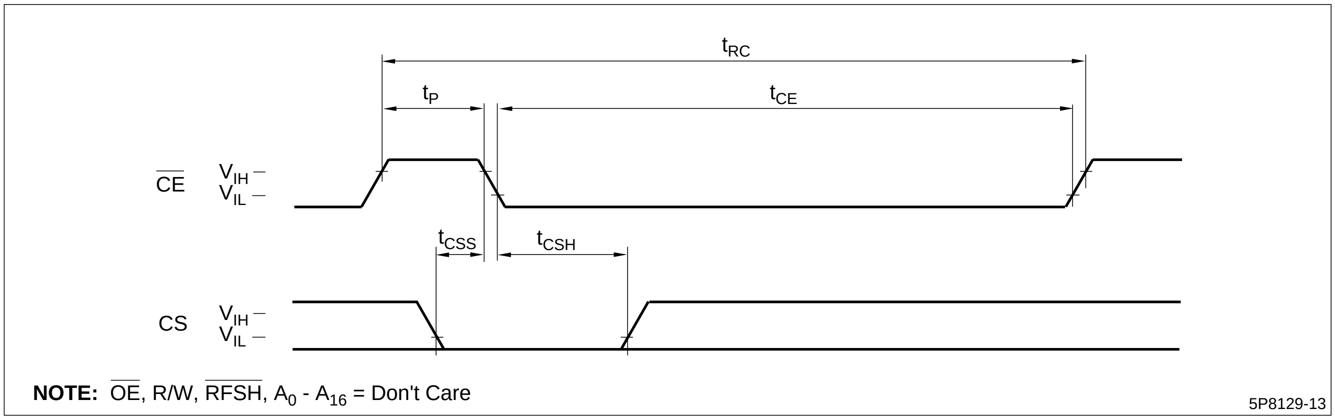
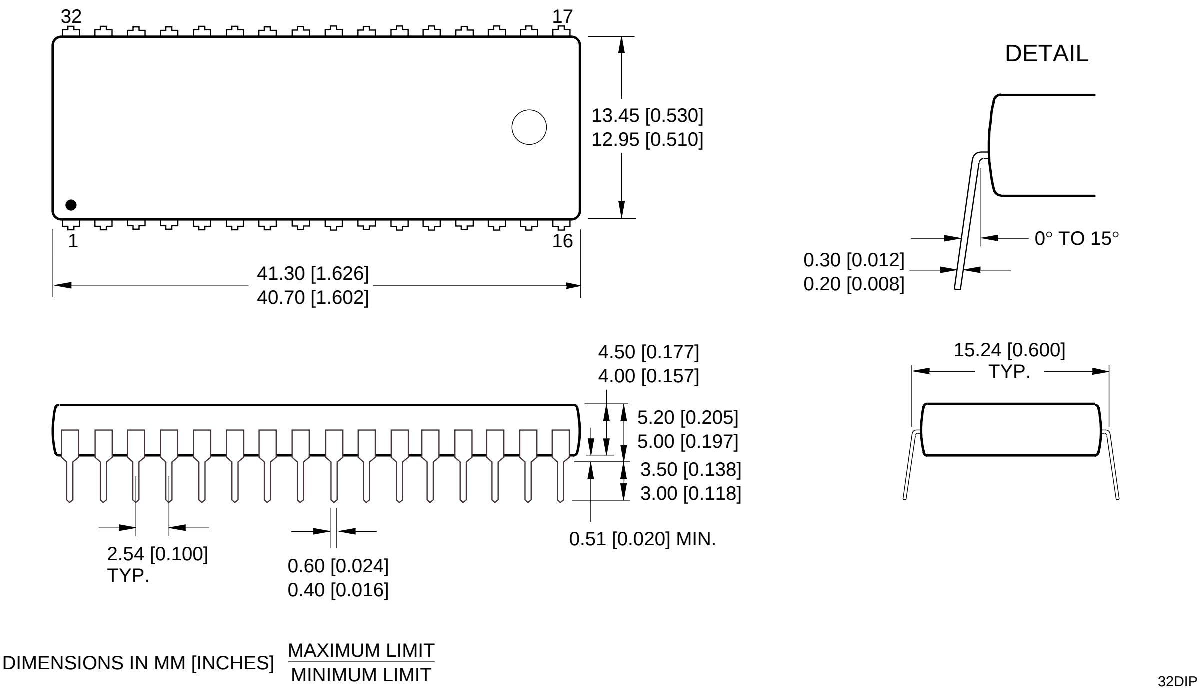


Figure 13. CS Standby Mode

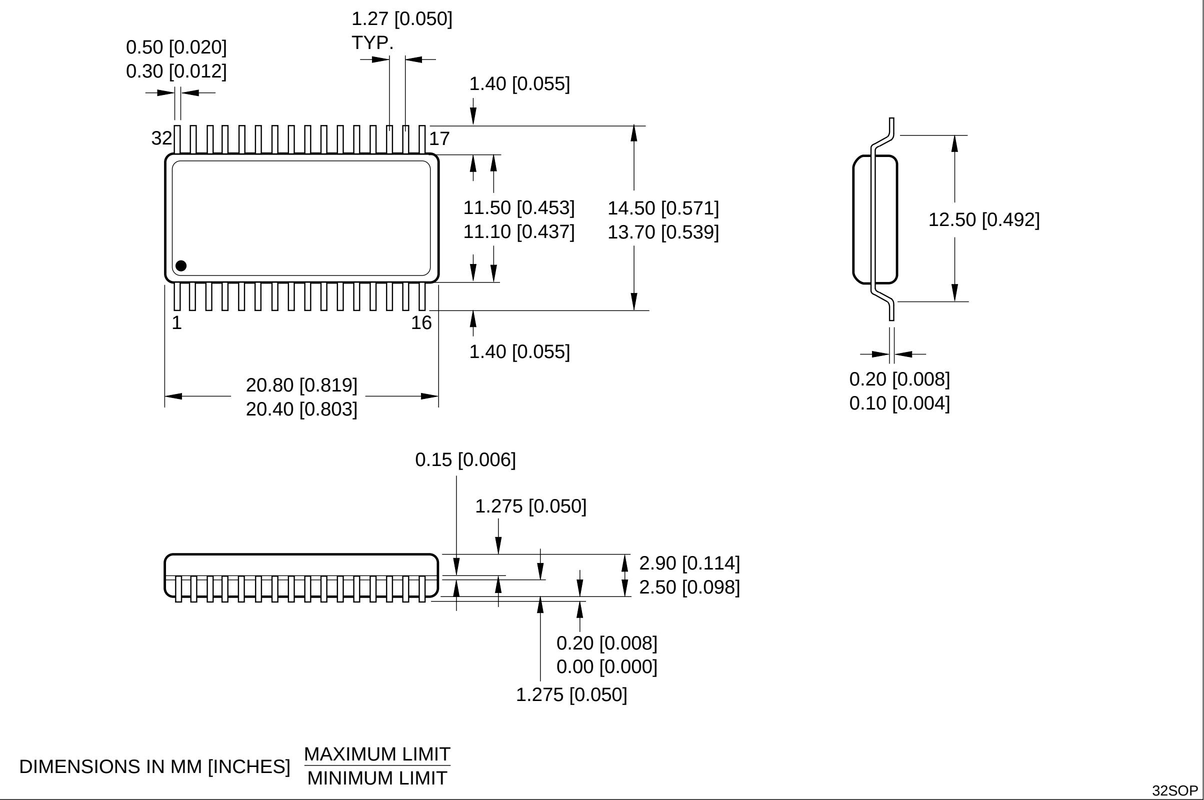
PACKAGE DIAGRAMS

32DIP (DIP032-P-0600)



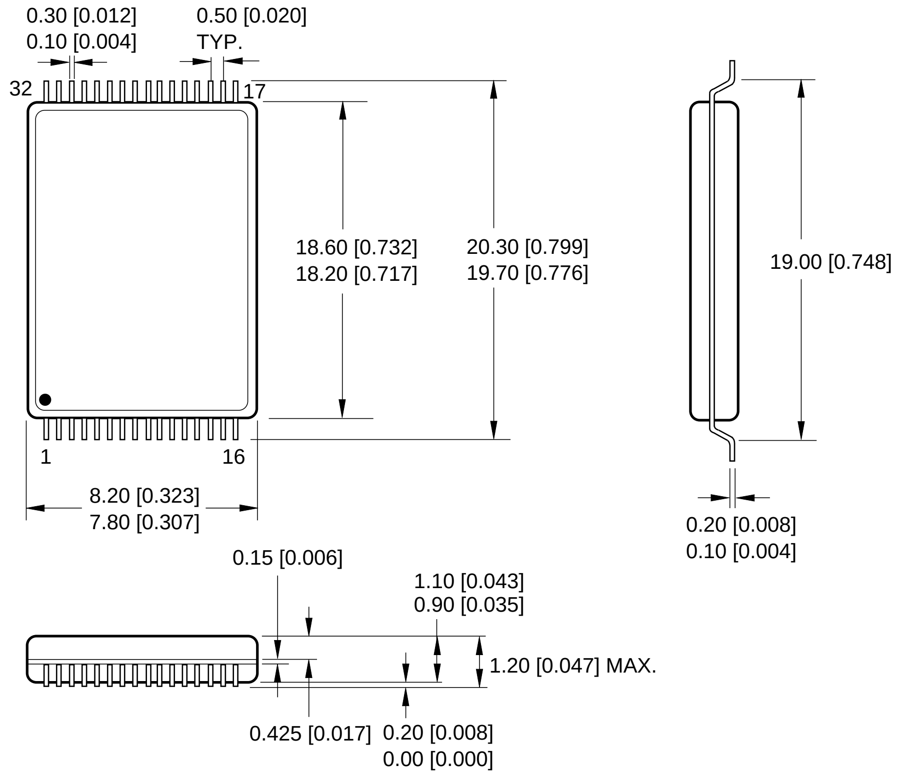
32-pin, 600-mil DIP

32SOP (SOP032-P-0525)



32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)



DIMENSIONS IN MM [INCHES] $\frac{\text{MAXIMUM LIMIT}}{\text{MINIMUM LIMIT}}$

32TSOP

32-pin, 8 × 20 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH5P8129 X - ##
Device Type Package Speed

- 60 60 Access Time (ns)
- 80 80
- 10 100

Package:

- Blank 32-pin, 600-mil DIP (DIP032-P-0600)
- N 32-pin, 525-mil SOP (SOP032-P-0525)
- T 32-pin, 8 x 20 mm^2 TSOP (Type I) (TSOP032-P-0820)
- TR 32-pin, 8 x 20 mm^2 TSOP (Type I) Reverse bend (TSOP032-P-0820)

Device Type: CMOS 1M (128K x 8) Pseudo-Static RAM

Example: LH5P8129N-60 (CMOS 1M (128K x 8) Pseudo-Static RAM, 60 ns, 32-pin, 525-mil SOP)

5P8129-14