4+3 Multiphase R3™ PWM Regulator for Intel IMVP8™ Desktop CPUs with SMBus Support

ISL95866

Compliant with Intel IMVP8™, the ISL95866 provides a complete power solution for desktop microprocessors supporting the core (IA), graphics (GT), or unsliced graphics (GTUS or GTX). The controller provides control and protection for two Voltage Regulators (VR). The first VR can be configured for 4-, 3-, 2- or 1-phase operation. The second VR is configurable for 3-, 2- or 1-phase operation. The VRs feature a programmable SVID address to allow maximum flexibility in supporting desktop processor SKUs. Both controller outputs share a common serial control bus to communicate with the CPU and achieve lower cost and smaller board area compared with a two-chip approach.

Based on Intersil's Robust Ripple Regulator R3™ technology, the R3™ modulator has many advantages compared to traditional modulators. These include faster transient settling time, variable switching frequency in response to load transients and improved light-load efficiency due to diode emulation mode with load-dependent low switching frequency.

The ISL95866 has several other key features. The controller features three integrated +12V gate drivers with two on the VR A output. The controller supports either DCR current sensing with a single NTC thermistor for DCR temperature compensation or more precision through resistor current sensing if desired. Both outputs feature remote voltage sense, programmable I_{MAX}, adjustable switching frequency, OC protection, and single VR_READY power-good indicator. The ISL95866 features an SMBus interface, which supports enabling or disabling droop, output voltage offset adjustment, and disabling of OVP and OCP protections.

Features

- Supports Intel serial data bus interface
- SMBus/PMBus/I^2C interface with SVID conflict free
  - DROOP, OVP, and OCP enable/disable
  - Voltage offset adjustment
- Green hybrid digital R3™ modulator
  - Excellent transient response
  - Phase shedding with power state selection
  - Diode emulation in single-phase for high light-load efficiency
- Dual output controller
  - Voltage regulator A: 4-, 3-, 2-, or 1-phase designs with two +12V integrated gate drivers
  - Voltage regulator B: 3-, 2-, or 1-phase designs with one +12V integrated gate driver
- 0.5% system accuracy over-temperature
- Supports multiple current-sensing methods
  - Lossless inductor DCR current sensing
  - Precision resistor current sensing
- Differential remote voltage sensing
- Resistor programmable address selection, I_{MAX}, and switching frequency for both outputs
- Adaptive body diode conduction time reduction

Applications

- IMVP8™ compliant desktops

Related Literature

- For a full list of related documents, visit our website
  - ISL95866 product page

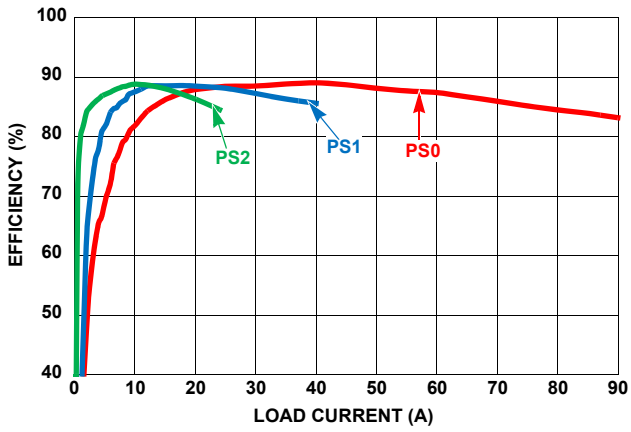

FIGURE 1. 4-PHASE EFFICIENCY vs LOAD

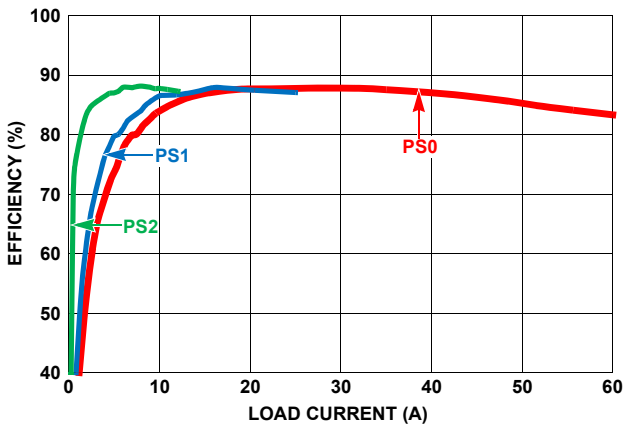

FIGURE 2. 3-PHASE EFFICIENCY vs LOAD

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Block Diagram

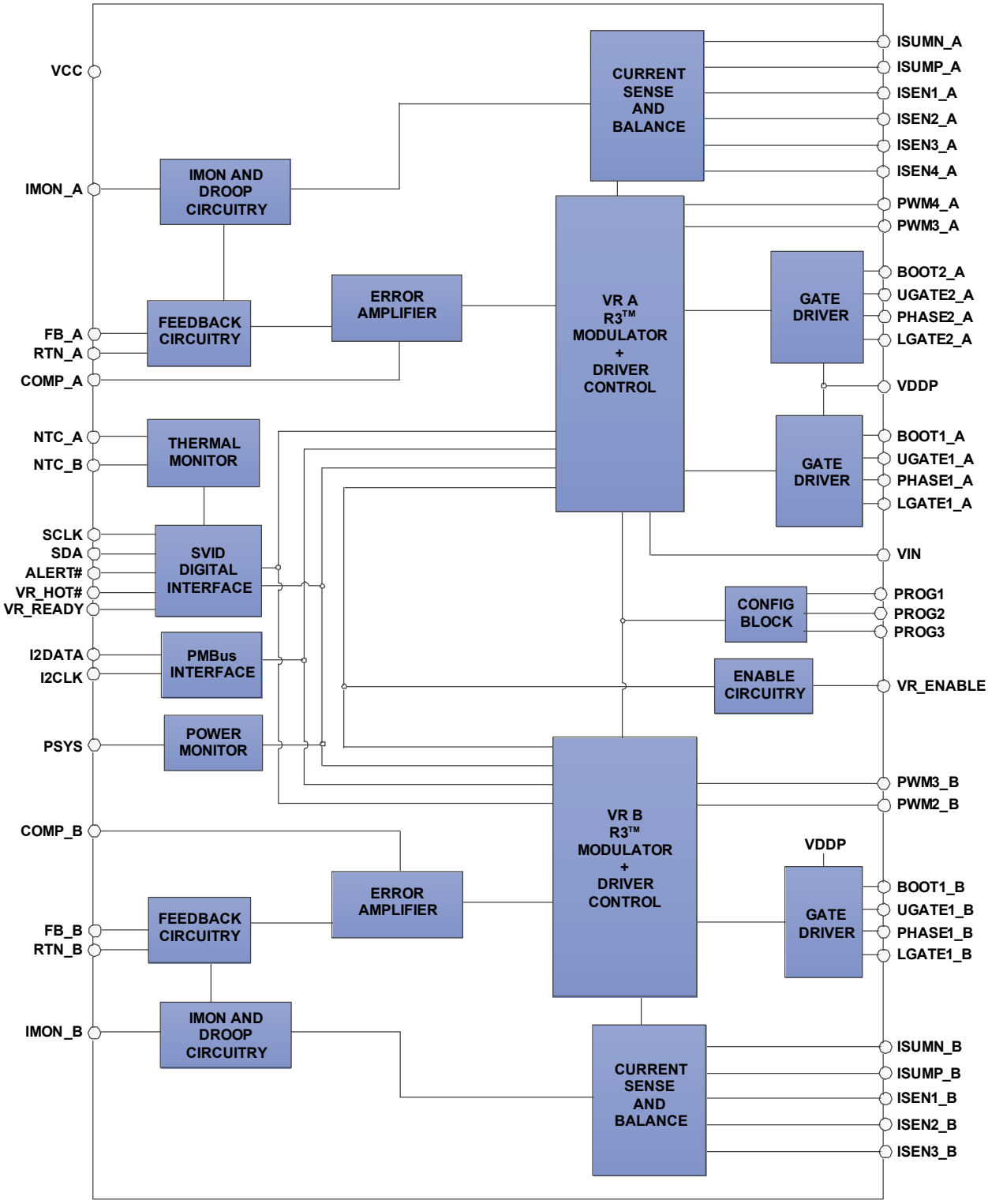


FIGURE 3. BLOCK DIAGRAM

Simplified Application Circuit for High Power CPU Core

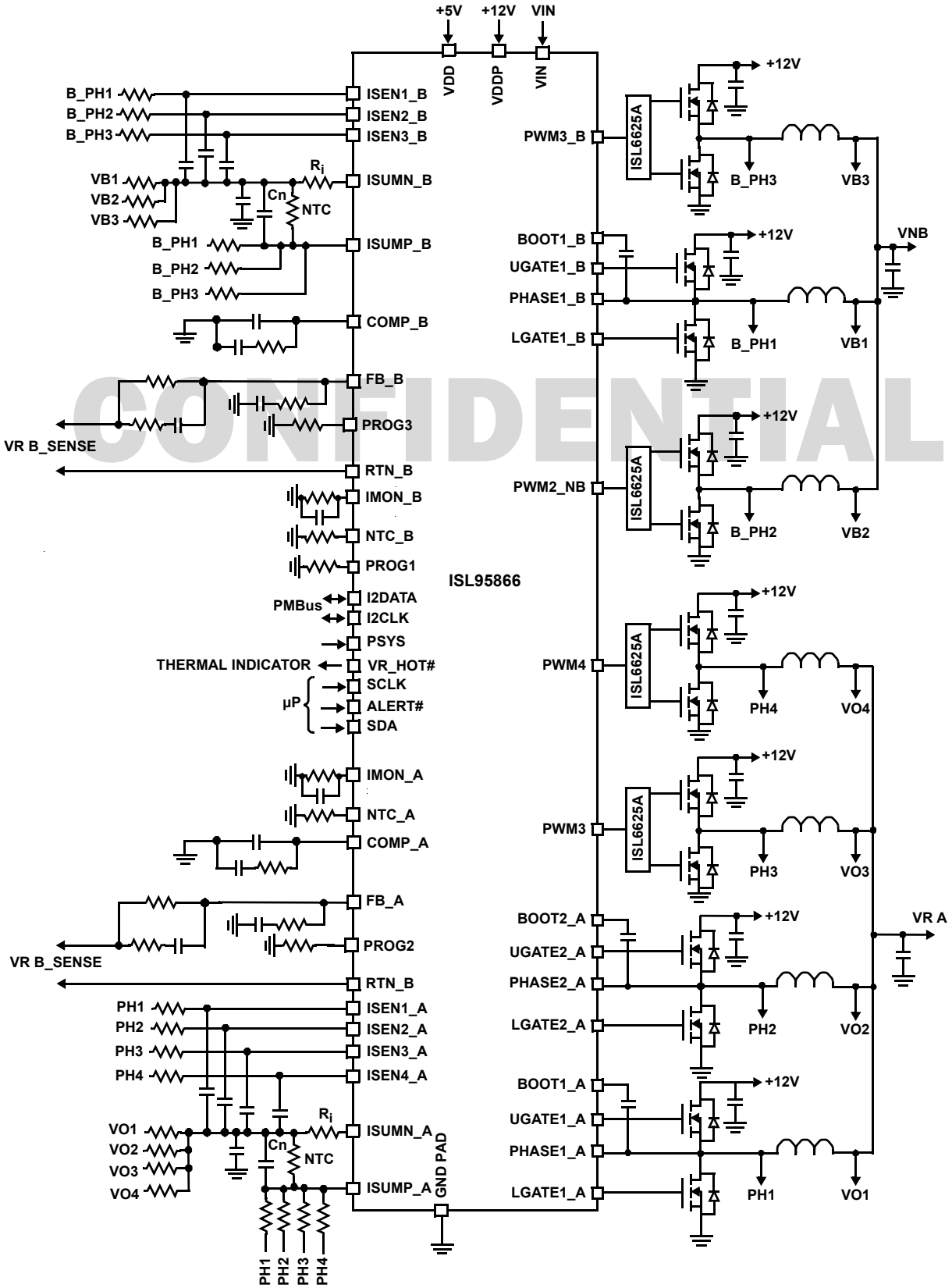


FIGURE 4. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Simplified Application Circuit for ISL95856 Drop-In Support

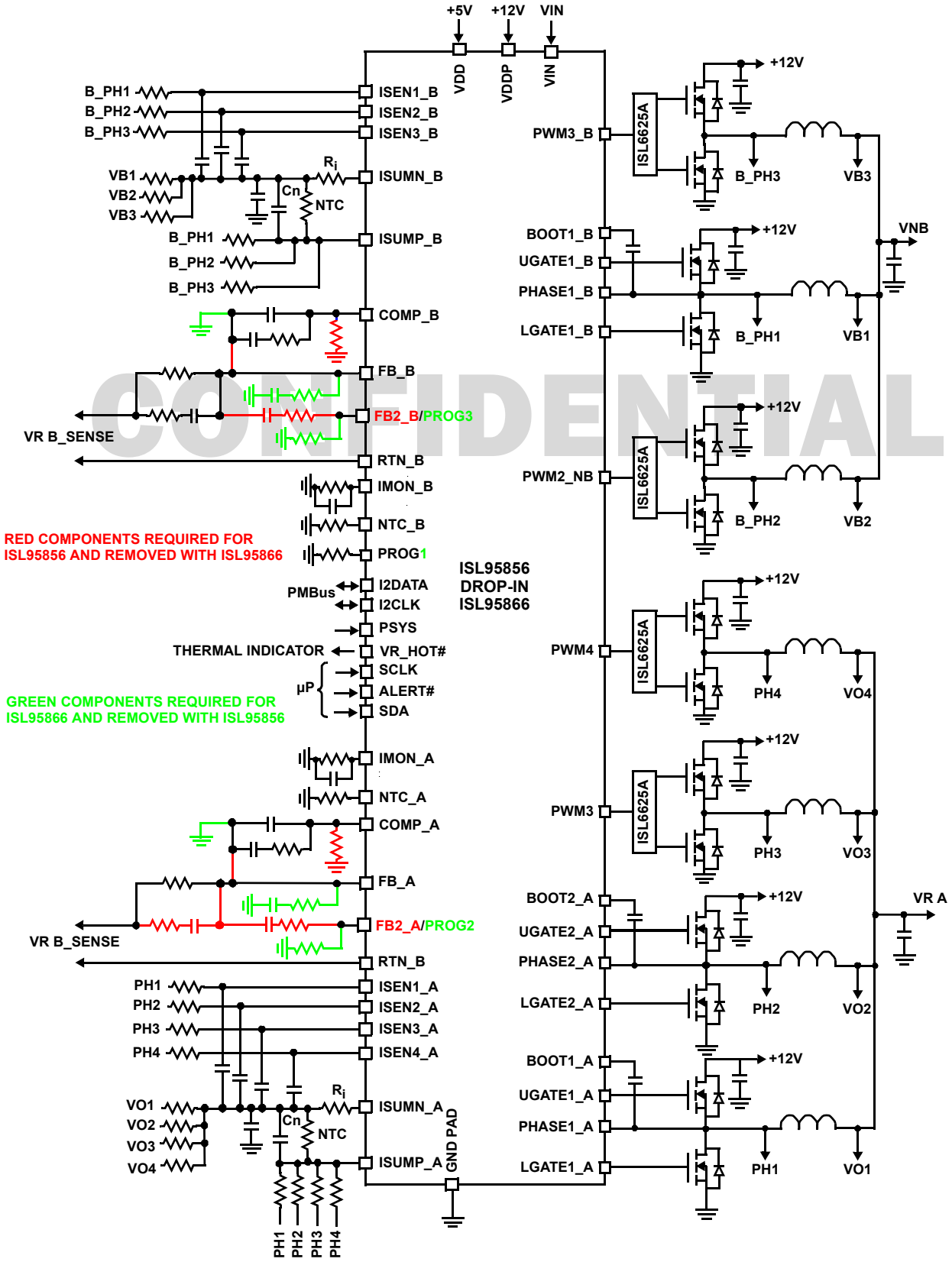


FIGURE 5. TYPICAL APPLICATION CIRCUIT USING INDUCTOR DCR SENSING

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL95866HRZ	95866 HRZ	-10 to +100	52 Ld 6x6 QFN	L52.6x6A
ISL95866IRZ	95866 IRZ	-40 to +100	52 Ld 6x6 QFN	L52.6x6A

NOTES:

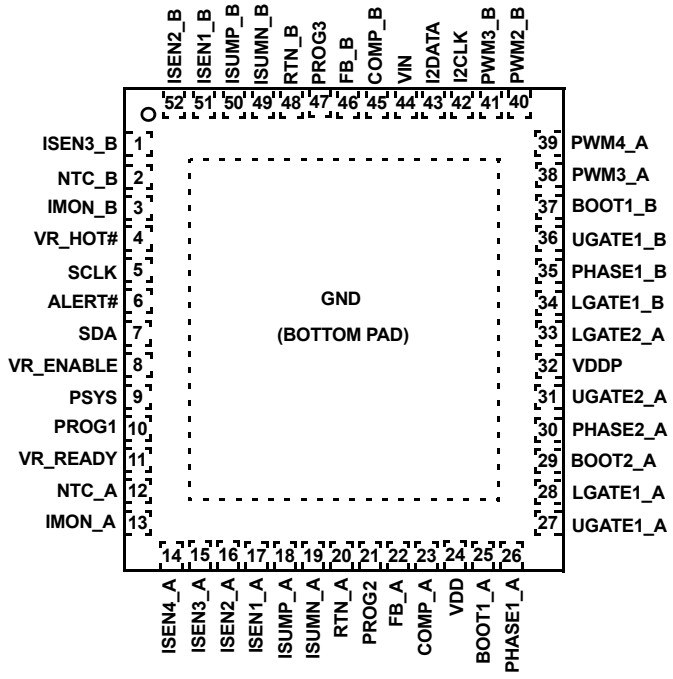
1. Add “-T” suffix for 4k tape and reel option. Refer to TB347 for details on reel specifications.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for ISL95866. For more information on MSL, see tech brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	MAXIMUM PHASE COUNT
ISL95866	4+3
ISL95868	3+2

Pin Configuration

ISL95866
(52 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	ISEN3_B	Individual current sensing for Channel 3 of the VR B. When ISEN3_B is pulled to +5V, the controller will disable Channel 3 and VR B will run as a 2-phase.
2	NTC_B	Thermistor input to the temperature monitor circuitry from VR B. Connect this pin to a resistor network with an NTC thermistor to GND. A current is sourced from the pin and generates a voltage, which is monitored versus an internal threshold to determine when the designated point is too hot. The IC temperature monitor circuitry controls the VR_HOT# output.
3	IMON_B	Regulator B current monitor. The IMON_B pin sources a current proportional to the regulator output current. A resistor connected from this pin to ground will set a voltage that is proportional to the load current. This voltage is sampled internally to produce a digital IMON_B signal that can be read through the serial communication bus.
4	VR_HOT#	Open-drain thermal overload output indicator. Considered part of the communication bus with the CPU.
5	SCLK	Communication bus between the CPU and the VRs.
6	ALERT#	
7	SDA	
8	VR_ENABLE	Controller enable input. A high level logic signal on this pin enables the controller.
9	PSYS	Analog input from the platform battery charger that is proportional to real-time, total system power dissipation. Information is to be digitized and stored by the controller to be read by the CPU via SVID.
10	PROG1	Place a resistor from the PROG1 pin to AGND. The resistor value is selected based on programming options defined in the controller option tables.
11	VR_READY	Power-good open-drain output indicating when controller is able to supply regulated voltage on all outputs. Pull up externally with a 680Ω resistor to VDD or 1.9kΩ to 3.3V.
12	NTC_A	Thermistor input to the temperature monitor circuitry from VR A. Connect this pin to a resistor network with an NTC thermistor to GND. A current is sourced from the pin and generates a voltage, which is monitored versus an internal threshold to determine when the designated point is too hot. The IC temperature monitor circuitry controls the VR_HOT# output.
13	IMON_A	Regulator A current monitor. The IMON_A pin sources a current proportional to the regulator output current. A resistor connected from this pin to ground will set a voltage that is proportional to the load current. This voltage is sampled internally to produce a digital IMON_A signal that can be read through the serial communication bus.
14	ISEN4_A	Individual current sensing for VR A Phase 4. When ISEN4_A is pulled to VDD (+5V), the controller will disable VR Phase 4. This signal is used to monitor and correct for phase current imbalance.
15	ISEN3_A	Individual current sensing for VR A Phase 3. When ISEN3_A is pulled to VDD (+5V), the controller will disable VR Phase 3. Do not disable Phase 3 without also disabling Phase 4. This signal is used to monitor and correct for phase current imbalance.
16	ISEN2_A	Individual current sensing for VR A Phase 2. When ISEN2_A is pulled to VDD (+5V), the controller will disable VR Phase 2. Do not disable Phase 2 without also disabling Phase 3. This signal is used to monitor and correct for phase current imbalance.
17	ISEN1_A	Individual current sensing for VR A Phase 1. This signal is used to monitor and correct for phase current imbalance. In 1-phase configurations, connect this pin to GND.
18	ISUMP_A	VR A droop current-sensing inputs.
19	ISUMN_A	
20	RTN_A	Ground return for differential remote output voltage sensing. Connect to remote negative sense point on the CPU through a resistor.
21	PROG2	Place a resistor from the PROG2 pin to AGND. The resistor value is selected based on programming options defined in the controller option tables.
22	FB_A	Output voltage feedback sensing input for regulation of VR A. Connect to the remote positive sense point on the CPU through a resistor. The resistor value can be used to scale droop for VR A.
23	COMP_A	Error amplifier output for VR A. A resistor from the COMP_A pin to ground programs controller functionality. The resistor value is selected based on programming options defined in the controller option tables.
24	VDD	+5V bias supply input for the controller. Bypass to ground with a high quality 0.1µF ceramic capacitor. Use the +5V Always rail, which is present when +12V rail is powered down.
25	BOOT1_A	VR A, Phase 1 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT1_A and the PHASE1_A pins. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT1_A pin each time the PHASE1_A pin drops below VCCP, minus the voltage dropped across the internal boot diode.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
26	PHASE1_A	Current return path for VR A Phase 1 high-side MOSFET gate driver. Connect the PHASE1_A pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 1 of VR A.
27	UGATE1_A	Output of VR A, Phase 1 high-side MOSFET gate driver. Connect the UGATE1_A pin to the gate of the VR A Phase 1 high-side MOSFET.
28	LGATE1_A	Output of VR A, Phase 1 low-side MOSFET gate driver. Connect the LGATE1_A pin to the gate of the VR A Phase 1 low-side MOSFET.
29	BOOT2_A	VR A, Phase 2 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT2_A and the PHASE2_A pins. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT2_A pin each time the PHASE2_A pin drops below VDDP minus the voltage dropped across the internal boot diode.
30	PHASE2_A	Current return path for VR A Phase 2 high-side MOSFET gate driver. Connect the PHASE2_A pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain and the output inductor of Phase 2 of VR A.
31	UGATE2_A	Output of VR A, Phase 2 high-side MOSFET gate driver. Connect the UGATE2_A pin to the gate of the VR A Phase 2 high-side MOSFET.
32	VDDP	Input voltage bias for the internal gate drivers. Connect +5V or +12V to the VDDP pin. Decouple with at least 1µF of an MLCC capacitor.
33	LGATE2_A	Output of VR A, Phase 2 low-side MOSFET gate driver. Connect the LGATE2_A pin to the gate of the VR A Phase 2 low-side MOSFET.
34	LGATE1_B	Output of VR B, Phase 1 low-side MOSFET gate driver. Connect the LGATE1_B pin to the gate of the VR B Phase 1 low-side MOSFET.
35	PHASE1_B	Current return path for VR B Phase 1 high-side MOSFET gate driver. Connect the PHASE1_B pin to the node consisting of the high-side MOSFET source, the low-side MOSFET drain, and the output inductor of Phase 1 of VR B.
36	UGATE1_B	Output of VR B, Phase 1 high-side MOSFET gate driver. Connect the UGATE1_B pin to the gate of the VR B Phase 1 high-side MOSFET.
37	BOOT1_B	VR B, Phase 1 internal gate driver high-side MOSFET bootstrap capacitor connection. Connect an MLCC capacitor between the BOOT1_B and the PHASE1_B pins. The boot capacitor is charged through an internal boot diode connected from the VDDP pin to the BOOT1_B pin each time the PHASE1_B pin drops below VDDP, minus the voltage dropped across the internal boot diode.
38	PWM3_A	PWM output of Channel 3 of VR A. Disabled if ISEN3_A is tied to +5V.
39	PWM4_A	PWM output of Channel 4 of VR A. Disabled if ISEN4_A is tied to +5V.
40	PWM2_B	PWM output for Channel 2 of VR B. Disabled when ISEN2_B is tied to +5V.
41	PWM3_B	PWM output for Channel 3 of VR B. Disabled when ISEN3_B is tied to +5V.
42	I2CLK	SMBus/PMBus/I^2C interface used for additional communication with the controller outside of the CPU interface pins. Tie to VDD with 4.7kΩ pull-up resistor when not used.
43	I2DATA	
44	VIN	Input supply voltage used for input voltage feed-forward.
45	COMP_B	Error amplifier output for VR B. A resistor from the COMP_B pin to ground programs controller functionality. The resistor value is selected based on programming options defined in the controller option tables.
46	FB_B	Output voltage feedback sensing input for regulation of VR B. Connect to the remote positive sense point on the CPU through a resistor. The resistor value can be used to scale droop for VR B.
47	PROG3	Place a resistor from the PROG3 pin to AGND. The resistor value is selected based on programming options defined in the controller option tables.
48	RTN_B	Ground return for differential remote output voltage sensing. Connect to remote negative sense point on the CPU through a resistor.
49	ISUMN_B	Inverting input of the transconductance amplifier for current monitor and load line of VR B.
50	ISUMP_B	Noninverting input of the transconductance amplifier for current monitor and load line of VR B.
51	ISEN1_B	Individual current sensing for VR B Phase 1. This signal is used to monitor and correct for phase current imbalance. In 1-phase configurations, connect this pin to GND.
52	ISEN2_B	Individual current sensing for VR B Phase 2. When ISEN2_B is pulled to VDD (+5V), the controller will disable VR Phase 2. This signal is used to monitor and correct for phase current imbalance.
	GND (Bottom Pad)	Signal common of the IC. Unless otherwise stated, signals are referenced to the GND pin.

Absolute Maximum Ratings

Supply Voltage, VDD . . . . . -0.3V to +6.5V
Input Supply Voltage, VIN . . . . . +22V
Gate Driver Supply Voltage, VDDP . . . . . -0.3V to + 15V
Boot Voltage (VBOOT) . . . . . -0.3V to +32V
UGATE Voltage (VUGATE) . . . . . (VPHASE - 0.3V_{DC}) to VBOOT + 0.3V
VPHASE - 3.5V (<100ns Pulse Width, 2µJ) to VBOOT + 0.3V
LGATE Voltage (VLGATE) . . . . . (GND - 0.3V_{DC}) to VDDP + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to VDDP + 0.3V
PHASE Voltage (VPHASE) . . . . . (GND - 0.3V_{DC}) to 25V_{DC}
GND - 8V (<400ns Pulse Width, 20µJ)
Open-Drain Outputs, PGOOD, PGOOD_NB, VR_HOT_L. . . . . -0.3V to +6.5V
All Other Pins . . . . . -0.3V to VDD + 0.3V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
52 Ld QFN Package (Notes 4, 5)	28	2.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Supply Voltage, V_{DD} . . . . . +5V ±5%
Input Supply, V_{IN} . . . . . +9V to +20V
$VDDP_{NOMINAL}$ = 5V
Input Supply, V_{IN} . . . . . +9V to +13.2V
$VDDP_{NOMINAL}$ = 12V
Maximum BOOT Voltage, V_{BOOT} . . . . . +26V
Driver Supply Voltage, VDDP . . . . . +4.5V to +13.2V
Ambient Temperature
HRZ . . . . . -10°C to +100°C
IRZ . . . . . -40°C to +100°C
Junction Temperature
HRZ . . . . . -10°C to +125°C
IRZ . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted.
Boldface limits apply across the operating temperature range, -40°C to +100°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT POWER SUPPLY						
V_{IN} Supply Current	I_{VIN}	VR_ENABLE = 1V		44	**60**	µA
		VR_ENABLE = 0V			**1**	µA
V_{DD} Supply Current	I_{VDD}	VR_ENABLE = 1V		11	**14**	mA
		VR_ENABLE = 0V			**128**	µA
VDDP Supply Current	I_{VDDP}	VR_ENABLE = 1V, VDDP = +12V		290	**450**	µA
		VR_ENABLE = 0V VDDP = +12V			**1.5**	mA
POWER-ON RESET THRESHOLDS						
VDD POR Threshold	VDD_POR_r	V_{DD} rising		4.35	**4.50**	V
	VDD_POR_f	V_{DD} falling	**4.00**	4.15		V
VDDP POR Threshold	$VDDP\_POR_r$	V_{DD} rising		4.25	**4.50**	V
	$VDDP\_POR_f$	V_{DD} falling	**3.35**	3.80		V
VIN POR Threshold	VIN_POR_r	V_{IN} rising		7.85	**8.40**	V
	VIN_POR_f	V_{IN} falling	**6.7**	7.3		V

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SYSTEM AND REFERENCES						
System Accuracy	HRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.52V	-0.5		+0.5	%
		VID = 0.50V to 0.745V	-7		+7	mV
		VID = 0.25V to 0.495V	-10		+10	mV
	IRZ %Error (V_{OUT})	No load; closed loop, active mode range, VID = 0.75V to 1.52V	**-0.8**		**+0.8**	%
		VID = 0.50V to 0.745V	**-9**		**+9**	mV
		VID = 0.25V to 0.495V	**-12**		**+12**	mV
Maximum Output Voltage	$V_{OUT(max)}$	VID = [11111111]		1.52		V
Minimum Output Voltage	$V_{OUT(min)}$	VID = [00000000]		0.0		V
V_{BOOT} Voltage		Intel default V_{BOOT}		0		V
		V_{BOOT} debug		1.05		V
CHANNEL FREQUENCY						
300kHz Configuration	f_{SW_300k}	Configured by PROG pin	**280**	300	**320**	kHz
445kHz Configuration	f_{SW_445k}	Configured by PROG pin	**410**	445	**480**	kHz
AMPLIFIERS						
Current-Sense Amplifier Input Offset	HRZ	I_{FB} = 0A	-0.15		+0.15	mV
	IRZ	I_{FB} = 0A	**-0.20**		**+0.20**	mV
Error Amp DC Gain	A_{v0}			119		dB
Error Amp Gain-Bandwidth Product	GBW	C_L = 20pF		17		MHz
ISEN						
Offset Voltage		Maximum of I_{SEN} - minimum of I_{SEN}			1	mV
Input Bias Current				20		nA
IMON						
IMON Output Current		ISUM- pin current = 40µA	9.7	10.0	10.3	µA
		ISUM- pin current = 20µA	4.8	5.0	5.2	µA
		ISUM- pin current = 4µA	0.875	1.000	1.125	µA
ICCMAX Alert Trip Voltage		Rising	1.185	1.200	1.215	V
ICCMAX Alert Reset Voltage		Falling	1.115	1.130	1.145	V
VR_READY AND PROTECTION MONITORS						
VR_READY Low Voltage	V_{OL}	I_{VR_READY} = 4mA		0.15	**0.40**	V
VR_READY Leakage Current	I_{OH}	VR_READY = 5V	**-1**		**1**	µA
VR_READY Delay		Time from VR_ENABLE high to VR_READY high; V_{BOOT} = 1.05V		1.15	**1.70**	ms
VR_HOT# Low Resistance		$I_{VR\_HOT\#}$ = 10mA		7	12	Ω
VR_HOT# Leakage Current		$V_{VR\_HOT\#}$ = 5V			**1**	µA
ALERT# Low Resistance		$I_{ALERT\#}$ = 10mA		7	**12**	Ω
ALERT# Leakage Current		$V_{ALERT\#}$ = 5V			**1**	µA
GATE DRIVER						
UGATE Pull-Up Resistance	R_{UGPU}	200mA source current, VDDP = +5V		3.73		Ω
		200mA source current, VDDP = +12V		3.71		Ω
UGATE Source Current	I_{UGSRC}	UGATE - PHASE = 2.5V, VDDP = +5V		0.59		A
		UGATE - PHASE = 2.5V, VDDP = +12V		1.30		A

Electrical Specifications

Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
UGATE Pull-Down Resistance	R_{UGPD}	250mA sink current, VDDP = +5V		1.43		Ω
		250mA sink current, VDDP = +12V		1.41		Ω
UGATE Sink Current	I_{UGSNK}	UGATE - PHASE = 2.5V, VDDP = +5V		1.25		A
		UGATE - PHASE = 2.5V, VDDP = +12V		1.27		A
LGATE Pull-Up Resistance	R_{LGPU}	250mA source current, VDDP = +5V		2.82		Ω
		250mA source current, VDDP = +12V		2.75		Ω
LGATE Source Current	I_{LGSRC}	LGATE - VSSP = 2.5V, VDDP = +5V		0.76		A
		LGATE - VSSP = 2.5V, VDDP = +12V		1.75		A
LGATE Sink Resistance	R_{LGPD}	250mA sink current, VDDP = +5V		0.6		Ω
		250mA sink current, VDDP = +12V		0.6		Ω
LGATE Sink Current	I_{LGSNK}	LGATE - VSSP = 2.5V, VDDP = +5V		2.14		A
	I_{LGSNK}	LGATE - VSSP = 2.5V, VDDP = +12V		2.14		A
UGATE to LGATE Dead Time	t_{UGFLGR}	UGATE falling < 1V to LGATE rising > 1V, VDDP = +5V, no load		59		ns
LGATE to UGATE Dead Time	t_{LGFUGR}	LGATE falling < 1V to UGATE rising > 1V, VDDP = +5V, no load		37		ns
PWM						
PWM Output Low	V_{OL}	Sinking 5mA			**1.0**	V
PWM Output High	V_{OH}	Sourcing 5mA	**4.0**			V
PWM Tri-State Leakage		PWM = 2.5V			**0.5**	µA
PROTECTION						
Overvoltage Threshold	OV_H	V_{ISUMN} > setpoint for >1µs, SET_OV = 00h	**V_{ID} + 250mV**	V_{ID} + 300mV	**V_{ID} + 330mV**	V
Overcurrent Trip Threshold [IMONx Voltage Based Detection]	V_{IMONx_OCP}	PS0 in 4-, 3-, 2-phase configurations, or any PSx in 1-phase configuration	**54**	60	**66**	µA
		PS1 in 3-phase configuration	**36**	40	**44**	µA
		PS1 in 4-phase configuration PS1/2/3 in 2-phase configuration	**27**	30	**33**	µA
		PS2/3 in 4- or 3-phase configuration	**18**	20	**22**	µA
NTC Source Current		NTC = 1.3V	**9.5**	10.0	**10.5**	µA
NTC VR_HOT# Trip Voltage		NTC voltage forced, voltage falling threshold	**0.189**	0.199	**0.209**	V
NTC VR_HOT# Reset Voltage		Rising	**0.211**	0.221	**0.231**	V
Therm_ Alert Trip Voltage		Falling	**0.203**	0.213	**0.223**	V
Therm_ Alert Reset Voltage		Rising	**0.226**	0.236	**0.246**	V
SLEW RATE						
Fast Slew Rate			10.0	12.5		V
Slow Slew Rate			**5.00**	6.25		V
LOGIC AND SERIAL INTERFACE						
VR_ENABLE Input Low	V_{IL}				**0.3**	V
VR_ENABLE Input High	V_{IH}	HRZ	**0.7**			V
		IRZ	**0.75**			V
VR_ENABLE Leakage Current	I_{ENABLE}	VR_ENABLE = 0V	**-1**	0	1	µA
		VR_ENABLE = 1V			**5**	µA
SCLK Maximum Speed				42		MHz
SCLK Minimum Speed				13		MHz

Electrical Specifications Operating Conditions: V_{DD} = 5V, T_A = -10°C to +100°C (HRZ), f_{SW} = 300kHz, unless otherwise noted. **Boldface limits apply across the operating temperature range, -40°C to +100°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
SCLK, SDA Leakage		VR_ENABLE = 0V, SCLK and SDA = 0V and 1V	**-1**		**1**	µA
		VR_ENABLE = 1V, SCLK, SDA = 1V	**-2**		**1**	µA
		VR_ENABLE = 1V, SDA = 0V	**-28**	-22	**-16**	µA
		VR_ENABLE = 1V, SCLK = 0V	**-55**	-42	**-33**	µA
SDA Low Resistance		I_{SDA} = 10mA		7	**12**	Ω
I2CLK Maximum Speed			**400**			kHz
I2CLK Minimum Speed					**50**	kHz
I^2C Timeout			**25**	30	**35**	ms
I2DATA Low Resistance		I_{I2DATA} = 4mA		28	**40**	Ω
I2CLK, I2DATA Leakage		VR_ENABLE = 0V, I2CLK and I2DATA = 0V and 1V	**-1**		**1**	µA
		VR_ENABLE = 1V, I2CLK and I2DATA = 0V and 1V	**-1**		**1**	µA

NOTE:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Gate Driver Timing Diagram

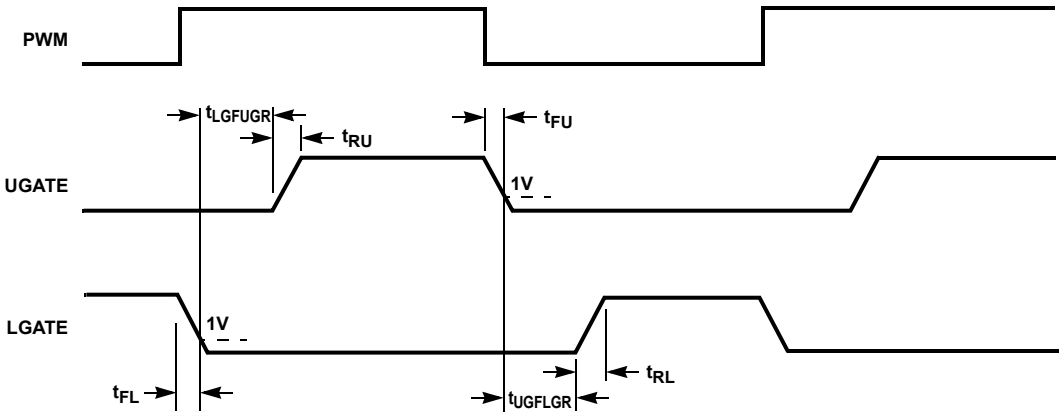


FIGURE 6. GATE DRIVER TIMING DIAGRAM

Typical Performance Curves

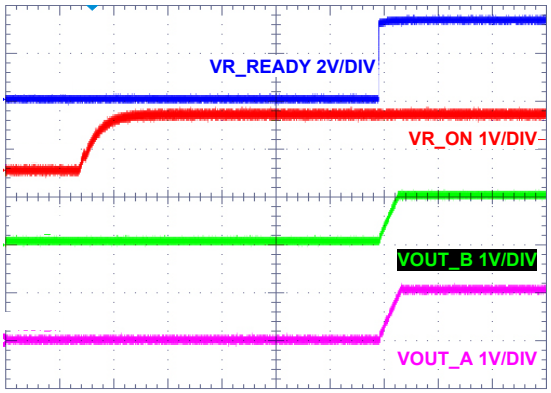


FIGURE 7. START-UP OF VR A AND VR B

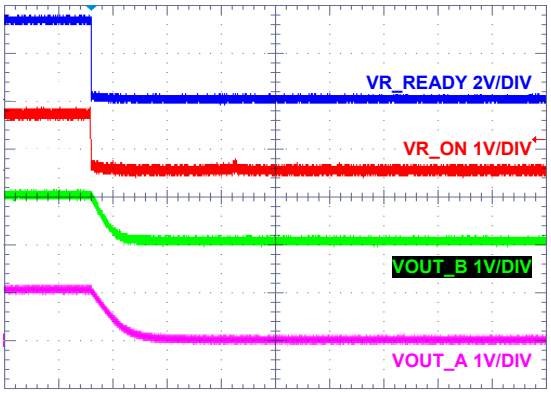


FIGURE 8. SHUTDOWN OF VR A AND VR B

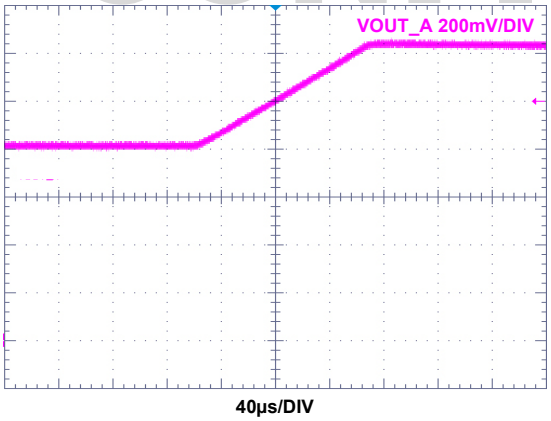


FIGURE 9. VR A INCREASING DAC CHANGE

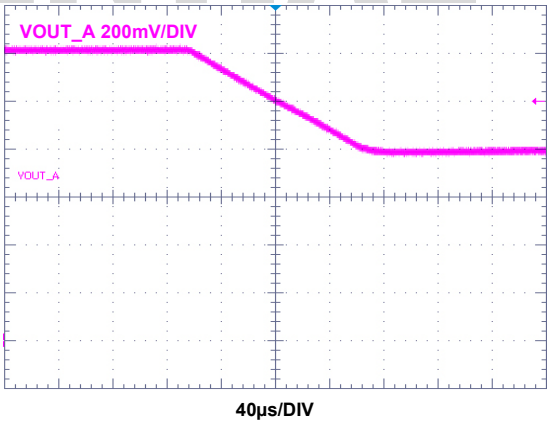


FIGURE 10. VR A DECREASING DAC CHANGE

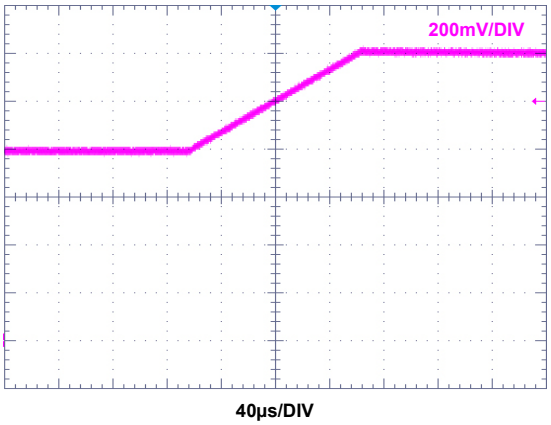


FIGURE 11. VR B INCREASING DAC CHANGE

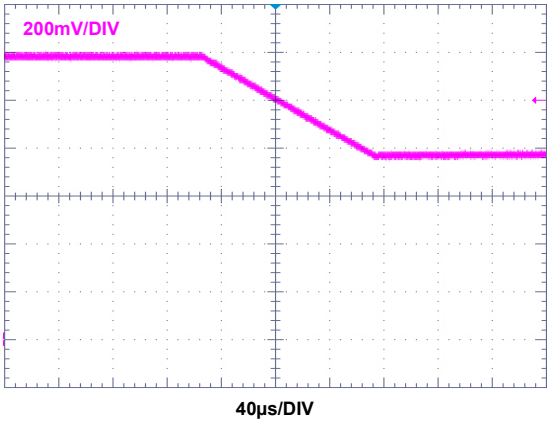


FIGURE 12. VR B DECREASING DAC CHANGE

Theory of Operation

The ISL95866 is a two output, multiphase controller with address support to provide two of three possible Intel IMVP8 desktop microprocessor core (IA), graphics (GT), or unsliced graphics (GTUS or GTX). The controller supports 1-, 2-, 3-, or 4-phase operation on voltage regulator VR A. Voltage regulator VR B supports 1-, 2-, or 3-phase operation. The ISL95866 is designed to be compliant to Intel IMVP8™ specifications with SerialVID features. The system parameters and SVID required registers are programmable through three dedicated programming pins. This greatly simplifies the system design for various platforms and lowers inventory complexity and cost by using a single device. Figures 4 and 5 beginning on page 4 provide a top level view of configuring both outputs using the ISL95866 controller.

R3™ Modulator

The R3™ modulator is Intersil's proprietary synthetic current-mode hysteretic controller, which blends both fixed frequency PWM and variable frequency hysteretic control technologies. This modulator topology offers high noise immunity and a rapid transient response to dynamic load scenarios. Under static conditions, the desired switching frequency is maintained within the entire specified range of input voltages, output voltages, and load currents. During load transients the controller will increase or decrease the PWM pulses and switching frequency to maintain output voltage regulation. Figure 13 illustrates this effect during a load insertion. As the window voltage starts to climb from a load step, the time between PWM pulses decreases as f_{SW} increases to keep the output within regulation.

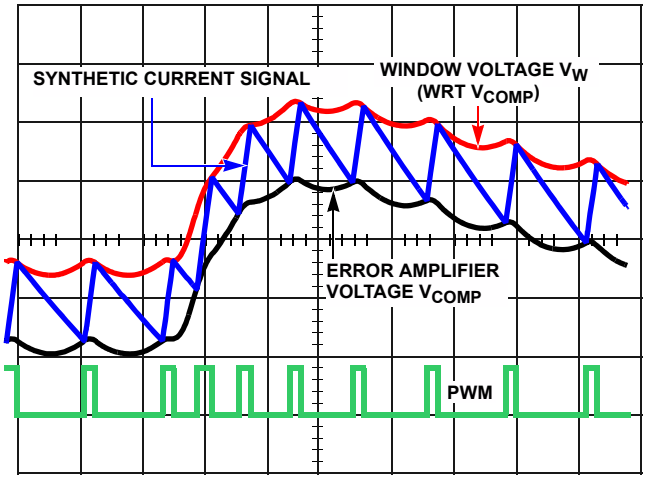


FIGURE 13. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion is impossible to ignore. Multiphase converters overcome the daunting technical challenges in producing a cost-effective and thermally viable single-phase converter at high Thermal Design Current (TDC) levels. The ISL95866 controller outputs reduce the complexity of multiphase implementation by integrating vital functions and requiring minimal output components.

INTERLEAVING

The switching of each channel in a multiphase converter is timed to be symmetrically out-of-phase with the other channels. For the example of a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times that of the ripple frequency of any one phase, as illustrated in Figure 14. The three channel currents (I_{L1}, I_{L2}, and I_{L3}) combine to form the AC ripple current and to supply the DC load current.

The ripple current of a multiphase converter is less than that of a single-phase converter supplying the same load. To understand why, examine Equation 1, which represents an individual channel's peak-to-peak inductor current.

$$I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_{SW} \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value and f_{SW} is the switching frequency.

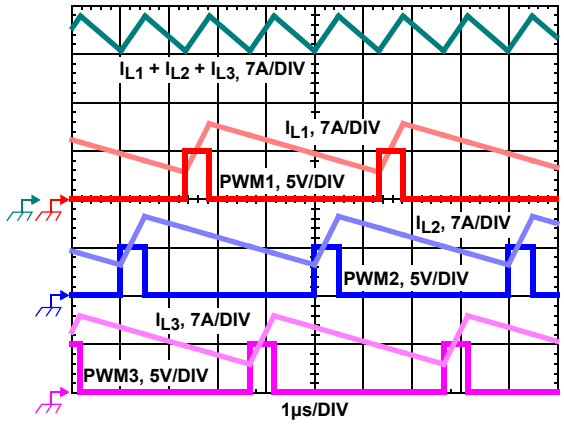


FIGURE 14. PWM AND INDUCTOR CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

In a multiphase converter, the output capacitor current is the superposition of the ripple currents from each of the individual phases. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N (symmetrically phase-shifted inductor currents) in Equation 2. The peak-to-peak overall ripple current ($I_{C(P\text{-}P)}$) decreases with the increase in the number of channels, as shown in Figure 15, which introduces the concept of the Ripple Current Multiplier (K_{RCM}). At the (steady state) duty cycles for which the ripple current, and thus the K_{RCM}, is zero, the turn-off of one phase corresponds exactly with the turn-on of another phase. This results in the sum of all phase currents being always the (constant) load current and therefore, there is no ripple current in this case.

The output voltage ripple is a function of capacitance, capacitor Equivalent Series Resistance (ESR), and the summed inductor ripple current. Increased ripple frequency and lower ripple amplitude mean that the designer can use lower saturation-current inductors and fewer or less costly output capacitors for any performance specification.

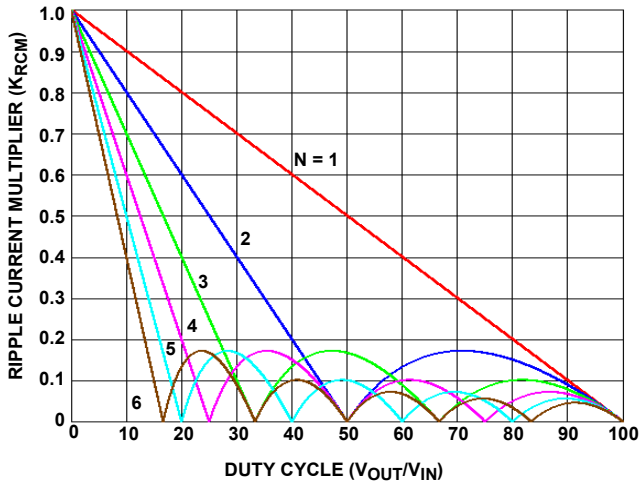


FIGURE 15. RIPPLE CURRENT MULTIPLIER vs DUTY CYCLE

$$I_{C(P-P)} = \frac{V_{OUT}}{L \cdot f_{SW}} K_{RCM} \quad \text{(EQ. 2)}$$

$$K_{RCM} = \frac{(N \cdot D - m + 1) \cdot (m - (N \cdot D))}{N \cdot D}$$

for $m - 1 \le N \cdot D \le m$

$$m = \text{ROUNDUP}(N \cdot D, 0)$$

Another benefit of interleaving is to reduce the input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitors. Figure 16 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

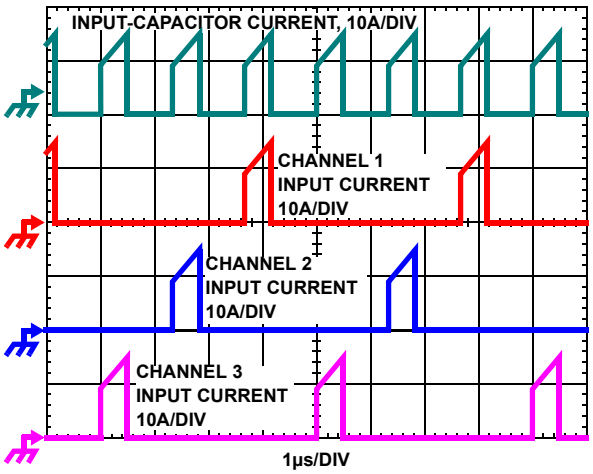


FIGURE 16. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

The converter depicted in Figure 16 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has $11.9A_{RMS}$ input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent 3-phase converter.

A more detailed exposition of input capacitor design is provided in the "Input Capacitor Selection" on page 23.

MULTIPHASE R3™ MODULATOR

The Intersil ISL95866 controller uses the patented R3™ (Robust Ripple Regulator) modulator. The R3™ modulator combines the best features of fixed frequency PWM and hysteretic PWM while eliminating many of their shortcomings. Figure 17 shows the conceptual multiphase R3™ modulator circuit and Figure 18 on page 16 illustrates the operational principles.

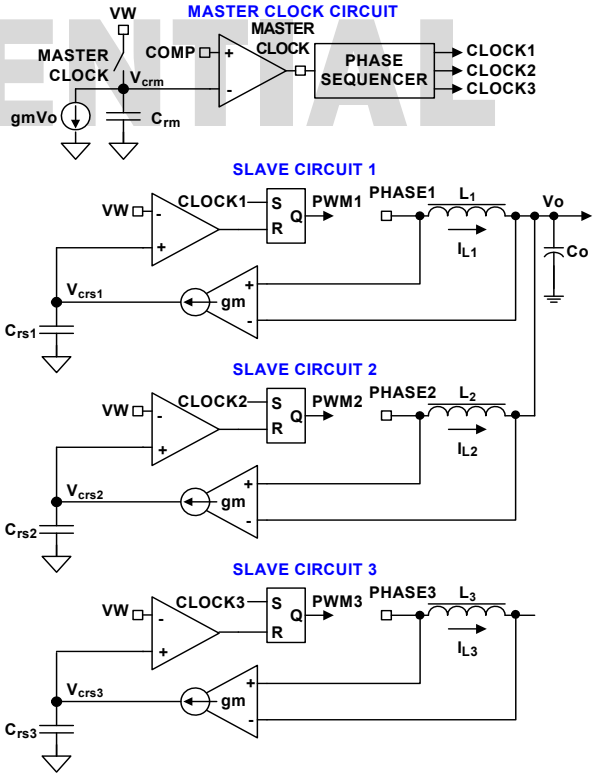


FIGURE 17. R3™ MODULATOR CIRCUIT

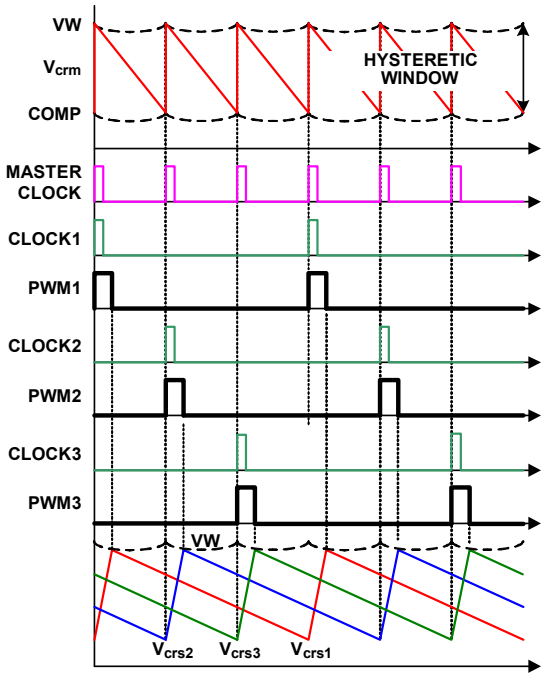


FIGURE 18. R3™ MODULATOR OPERATION PRINCIPLES IN STEADY STATE

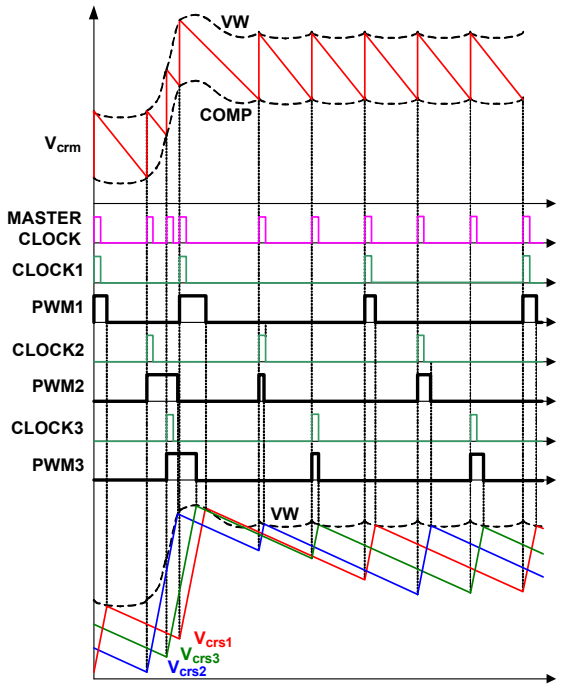


FIGURE 19. R3™ MODULATOR OPERATION PRINCIPLES IN LOAD INSERTION RESPONSE

The internal modulator uses a master clock circuit to generate the clocks for the slave circuits, one per phase. The R3™ modulator master oscillator slews between two voltage signals; the COMP voltage (the output of the voltage sense error amplifier, assuming the topology of Figure 30 on page 27) and VW (Voltage Window), a voltage positively offset from COMP by an offset voltage that is dependent on the nominal switching frequency. The modulator discharges the master clock ripple capacitor, C_{rm}, with a current source equal to gmVo, where gm is a gain factor, dependent on the nominal switching frequency and also on number of active phases. The C_{rm} voltage, V_{crm}, is a sawtooth waveform traversing between the VW and COMP voltages. It resets (charges quickly) to VW when it discharges (with discharge current gmVo) to COMP and generates a one-shot master clock signal. A phase sequencer distributes the master clock signal to the active slave circuits. For example, if the conceptual VR is in 4-phase mode, the master clock signal is distributed to the four phases 90° out-of-phase, in 3-phase mode distributed to the three phases 120° out-of-phase, and in 2-phase mode distributed to Phases 1 and 2 180° out-of-phase. If VR is in 1-phase mode, the master clock signal is distributed to Phase 1 only and is the Clock1 signal.

Each slave circuit has its own ripple capacitor, C_{rsn}, whose voltage mimics the inductor ripple current. A g_m amplifier converts the inductor voltage (or alternatively, series sense resistor voltage, indicative of that phase's inductor current) into a current source to charge and discharge C_{rsn}. The slave circuit turns on its PWM pulse upon receiving its respective clock signal Clock*n* and the current source *charges* C_{rsn} with a current proportional to its respective positive inductor voltage. When the C_{rsn} voltage (V_{Crsn}) rises to VW, the slave circuit turns off the PWM pulse and the current source then *discharges* C_{rsn}, with a current proportional to its respective now-negative inductor voltage. C_{rsn} discharges until the next Clock*n* pulse and the cycle repeats.

Since the modulator works with the V_{crsn}, which are large amplitude and noise-free synthesized signals, it achieves lower phase jitter than conventional hysteretic mode and fixed PWM mode controllers. Unlike conventional hysteretic mode converters, the ISL95866 uses an error amplifier that allows the controller outputs to maintain a 0.5% output voltage accuracy.

Figure 19 illustrates the operational principles during load insertion response. The COMP voltage rises during load insertion (due to the sudden discharge of the output capacitor driving the inverting input of the error amplifier), generating the master clock signal more quickly. Thus, the PWM pulses turn on earlier, increasing the effective switching frequency. This phenomenon allows for higher control loop bandwidth than conventional fixed frequency PWM controllers. The VW voltage rises with the COMP voltage, making the PWM on-time pulses wider. During load release response, the COMP voltage falls. It takes the master clock circuit longer to generate the next master clock signal so the PWM pulse is held off until needed. The VW voltage falls with the COMP voltage, reducing the current PWM pulse width. The inherent pulse frequency and width increases due to an increasing load transient. Likewise, the pulse frequency and width reductions due to a decreasing load transient, produce the excellent load transient response of the R3™ modulator.

Since all phases share the same VW window (master clock frequency generator) and threshold (slave pulse width generator) voltage, dynamic current balance among phases is ensured, inherently, for the duration of any load transient event.

The R3™ modulator intrinsically has input voltage feed-forward control, due to the proportional dependence of the clock generator slave transconductance gains on the input voltage. This dependence decreases the on-time pulse-width of each phase in proportion to an increase in input voltage, making the output voltage insensitive to a fast slew rate input voltage change.

Diode Emulation and Period Stretching

The ISL95866 can operate each of its two controller outputs in Diode Emulation Mode (DEM) to improve light-load efficiency. Diode emulation is enabled in PS2 and PS3 power states. VR A output can invoke diode emulation for Channels 1 and 2, while VR B can put Channel 1 into Diode Emulation mode, which is also known as Discontinuous Conduction Mode (DCM).

In DEM during the PWM off-state (while PWM is low), the low-side MOSFET conducts while the current is flowing from source-to-drain and blocks reverse current, emulating a diode. Figure 20 illustrates that, when LGATE is on, the low-side MOSFET carries current, creating negative voltage on the phase node due to the voltage drop across the ON-resistance. For the case of the ISL6625A driver, the driver monitors the inductor current by monitoring the phase node voltage. It turns off LGATE when the phase node voltage reaches zero to prevent the inductor current from reversing the direction and creating unnecessary power loss.

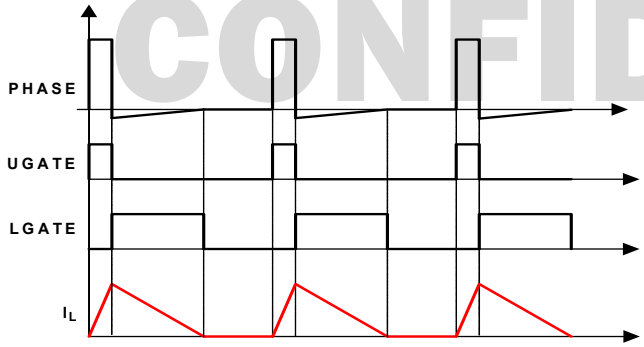


FIGURE 20. DIODE EMULATION

If the load current is light enough, as Figure 20 illustrates, the inductor current will reach and stay at zero before the next phase node pulse and the regulator is in Discontinuous Conduction Mode (DCM). If the load current is heavy enough, the inductor current will never reach 0A and the regulator will appear to operate in Continuous Conduction Mode (CCM), although the controller is nevertheless configured for DEM.

Figure 21 shows the operation principle in Diode Emulation mode at light load. The load gets incrementally lighter in the three cases from top to bottom. The PWM on-time is determined by the VW window size, making the inductor current triangle the same in the three cases (only the time between inductor current triangles changes). The controller clamps the ripple capacitor voltage V_{crs} in DEM to make it mimic the inductor current. It takes the COMP voltage longer to hit V_{crm}, which produces master clock pulses, naturally stretching the switching period. The inductor current triangles move further apart from each other such that the inductor current average value is equal to the load current. The reduced switching frequency improves light-load efficiency.

Because the next clock pulse occurs when V_{COMP} (which tracks output voltage error) rises above V_{CRM}, DEM switching pulse frequency is responsive to load transient events in a manner similar to that of the multiphase CCM operation.

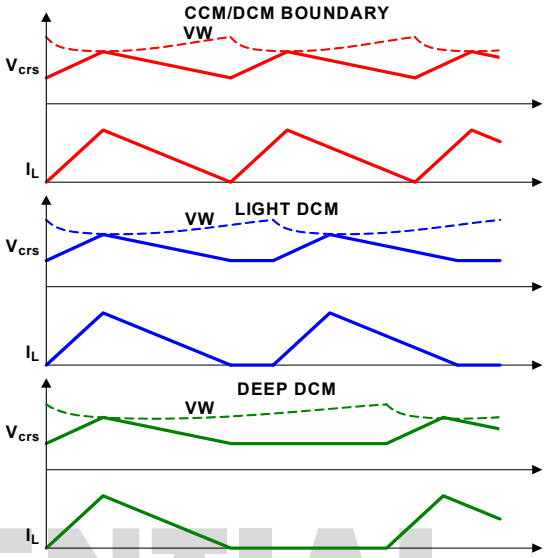


FIGURE 21. PERIOD STRETCHING

Power-On Reset

In order to guarantee sufficient bias for proper operation, the ISL95866 requires the input supplies tied to VDD, VDDP, and VIN exceed their respective rising Power-On Reset (POR) thresholds prior to operation. Hysteresis between the rising and falling thresholds prevent nuisance trips where the ISL95866 would inadvertently turn off. The POR thresholds only turn off the controller when bias voltages drop substantially (see "Electrical Specifications" on page 9).

Start-Up Timing

With the controller's POR thresholds (VDD, VDDP, VIN) exceeded, the start-up sequence begins when VR_ENABLE exceeds the logic high threshold. Figure 22 shows the typical start-up timing for the controller. The IA, GT, or GTUS rails all boot to 0V per IMVP8 specifications.

The controller features a digital soft-start ramp, which increments the DAC to the V_{BOOT} voltage. The power-good signal for all outputs, VR_READY, is asserted high when the DAC begins ramping. At the end of the DAC ramp to V_{BOOT}, ALERT# is asserted low. Similar results occur if VR_ENABLE is tied directly to V_{DD}. The soft-start sequence begins after V_{DD} crosses the rising POR threshold.

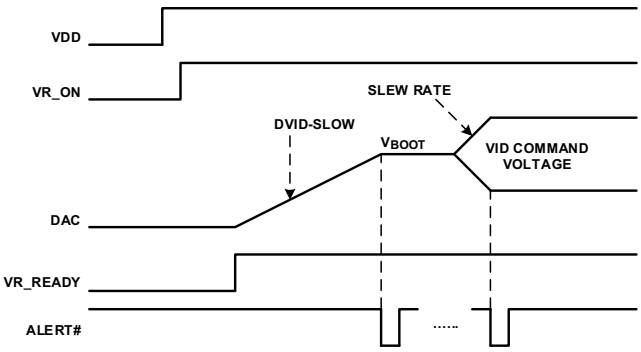


FIGURE 22. TYPICAL SOFT-START WAVEFORMS

Diode Throttling

During the soft-start ramp-up, the ISL95866 operates in Diode Throttling mode until the output has exceeded 400mV. In Diode Throttling mode, the lower MOSFET is kept OFF so that the MOSFET body diode conducts, similar to a standard buck regulator.

Modes of Operation

The ISL95866 controller supports two voltage regulator outputs configured independently. VR A supports 4-phases or less and VR B supports 3-phases or less operation.

VR A Configuration and Operation

The VR A can be configured for 4-, 3-, 2-, or 1-phase operation. Table 2 shows the VR configurations and operational modes programmed by the ISEN4, ISEN3, and ISEN2 pin connections and by the Power State command (SVID Register 32h). To enable a phase, its ISEN pin must be connected through a low pass filter to its respective phase node at the inductor. If its ISEN pin is tied to VDD, that phase is disabled. Phases are disabled in order, starting with the highest numbered phase, as follows:

For a 3-phase configuration, tie the ISEN4 pin to VDD. In this configuration, Phases 1, 2, and 3 are active. For the 2-phase configuration, tie the ISEN3 and ISEN4 pin to VDD. In this configuration, Phases 1 and 2 are active. For the 1-phase configuration, tie the ISEN4, ISEN3, and ISEN2 pin to VDD. In this configuration, only Phase 1 is active.

In a 4-phase configuration, VR A operates in 4-phase CCM in PS0. It enters 2-phase CCM mode in PS1 by dropping Phases 3 and 4 and reducing the overcurrent protection level to 1/2 of the initial value. Based on configuration determined by the PROG1 resistor value, see Table 7 on page 33, the controller will enter either 1-phase CCM or DEM in PS2 and PS3. The controller drops Phases 4, 3, and 2, and reduces the overcurrent protection levels to 1/3 of the initial value.

In a 3-phase configuration, VR A operates in 3-phase CCM in PS0. (Phase 4 is disabled). It enters 2-phase CCM mode in PS1 by dropping Phase 3 and reducing the overcurrent protection level to 2/3 of the initial value. It enters 1-phase CCM or DEM based on the PROG2 resistor configuration in PS2 and PS3 by dropping Phases 3 and 2, and reducing the overcurrent and the protection level to 1/3 of the initial value.

In a 2-phase configuration, VR A operates in 2-phase CCM in PS0. (Phases 4 and 3 are disabled.) It enters 1-phase mode in PS1, PS2, and PS3 by dropping Phase 2 and reducing the overcurrent protection level to 1/2 of the initial value. PS1 operates in CCM and PS2, and PS3 operate in CCM or DEM based on the PROG2 resistor value.

TABLE 2. VR A MODES OF OPERATION

ISEN4	ISEN3	ISEN2	CONFIGURATION	PS	MODE	OCP THRESHOLD (µA)
To Power Stage	To Power Stage	To Power Stage	4-phase CPU VR configuration	0	4-phase CCM	60
				1	2-phase CCM	30
				2	1-phase opt: DEM or CCM	20
				3		
Tied to VDD			3-phase CPU VR configuration	0	3-phase CCM	60
				1	2-phase CCM	40
				2	1-phase opt: DEM or CCM	20
				3		
	Tied to VDD		2-phase CPU VR configuration	0	2-phase CCM	60
				1	1-phase CCM	30
				2	1-phase opt: DEM or CCM	
				3		
		Tied to VDD	1-phase CPU VR configuration	0	1-phase CCM	60
				1		
				2	1-phase opt: DEM or CCM	
				3		

In the 1-phase configuration, the VR A operates in 1-phase CCM in PS0 and PS1, and enters 1-phase CCM or DEM based on the PROG2 configuration in PS2 and PS3. The overcurrent protection level is the same for all power states.

VR B Configuration and Operation

The VR B can be configured for 3-, 2-, or 1-phase operation. Table 3 on page 19 shows the VR configurations and operational modes programmed by the ISEN3 and ISEN2 pin connections and by the Power State command (SVID Register 32h). To enable a phase, its ISEN pin must be connected through a low pass filter, to its respective phase node at the inductor. If its ISEN pin is tied to VDD, that phase is disabled. Phases are disabled in order, starting with the highest numbered phase, as follows:

In a 3-phase configuration, VR B operates in 3-phase CCM in PS0. It enters 2-phase CCM mode in PS1 by dropping Phase 3 and reducing the overcurrent protection level to 2/3 of the initial value. It enters 1-phase CCM or DCM based on PROG2 configuration in PS2 and PS3 by dropping Phases 3 and 2, and reducing the overcurrent and the protection level to 1/3 of the initial value.

In the 2-phase configuration, the VR A operates in 2-phase CCM in PS0. (Phases 4 and 3 are disabled.) It enters 1-phase mode in PS1, PS2, and PS3 by dropping Phase 2 and reducing the overcurrent protection level to 1/2 of the initial value. PS1 operates in CCM, and PS2 and PS3 operate in CCM or DCM based on PROG2 configuration.

In the 1-phase configuration, the VR A operates in 1-phase CCM in PS0 and PS1 and enters 1-phase CCM or DCM based on PROG2 configuration in PS2 and PS3. The overcurrent protection level is the same for all power states.

TABLE 3. VR B MODES OF OPERATION

ISEN3	ISEN2	CONFIGURATION	PS	MODE	OCP THRESHOLD (µA)
To Power Stage	To Power Stage	3-phase CPU VR configuration	0	3-phase CCM	60
			1	2-phase CCM	40
			2	1-phase opt: DEM or CCM	20
			3		
Tied to VDD		2-phase CPU VR configuration	0	2-phase CCM	60
			1	1-phase CCM	30
			2	1-phase opt: DEM or CCM	
			3		
	Tied to VDD	1-phase CPU VR configuration	0	1-phase CCM	60
			1		
			2	1-phase opt: DEM or CCM	
			3		

Disabling Outputs

Each of the ISL95866 VRs is disabled by connecting the ISEN1x pin to +5V. The controller will not acknowledge SVID communication to a disabled VR.

Programming Resistors

There are three programming resistors, PROG1, PROG2 and PROG3 used to configure the ISL95866. A resistor from each pin to GND is used to configure the controller outputs based on Table 3, 4, and 5.

The PROG1 pin sets the address registers and switching frequency for both VRs. VR B droop is also set by PROG1. Table 4 shows how to select the PROG1 resistance to set the address registers for each output (VR A and VR B). The two controller outputs can be configured to support processor core (IA), graphics (GT), andd unsliced graphics (GTUS or GTX) rails of the Intel IMVP8™ processor. The ability to swap the address between the two outputs allows for ease of implementation depending on physical location of the controller on the top or bottom of the motherboard in relation to the processor. The selection should be based on the TDC requirements of the rail and the number of phases required to support the overall current.

The PROG1 resistor also sets the switching frequency, which is common to both VRs. The switching frequency options are 300kHz and 450kHz for most address combinations with a small selection, which allow 350kHz, providing flexibility in optimizing the regulator for a wide array of solutions. VR B droop can be set as active or disabled depending on the need to support a load line by the VR B configured output.

TABLE 4. IMVP8 PROG1 PROGRAMMING TABLE

TYPICAL RESISTOR VALUE (±1%, kΩ)	ADDRESS SELECTION		VR A AND VR B SWITCHING FREQUENCY (kHz)	VR B DROOP
	VR A	VR B		
2.85	IA [00h]	GT [01h]	300	Active
5.62	IA [00h]	GT [01h]	300	Disabled
9.31	IA [00h]	GT [01h]	450	Active
13.3	IA [00h]	GT [01h]	450	Disabled
16.9	GT[01h]	IA [00h]	300	Active
20.5	GT [01h]	IA [00h]	300	Disabled
24.3	GT [01h]	IA [00h]	450	Active
28.0	GT [01h]	IA [00h]	450	Disabled
63.4	GT [01h]	GTUS [03h]	300	Active
71.5	GT [01h]	GTUS [03h]	300	Disabled
78.7	GT [01h]	GTUS [03h]	450	Active
88.7	GT [01h]	GTUS [03h]	450	Disabled
100	IA [00h]	GTUS [03h]	300	Active
110	IA [00h]	GTUS [03h]	300	Disabled
121	IA [00h]	GTUS [03h]	450	Active
137	IA [00h]	GTUS [03h]	450	Disabled
150	GT [01h]	GTUS [03h]	350	Active
165	GT [01h]	GTUS [03h]	350	Disabled

The PROG2 pin sets the VR A $I_{CC(MAX)}$ register value. Determine the maximum current VR A can support and select the $I_{CC(MAX)}$ register value in Table 7 on page 33, which matches or exceeds the desired value. The CPU will read the $I_{CC(MAX)}$ register value and ensure that the CPU current does not exceed the value specified by VR A $I_{CC(MAX)}$ register.

The PROG2 resistor also allows the selection of CCM versus DEM mode operation during power states PS2 and PS3. The selection is common to both VR A and VR B outputs when entering these power states. Reference "Diode Emulation and Period Stretching" on page 17 for more details on CCM and DEM operation.

TABLE 5. IMVP8 PROG2 PROGRAMMING TABLE

TYPICAL RESISTOR VALUE (±1%, kΩ)	IMAX VR A				VR A AND VR B CCM/DCM PS2 AND PS3
	4-PH (A)	3-PH (A)	2-PH (A)	1-PH (A)	
5.62	72	54	36	18	CCM
9.31	80	60	40	20	CCM
13.3	88	66	44	22	CCM
16.9	96	72	48	24	CCM
20.5	104	78	52	26	CCM
24.3	112	84	56	28	CCM
28.0	120	90	60	30	CCM
34.0	128	96	64	32	CCM
41.2	136	102	68	34	CCM
48.7	144	108	72	36	CCM
56.2	152	114	76	38	CCM
63.4	160	120	80	40	CCM
71.5	80	60	40	20	DCM
78.7	88	66	44	22	DCM
88.7	96	72	48	24	DCM
100	104	78	52	26	DCM
110	112	84	56	28	DCM
121	120	90	60	30	DCM
137	128	96	64	32	DCM
150	136	102	68	34	DCM
165	144	108	72	36	DCM
182	152	114	76	38	DCM
215	160	120	80	40	DCM

TABLE 6. IMVP8 PROG3 PROGRAMMING TABLE

TYPICAL RESISTOR VALUE (±1%, kΩ)	IMAX VR B			V_{BOOT} VR A AND VR B (V)
	3-PH (A)	2-PH (A)	1-PH (A)	
5.62	54	36	18	0
9.31	60	40	20	0
13.3	66	44	22	0
16.9	72	48	24	0
20.5	78	52	26	0
24.3	84	56	28	0
28.0	90	60	30	0
34.0	96	64	32	0
41.2	102	68	34	0
48.7	108	72	36	0
56.2	114	76	38	0
63.4	120	80	40	0
71.5	60	40	20	1.05
78.7	66	44	22	1.05
88.7	72	48	24	1.05
100	78	52	26	1.05
110	84	56	28	1.05
121	90	60	30	1.05
137	96	64	32	1.05
150	102	68	34	1.05
165	108	72	36	1.05
182	114	76	38	1.05
215	120	80	40	1.05

PROG3 sets the VR B $I_{CC(MAX)}$ register value. Determine the maximum current VR A can support and select the $I_{CC(MAX)}$ register value in Table 9 on page 38, which matches or exceeds the desired value. The CPU will read the $I_{CC(MAX)}$ register value and ensure that the processor does not exceed the value specified by VR B $I_{CC(MAX)}$ register.

The resistor also selects the common start-up (V_{BOOT}) voltage of both controller outputs. When the controller is in the targeted application with a CPU installed, select PROG3 such that both VR A and VR B power up to a V_{BOOT} voltage of 0V, as required by the Intel IMVP8™ specifications for IA, GT, and GTUS rails.

In the absence of a CPU or for prototype work where booting to 0V would create an issue with testing the voltage regulators, select PROG3 for a V_{BOOT} voltage of 1.05V.

Switching Frequency Selection

There are a number of variables to consider when choosing switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in "MOSFETs" on page 21 and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output voltage ripple as outlined in "Output Filter Design" on page 22. Choose the lowest switching frequency that allows the regulator to meet the transient-response and output voltage ripple requirements.

The ISL95866 supports three switching frequencies, 300kHz, 350kHz, and 450kHz. Refer to Table 4 on page 19 for how to select the switching frequency common to both outputs. Note that when the ISL95866 is in Continuous Conduction Mode (CCM), the switching frequency is not strictly constant due to the nature of the R3™ modulator. As explained in "Multiphase R3™ Modulator" on page 15, the effective switching frequency will increase during load insertion and will decrease during load release to achieve fast response. However, the switching frequency is nearly constant at constant load. Variation is

expected when the power stage condition, such as input voltage, output voltage, load, etc. changes. The variation is usually less than 15% and does not have any significant effect on output voltage ripple magnitude.

Minimum on-time compensation has been implemented in this controller, such that the steady-state PWM on-time will not be shorter than 40ns. A reduction in CCM switching frequency, due to period-stretching, could be observed at some low VID and high V_{IN} conditions due to this function. Note that the minimum on-time mechanism does not directly force the PWM pulse to be greater than 40ns. Instead, it adjusts certain modulator parameters to increase the nominal switching period in response to the output voltage and the input voltage, such that the steady-state expected duty cycle ($D = V_{OUT}/V_{IN}$) results in an on-time of at least 40ns. The modulator dynamic behavior is not changed in any other way, so in response to a transient event the dv/dt of the COMP signal will continue to produce the dynamic frequency and pulse width behavior described in "R3™ Modulator" on page 14. During SetVID or load transient events, PWM on-time pulses of less than 40ns duration may be observed.

PSYS - System Power Monitoring

In an IMVP8 system the PSYS signal is used to monitor the total system input power from either the battery or adapter. When implemented according to Intel's specifications, the PSYS voltage is a 1.2V full-scale analog signal sent into the PSYS pin of the ISL95866. The PSYS signal is then digitized and sent to the CPU over the SVID Bus.

This pin is designed to be used in conjunction with Intersil battery chargers. The full-scale current sent to the ISL95866 PSYS pin from the charger IC should be scaled to a 1.2V full-scale voltage using the appropriate resistor from the PSYS pin to GND.

For those systems where PSYS is not required, the pin can be tied to GND. This will result in the PSYS register producing all zeros if read. This is a valid state and a good condition for instances when PSYS is not in use. PSYS can be disabled through the CPU's MSR registers as well.

General Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Intersil provides complete reference designs, which include schematics, bill of materials, and example board layouts for common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily upon the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer is concerned with whether components can be mounted on both sides of the circuit board; whether through-hole components are permitted; and the total board space available for power supply circuitry. Generally speaking, the most economical solutions are those in which each phase handles between 15A and 25A. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heatsinks and forced air to cool the MOSFETs, inductors, and heat-dissipating surfaces.

MOSFETs

The choice of MOSFETs depends on the current each MOSFET is required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heatsinking and air flow.

Lower MOSFET Power Calculation

The calculation for heat dissipated in the lower (alternatively called low-side) MOSFET of each phase is simple, since virtually all of the heat loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 3, I_M is the maximum continuous output current; I_{P-P} is the peak-to-peak inductor current per phase (see Equation 1 on page 14); d is the duty cycle (V_{OUT}/V_{IN}); and L is the per-channel inductance. Equation 3 shows the approximation.

$$P_{LOW,1} = r_{DS(ON)}\left[\frac{I_M^2}{N} + \frac{I_{P-P}^2}{12}\right]\cdot(1-d) \quad \text{(EQ. 3)}$$

A term can be added to the lower MOSFET loss equation to account for the loss during dead time when inductor current is flowing through the lower MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_{SW}, and the length of dead times (t_{d1} and t_{d2}) at the beginning and end of the lower MOSFET conduction interval, respectively.

$$P_{LOW,2} = V_{D(ON)} f_{SW}\left[\left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)t_{d1} + \left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)t_{d2}\right] \quad \text{(EQ. 4)}$$

Finally, the power loss of output capacitance of the lower MOSFET is approximated in Equation 5:

$$P_{LOW,3} \approx \frac{2}{3}\cdot V_{IN}^{1.5}\cdot C_{OSS\_LOW}\cdot\sqrt{V_{DS\_LOW}}\cdot f_{SW} \quad \text{(EQ. 5)}$$

where C_{OSS_LOW} is the output capacitance of the lower MOSFET at the test voltage of V_{DS_LOW}. Depending on the amount of ringing, the actual power dissipation is slightly higher than this.

Thus, the total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$, $P_{LOW,2}$, and $P_{LOW,3}$.

Upper MOSFET Power Calculation

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses are divided into separate components involving the upper MOSFET switching times, the lower MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET

begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 6, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP(1)}$.

$$P_{UP(1)} \approx V_{IN}\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)\left(\frac{t_1}{2}\right)f_{SW} \quad \text{(EQ. 6)}$$

At turn-on, the upper MOSFET begins to conduct and this transition occurs over a time (t_2). In Equation 7, the approximate power loss is $P_{UP(2)}$.

$$P_{UP(2)} \approx V_{IN}\left(\frac{I_M}{N} - \frac{I_{P-P}}{2}\right)\left(\frac{t_2}{2}\right)f_{SW} \quad \text{(EQ. 7)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower MOSFET's body diode can draw all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is PUP(3) and is approximated in Equation 8:

$$P_{UP(3)} = V_{IN}Q_{rr}f_{SW} \quad \text{(EQ. 8)}$$

The resistive part of the upper MOSFET is given in Equation 9 as $P_{UP(4)}$.

$$P_{UP(4)} \approx r_{DS(ON)}\left[\left(\frac{I_M}{N}\right)^2 + \frac{I_{P-P}^2}{12}\right] \cdot d \quad \text{(EQ. 9)}$$

Equation 10 accounts for some power loss due to the drain-to-source parasitic inductance (L_{DS}, including PCB parasitic inductance) of the upper MOSFET, although it is not exact:

$$P_{UP(5)} \approx L_{DS}\left(\frac{I_M}{N} + \frac{I_{P-P}}{2}\right)^2 \quad \text{(EQ. 10)}$$

Finally, the power loss of output capacitance of the upper MOSFET is approximated in Equation 11:

$$P_{UP(6)} \approx \frac{2}{3} \cdot V_{IN}^{1.5} \cdot C_{OSS\_UP} \cdot \sqrt{V_{DS\_UP}} \cdot f_{SW} \quad \text{(EQ. 11)}$$

where C_{OSS_UP} is the output capacitance of the lower MOSFET at the V_{DS_UP} test voltage. Depending on the amount of ringing, the actual power dissipation is slightly higher than this.

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 6 through 11. Since the power equations depend on MOSFET parameters, choosing the correct MOSFET is an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

DRIVER SELECTION

The two voltage regulator outputs of the ISL95866 feature internal gate drivers and PWM signals to drive external MOSFET drivers, specifically the ISL6625A. The ISL6625A is a similar +12V gate driver to the internal gate drivers of the ISL95866.

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter that smooths the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter necessarily limits the system transient response. The output capacitor must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load current slew rate, di/dt, and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount, as shown in Equation 12:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 12)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current (see "Interleaving" on page 14 and Equation 2 on page 15), a voltage develops across the bulk-capacitor ESR equal to $I_{C(P-P)}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines a lower limit on the inductance as shown in Equation 13.

$$L \geq ESR \cdot \frac{V_{OUT} \cdot K_{RCM}}{f_{SW} \cdot V_{IN} \cdot V_{P-P(MAX)}} \quad \text{(EQ. 13)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current

before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 14 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output voltage deviation than the leading edge. Equation 15 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated and L should be selected based on the lower of the two results. In each equation, L is the per-channel inductance, C is the total output capacitance, and N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_{OUT}}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right] \quad \text{(EQ. 14)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2}\left[\Delta V_{MAX} - \Delta I \cdot ESR\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 15)}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs, which is related to duty cycle and the number of active phases. The input RMS current can be calculated with Equation 16.

$$I_{IN(RMS)} = \sqrt{K_{IN(CM)}^2 \bullet Io^2 + K_{RAMP(CM)}^2 \bullet I_{Lo(P-P)}^2} \quad \text{(EQ. 16)}$$

$$K_{IN(CM)} = \sqrt{\frac{(N \bullet D - m + 1) \bullet (m - N \bullet D)}{N^2}} \quad \text{(EQ. 17)}$$

$$K_{RAMP(CM)} = \sqrt{\frac{m^2(N \bullet D - m + 1)^3 + (m-1)^2(m - N \bullet D)^3}{12N^2D^2}} \quad \text{(EQ. 18)}$$

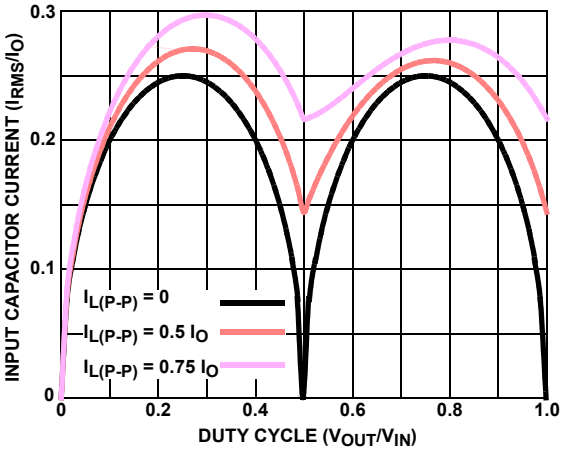


FIGURE 23. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 2-PHASE CONVERTER

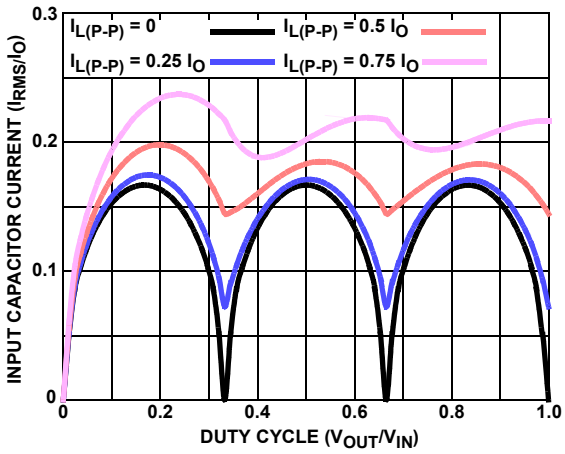


FIGURE 24. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 3-PHASE CONVERTER

For a 2-phase design, use Figure 23 to determine the input capacitor RMS current requirement given the duty cycle, maximum sustained output current (I_O), and the ratio of the per-phase peak-to-peak inductor current ($I_{L(P-P)}$) to I_O. Select a bulk capacitor with a ripple current rating that will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25x greater than the maximum input voltage.

Figures 24 and 25 provide the same input RMS current information for 3- and 1-phase designs, respectively. Use the same approach to selecting the bulk capacitor type and number, as previously described.

Low capacitance, high-frequency ceramic capacitors are needed in addition to the bulk capacitors to suppress leading and falling edge voltage spikes resulting from the high current slew rates produced by the upper MOSFETs turning on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitic impedances and maximize noise suppression.

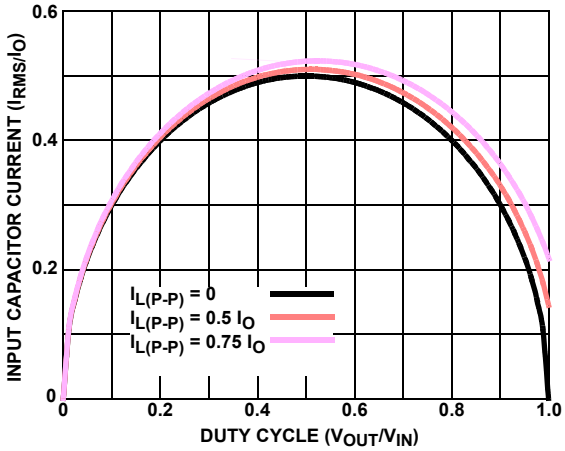


FIGURE 25. NORMALIZED INPUT CAPACITOR RMS CURRENT vs DUTY CYCLE FOR SINGLE-PHASE CONVERTER

MULTIPHASE RMS IMPROVEMENT

Figure 25 provides a reference to demonstrate the dramatic reductions in input capacitor RMS current upon the implementation of the multiphase topology. For example, compare the input RMS current requirements of a 2-phase converter versus that of a single-phase. Assume both converters have a duty cycle of 0.25, maximum sustained output current of 40A and a ratio of $I_{L(P-P)}$ to I_O of 0.5. The single-phase converter would require $17.3A_{RMS}$ current capacity, while the 2-phase converter would only require $10.9A_{RMS}$. The advantages become even more pronounced when the output current is increased and additional phases are added to keep the component cost down relative to the single-phase approach.

Inductor Current Sensing and Balancing

The two VR outputs of the ISL95866 each support a different number of active channels. VR A of the controller can support up to a 4-phase operation and VR B up to a 3-phase operation. Figure 26 shows the inductor DCR current-sensing network as an example of a 3-phase voltage regulator. The principles described can be applied to any of the two outputs.

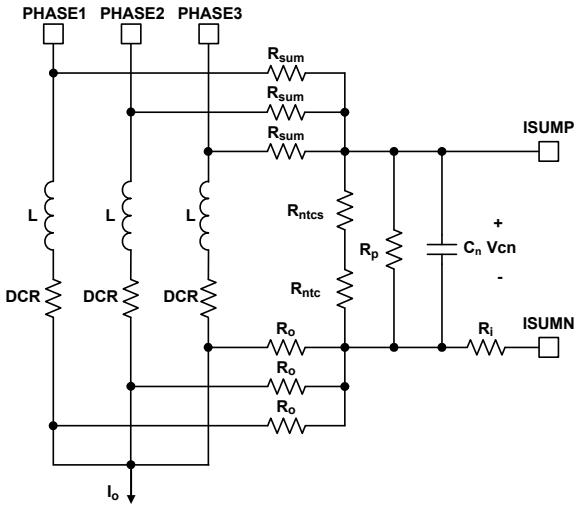


FIGURE 26. DCR CURRENT-SENSING NETWORK

Inductor DCR Current-Sensing Network

Referencing Figure 26, an inductor's current flows through the inductor's DCR and creates a voltage drop. Each inductor has two resistors, R_{sum} and R_o, connected to its pads to accurately sense the inductor current by sensing the DCR voltage drop. The R_{sum} and R_o resistors are connected in a summing network as shown and feed the total current information to the NTC network (consisting of R_{ntcs}, R_{ntc} and R_p) and capacitor C_n. R_{ntc} is a Negative Temperature Coefficient (NTC) thermistor used to compensate for the change in inductor DCR due to ambient temperature changes and due to power dissipation in the inductor.

The inductor output-side pads are electrically shorted in the schematic but have some parasitic trace impedance in an actual board layout, which is why one cannot simply short them together for the current-sensing summing network. It is recommended to use $R_o = 1\Omega$ to provide the needed isolation and resistive averaging between phases in a multiphase regulator and $R_o = 0\Omega$ for a single-phase regulator since no isolation between phases is needed. (Larger resistor values will introduce an error in the current sense during slewing of the output voltage.) Proper connection of inductor current-sense traces to inductor pads is essential for accurate current sensing. Please refer to the ISUMN_*x* and ISUMP_*x* descriptions in the "Layout Guidelines" on page 42. Since the R_o value is much smaller than the rest of the current-sensing circuit, the following analysis will, for simplicity, ignore it.

The summed inductor current information is applied to the capacitor C_n. Equations 19 through 23 describe the frequency-domain relationship between inductor total current $I_o(s)$ and C_n voltage $V_{Cn}(s)$:

$$V_{Cn}(s) = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \times I_o(s) \times A_{cs}(s) \quad \text{(EQ. 19)}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p} \quad \text{(EQ. 20)}$$

$$A_{cs}(s) = \frac{1 + \frac{s}{\omega_L}}{1 + \frac{s}{\omega_{sns}}} \quad \text{(EQ. 21)}$$

$$\omega_L = \frac{DCR}{L} \quad \text{(EQ. 22)}$$

$$\omega_{sns} = \frac{1}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times C_n} \quad \text{(EQ. 23)}$$

where N is the number of phases.

The inductor DCR value increases as the inductor temperature increases, due to the positive temperature coefficient of the copper windings. If uncompensated, this will cause the estimate of inductor current to increase with temperature. The resistance of a co-located NTC thermistor, R_{ntc}, decreases as its temperature increases, compensating for the increase in DCR. Proper selections of R_{sum}, R_{ntcs}, R_p, and R_{ntc} parameters ensure that V_{Cn} represents the inductor total DC current over the temperature range of interest.

There are many sets of parameters that can properly temperature-compensate the DCR change. Since the NTC network and the R_{sum} resistors form a voltage divider, V_{cn} is always a fraction of the inductor DCR voltage. It is recommended to have a high ratio of V_{cn} to the inductor DCR voltage, so the current-sense circuit has a higher signal level to work with.

A typical set of parameters that provide good temperature compensation are: $R_{sum} = 3.65k\Omega$, $R_p = 11k\Omega$, $R_{ntcs} = 2.61k\Omega$, and $R_{ntc} = 10k\Omega$ (ERT-J1VR103J). The NTC network parameters may need to be fine-tuned on actual boards. One can apply full-load DC current and record the output voltage reading immediately; then record the output voltage reading again when the board has reached the thermal steady state. A good NTC network can limit the output voltage drift to within 2mV. It is

recommended to follow the Intersil evaluation board layout and current-sensing network parameters to minimize engineering time.

$V_{Cn}(s)$ response must track $I_o(s)$ over a broad range of frequency for the controller to achieve good transient response. Transfer function $A_{cs}(s)$ (Equation 24) has unity gain at DC, a pole ω_{sns} and a zero ω_L. To obtain unity gain at all frequencies, set ω_L equal to ω_{sns} and solve for Cn.

$$C_n = \frac{L}{\frac{R_{ntcnet} \times \frac{R_{sum}}{N}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times DCR} \quad \text{(EQ. 24)}$$

For example, given N = 3, R_{sum} = 3.65kΩ, R_p = 11kΩ, R_{ntcs} = 2.61kΩ, R_{ntc} = 10kΩ, DCR = 0.9mΩ, and L = 0.36µH, Equation 24 gives C_n = 0.397µF.

When the load current I_{core} has a step change, the output voltage V_{CORE} also has a step change, determined by the DC load line resistance (the resistor-programmable output voltage droop value, or source resistance, of the regulator). Assuming the loop compensator design is correct, Figure 34 shows the expected load transient response waveforms for the correctly chosen value of C_n. If the C_n value is too large or too small, $V_{Cn}(s)$ will not accurately represent the real-time $I_o(s)$, and the load line transient response will deviate from the ideal. If C_n is too small, V_{CORE} will droop excessively (undershoot) upon abrupt load insertion before recovering to the intended DC value, which may create a system failure. Similarly, there is excessive overshoot during load decreases, which may hurt the CPU reliability. If C_n is too large, the V_{CORE} load line response to load changes will lag.

With the proper selection of C_n, assume that $A_{cs}(s) = 1$. With this assumption, Equation 24 is recast as Equation 25:

$$\frac{V_{Cn}}{I_O} = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \quad \text{(EQ. 25)}$$

The value of DCR and R_{ntcnet} are both temperature dependent. However, with a properly designed inductor temperature compensation network, one may also assume the room temperature inductor DCR value and the room temperature value of R_{ntcnet}, in subsequent calculations, since any temperature variation in one value is, ideally, exactly compensated by a variation in the other value. Equation 25 is evaluated, using room temperature resistance values, to obtain a constant value of the ratio V_{Cn}/I_O, in units of resistance, for a given DCR current-sense network design. This constant value, designated ρ_o, assumed to be independent of temperature, is required to complete the regulator design.

Equation 26 applies to the DCR current-sense circuit of Figure 26 on page 24.

$$\rho_o = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N} \right) \Bigg|_{RoomTemp} \quad \text{(EQ. 26)}$$

RESISTOR CURRENT-SENSING NETWORK

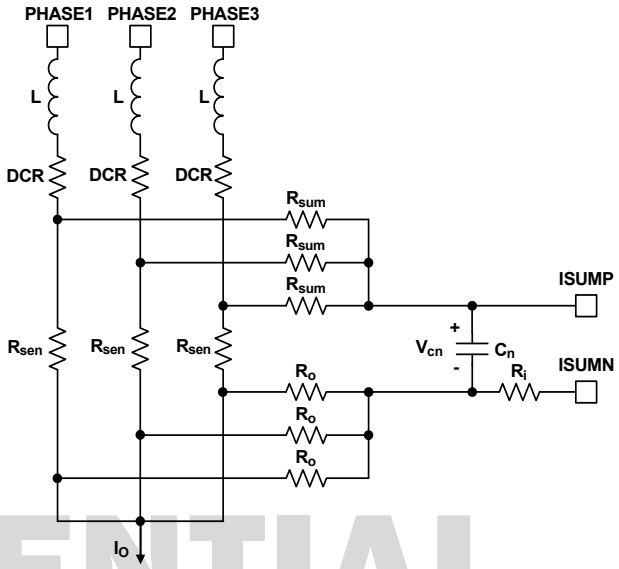


FIGURE 27. RESISTOR CURRENT-SENSING NETWORK

Figure 27 shows the resistor current-sensing network for the example of a 3-phase regulator. Each inductor has a series current-sensing resistor R_{sen}. R_{sum} and R_o are connected to the R_{sen} pads to accurately capture the inductor current information. The R_{sum} and R_o resistors are connected to capacitor C_n. R_{sum} and C_n form a filter for noise attenuation. Equations 27 through 29 give the $V_{Cn}(s)$ expression:

$$V_{Cn}(s) = \frac{R_{sen}}{N} \times I_O(s) \times A_{Rsen}(s) \quad \text{(EQ. 27)}$$

$$A_{Rsen}(s) = \frac{1}{1 + \frac{s}{\omega_{Rsen}}} \quad \text{(EQ. 28)}$$

$$\omega_{Rsen} = \frac{1}{\frac{R_{sum}}{N} \times C_n} \quad \text{(EQ. 29)}$$

Transfer function $A_{Rsen}(s)$ always has unity gain at DC. Current sensing resistor R_{sen} value will not have significant variation over temperature, so there is no need for the NTC network.

The recommended values are R_{sum} = 1kΩ and C_n = 5600pF.

As with the DCR current-sense network, Equation 29 is recast as Equation 30:

$$\frac{V_{Cn}}{I_o} = \frac{R_{sen}}{N} \quad \text{(EQ. 30)}$$

This equation is evaluated to obtain a constant value of the ratio V_{Cn}/I_o, in Ohm units, for a given sense-resistor current-sense network design. This constant value is designated ρ_o in Equation 31.

$$\rho_o = \frac{R_{sen}}{N} \quad \text{(EQ. 31)}$$

Equation 31 applies to the resistor current-sense circuit of Figure 27. As with the DCR-sense design, this constant value is required to complete the regulator design.

PROGRAMMING OF OUTPUT OVERCURRENT PROTECTION, I_{DROOP} AND IMON

The final step in designing the current-sense network is the selection of resistor R_i of Figures 26 or 27. This resistor determines the ratio of the controller's internal representation of output current (I_{droop}, also called the "droop current") to the actual output current, that is, to the sum of all the measured inductor currents. This internal representation is itself a current that is used (a) to compare to the overcurrent protection threshold, (b) to source the I_{droop} current to the FB pin to provide the programmable load-dependent output voltage "droop" or output DC load line, and (c) to drive the IMON pin external resistor to produce a voltage to represent the output current. This is measured and written to the I_{OUT} register, readable via the SVID bus.

Begin by selecting the maximum current that the regulator is designed to provide. This is the value of $I_{CC(MAX)}$ programmed with the programming pin resistance to ground for each VR output. Select the appropriate R_{PROG1} to program the lowest available value of $I_{CC(MAX)}$ that equals or exceeds the expected maximum load. The Overcurrent Protection (OCP) threshold I_{OCP} must exceed this value. I_{OCP} is typically chosen to be 20% to 25% greater than $I_{CC(MAX)}$ to allow for transient inductor current, such as output capacitor inrush current or transient overshoot current and inductor DCR or other current-sense component tolerance, etc. Note that for low values of $I_{CC(MAX)}$, a higher I_{OCP} threshold, as a percentage of $I_{CC(MAX)}$, may be required. I_{OCP} will determine the value of R_i.

Using VR B as the example, refer to Table 3 on page 19. The value of OCP threshold for either phase configuration (1-, 2-, or 3-phase) and any power state (PS0-PS3) is the threshold value of I_{droop} that will trigger the output overcurrent protection. Notice that the OCP threshold value of the PS0 row of any phase configuration is 60µA. R_i should be chosen such that I_{droop} is 60µA when the regulator output current is equal to the chosen value of output I_{OCP} as follows.

The mechanism by which R_i determines I_{droop} is illustrated in Figure 28.

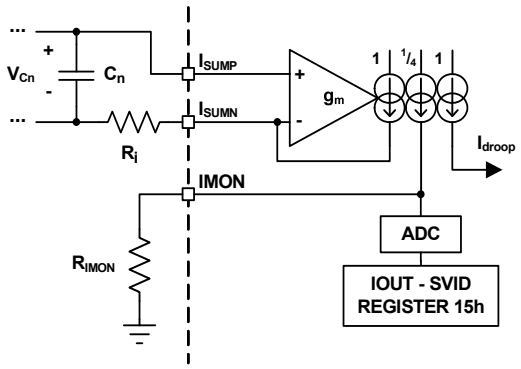


FIGURE 28. DROOP ILLUSTRATION

The ISUM transconductance amplifier produces the current that drops the voltage V_{Cn} across R_i, to make $V_{ISUMN} = V_{ISUMP}$. This current is mirrored 1:1 to produce I_{droop} and 4:1 to produce I_{IMON}. I_{droop} is compared directly to the OCP THRESHOLD, always 60µA in PS0, so R_i must be chosen to obtain the desired I_{OCP} using Equation 32.

$$R_i = \rho_o \times \frac{I_{OCP}}{60\mu A} \quad \text{(EQ. 32)}$$

where ρ_o is the constant value determined in Equation 26 on page 25 or Equation 31.

For a given value of output current, I_o, I_{droop} will have the value shown in Equation 33:

$$I_{droop} = \frac{\rho_o}{Ri} \times I_o \quad \text{(EQ. 33)}$$

I_{droop} is also used to program the slope of the output DC load line. The DC load line slope is the programmable regulator output resistance. Programming of the DC load line is explained in the next section.

The I_{OUT} register (SVID Register 15h) reports an 8-bit unsigned number indicative of the IMON pin voltage, scaled such that its value is 00h when V_{IMON} = 0V and FFh when V_{IMON} = 1.200V typically, 1.215V maximum. With R_i determined, R_{IMON} is chosen such that V_{IMON} = 1.200V when the regulator load current is equal to $I_{CC(MAX)}$, the maximum current value programmed by R_{PROG2}. Select R_{IMON} using Equation 34:

$$R_{IMON} = 1.200V \times \left(\rho_o \times \frac{I_{CC(MAX)}}{Ri \times 4}\right)^{-1} \quad \text{(EQ. 34)}$$

where again ρ_o is the constant value determined in Equation 26 or Equation 31. A capacitor should be added in parallel with R_{IMON} to filter the IMON pin voltage and to set the I_{OUT} register response time constant.

PROGRAMMING THE DC LOAD LINE

The DC load line is the effective DC series resistance of the voltage regulator output. The output series resistance causes the output voltage to "droop" below the selected regulation voltage by a voltage equal to the load current multiplied by the output resistance. The linear relationship of the output voltage drop to load current is called the load line and is expressed in units of resistance. It is designated R_{LL}. Figure 29 shows the equivalent circuit of a Voltage Regulator (VR) with the droop function. An ideal VR is equivalent to a voltage source (V = VID) and output impedance $Z_{out}(s)$. If $Z_{out}(s)$ is equal to the load line slope R_{LL}, i.e., constant output impedance independent of frequency, V_o will have a step response when I_o has a step change.

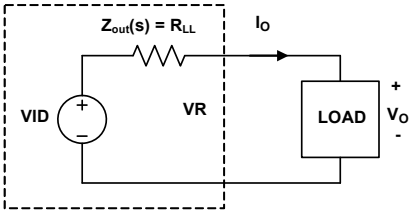


FIGURE 29. VOLTAGE REGULATOR EQUIVALENT CIRCUIT

The ISL95866 provides programmable DC load-line resistance. A typical desired value of the DC load line for Intel IMVP8 applications is R_{LL} = 2mΩ.

The programmable DC load-line mechanism is an integral part of the regulator's output voltage feedback compensator. This is illustrated in the feedback circuit and recommended compensation network shown in Figure 30.

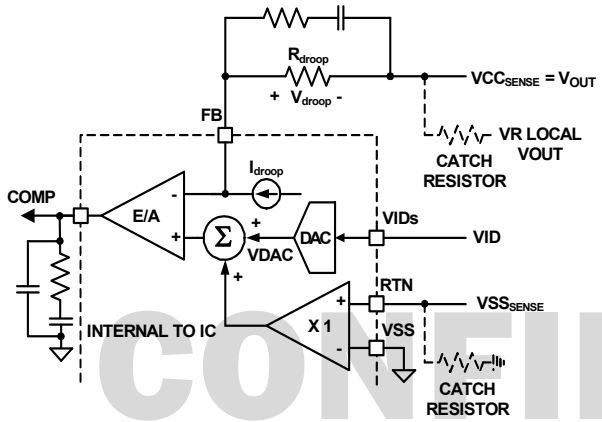


FIGURE 30. DIFFERENTIAL-VOLTAGE SENSING AND LOAD-LINE IMPLEMENTATION

The ISL95866 implements the DC load line by injecting a current, I_{droop}, which is proportional to the regulator output current I_{OUT}, into the voltage feedback node (the FB pin). The scaling of I_{droop} with respect to I_{OUT} was selected in the previous section to obtain the desired output I_{OCP} threshold. The droop voltage is the voltage drop across the resistance, called R_{droop}, between the FB pin and the output voltage due to I_{droop}. (R_{droop} is the only DC path between V_{OUT} and the FB pin.) R_{droop} is selected to implement the desired DC load line resistance R_{LL}. The FB pin voltage is thus raised above V_{OUT} by the droop voltage, requiring the regulator to reduce V_{OUT} to make V_{FB} equal to the voltage regulator reference voltage applied to the error amplifier noninverting input.

R_{droop} is a component of the voltage regulator stability compensation network. The regulator stability and dynamic response is determined independently of the value of R_{droop}, since the loop integral gain is set with the COMP-to-FB capacitance and the series-RC in parallel with R_{droop} will dominate the compensator response at and well below the open loop crossover frequency. Since R_{droop} plays a singular role in determining the DC load line, it is chosen solely for that purpose.

For a desired R_{LL}, the output voltage reduction, V_{droop}, due to an output load current, I_o, is as shown in Equation 35.

$$V_{droop} = R_{LL} \times I_o \quad \text{(EQ. 35)}$$

The value of V_{droop} obtained from the ISL95866 controller is the droop current, I_{droop}, multiplied by the droop resistor, R_{droop}. Using Equation 33, this value is as shown in Equation 36.

$$V_{droop} = I_{droop} \times R_{droop} = \frac{\rho_o}{R_i} \times I_o \times R_{droop} \quad \text{(EQ. 36)}$$

Equate these two expressions for V_{droop} and solve for R_{droop} to obtain the value in Equation 37.

$$R_{droop} = \frac{R_i \times R_{LL}}{\rho_o} \quad \text{(EQ. 37)}$$

PHASE DC VOLTAGE AND CURRENT BALANCING

To equally distribute power dissipation between the active phases of a VR, the controller provides a means to reduce the deviation of the DC component (approximately the product of the duty cycle and V_{VIN}) of each phase voltage from the average of all phases' DC voltages. The controller achieves phase node DC voltage balance by continually trimming the modulator slave circuits to match the ISEN*n* pin voltages. The connection of these pins to their respective phase nodes is depicted in Figure 31 for the inductor DCR current-sense method, for the example of a three phase VR. The DC voltage and current balancing methods described in this section apply also to current sensing using discrete sense resistors.

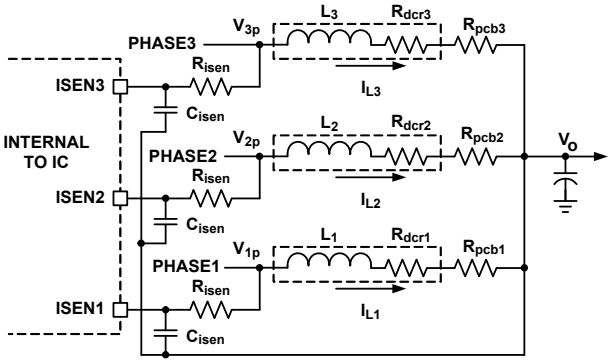


FIGURE 31. DUTY CYCLE BALANCING CIRCUIT

The phase nodes have high amplitude square-wave voltage waveforms, for which the DC component is indicative of each phase's relative contribution to the output. R_{isen} and C_{isen} form low-pass filters to remove the switching ripple of the phase node voltages, such that the voltages at the ISEN*n* pins approximately indicate each phase's DC voltage component and thus the relative contribution of each phase to the output current. The controller gradually and continually trims the R3™ modulator slave circuits. Thus, adjusting the relative duty cycle of each phase to reduce the phase node DC voltage differences, as indicated by each V_{ISENn}. This adjustment occurs slowly compared to the dynamic response of the multiphase modulator to output voltage commands, load transients, power state changes, and other system perturbations.

It is recommended to use a large R_{isen} and C_{isen} time constant, such that the ISEN*n* voltages have small ripple and are representative of the average or steady-state contribution of each phase to the output. Recommended values are R_{isen} = 10kΩ and C_{isen} = 0.22µF.

Ideally, balancing the phase nodes' average (DC) voltages will also balance the output current provided by each phase and thus the power dissipated in each phase's components. This is the case if the current-sense elements of each phase are identical (DCR of the inductors, or discrete current-sense resistors and the

associated current-sense networks) and if parasitic resistances of the circuit board traces from the sense connections to the common output voltage node are identical. Figure 31 shows the printed circuit trace resistances from each phase to the common output node. If these trace resistances are all equal, then the ideal of phase current balance is achieved with this design. This balance assumes the inductors and other current-sense components are identical, comparing each phase to the others, a true assumption within the published tolerance of component parameters.

Figure 31 includes the trace-resistance from each inductor to a single common output node, but not from the MOSFET switches to the inductor. This is correct assuming that each R_{isen} connection (V_{1p}, V_{2p} and V_{3p}) is routed directly to its respective inductor phase-node-side pad in order to eliminate the effect of phase node parasitic PCB resistance from the switching elements to the inductor. Equations 38 through 40 give the ISEN pin voltages:

$$V_{ISEN1} = (R_{dcr1} + R_{pcb1}) \times I_{L1} + Vo \quad \text{(EQ. 38)}$$

$$V_{ISEN2} = (R_{dcr2} + R_{pcb2}) \times I_{L2} + Vo \quad \text{(EQ. 39)}$$

$$V_{ISEN3} = (R_{dcr3} + R_{pcb3}) \times I_{L3} + Vo \quad \text{(EQ. 40)}$$

where R_{dcr1}, R_{dcr2}, and R_{dcr3} are the respective inductor DCRs, R_{pcb1}, R_{pcb2}, and R_{pcb3} are the respective parasitic PCB resistances between the inductor output-side pad and the output voltage rail; and I_{L1}, I_{L2}, and I_{L3} are inductor average currents.

The phase balance controller will adjust the phase pulse-width relative to the other phases to make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, thus obtaining $I_{L1} = I_{L2} = I_{L3}$ if $R_{dcr1} = R_{dcr2} = R_{dcr3}$, and $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

Since using the same components for L1, L2, and L3 will typically provide a good match of R_{dcr1}, R_{dcr2}, and R_{dcr3}, board layout will determine R_{pcb1}, R_{pcb2}, and R_{pcb3} and thus the matching of current per phase. It is recommended to have symmetrical layout for the power delivery path between each inductor and the output voltage rail, such that $R_{pcb1} = R_{pcb2} = R_{pcb3}$.

While careful symmetrical layout of the circuit board can achieve very good matching of these trace resistances, such layout is often difficult to achieve in practice. If trace resistances differ, then exact matching the phases' DC voltages will result in the imbalance of the phase currents. A modification of this circuit (to couple the signals of all the phases in the ISEN*n* networks) can correct the current imbalance due to unequal trace resistances to the output.

For the example case of a 3-phase configuration, Figure 32 shows the phase balancing circuit with the recommended trace-resistance imbalance correction. As before, V_{1p}, V_{2p}, and V_{3p} should be routed to their respective inductor phase-node-side pads in order to eliminate the effect of phase node parasitic PCB resistance from the switching elements to each inductor. The sensing traces for V_{1n}, V_{2n}, and V_{3n} should be routed to the V_{OUT} output-side inductor pads so they sense the voltage due only to the voltage drop across the inductor DCR and not due to the PCB trace resistance.

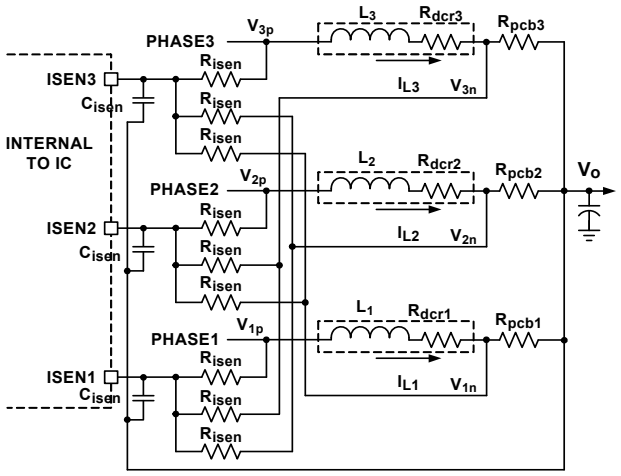


FIGURE 32. DIFFERENTIAL-SENSING CURRENT BALANCING CIRCUIT

Each ISEN pin sees the average voltage of three sources: its own phase inductor phase-node pad and the other two phases inductor output-side pads. Equations 41 through 43 give the ISEN pin voltages:

$$V_{ISEN1} = \frac{(V_{1p} + V_{2n} + V_{3n})}{3} \quad \text{(EQ. 41)}$$

$$V_{ISEN2} = \frac{(V_{1n} + V_{2p} + V_{3n})}{3} \quad \text{(EQ. 42)}$$

$$V_{ISEN3} = \frac{(V_{1n} + V_{2n} + V_{3p})}{3} \quad \text{(EQ. 43)}$$

The controller will make $V_{ISEN1} = V_{ISEN2} = V_{ISEN3}$, resulting in the equalities shown in Equations 44 and 45:

$$V_{1p} + V_{2n} + V_{3n} = V_{1n} + V_{2p} + V_{3n} \quad \text{(EQ. 44)}$$

$$V_{1n} + V_{2p} + V_{3n} = V_{1n} + V_{2n} + V_{3p} \quad \text{(EQ. 45)}$$

Simplifying Equation 44 gives Equation 46:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} \quad \text{(EQ. 46)}$$

and simplifying Equation 45 gives Equation 47:

$$V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 47)}$$

Combining Equations 46 and 47 gives Equation 48:

$$V_{1p} - V_{1n} = V_{2p} - V_{2n} = V_{3p} - V_{3n} \quad \text{(EQ. 48)}$$

which produces the desired result in Equation 49:

$$R_{dcr1} \times I_{L1} = R_{dcr2} \times I_{L2} = R_{dcr3} \times I_{L3} \quad \text{(EQ. 49)}$$

Current balancing ($I_{L1} = I_{L2} = I_{L3}$) is achieved independently of any mismatch of R_{pcb1}, R_{pcb2}, and R_{pcb3}, to within the tolerance of the resistance of the current-sense elements. Note that with the cross coupling of Figure 33, the phase balancing circuit no longer equalizes the average voltage of the phase nodes, but rather equalizes the DC components of the voltage drops across the current-sense elements.

Small absolute differences in PCB trace resistance from the inductors to the common output node can result in significant phase current imbalance. It is strongly recommended that the resistor pads and connections for the cross-coupling current balancing method be included in any PCB layout. The decision to include the additional Nx(N-1) trace-resistance correcting resistors can then be deferred until the extent of the current imbalance is measured on a functioning circuit. Considerations for making this decision are described in "Phase Current Balancing" on page 31.

With the ISEN*n* phase balancing mechanism (with cross-coupling resistors if needed, or without if not needed), the R3™ modulator achieves excellent current balancing during both steady state and transient operation. Figure 33 shows current balancing performance of an evaluation board with load transient of 12A/51A at different rep rates. The inductor currents follow the load current dynamic change with the output capacitors supplying the difference. The inductor currents can track the load current well at a low rep rate, but cannot track the load when the rep rate gets into the 100kHz range, which is outside of the control loop bandwidth. Regardless, the controller achieves excellent current *balancing* in all cases.

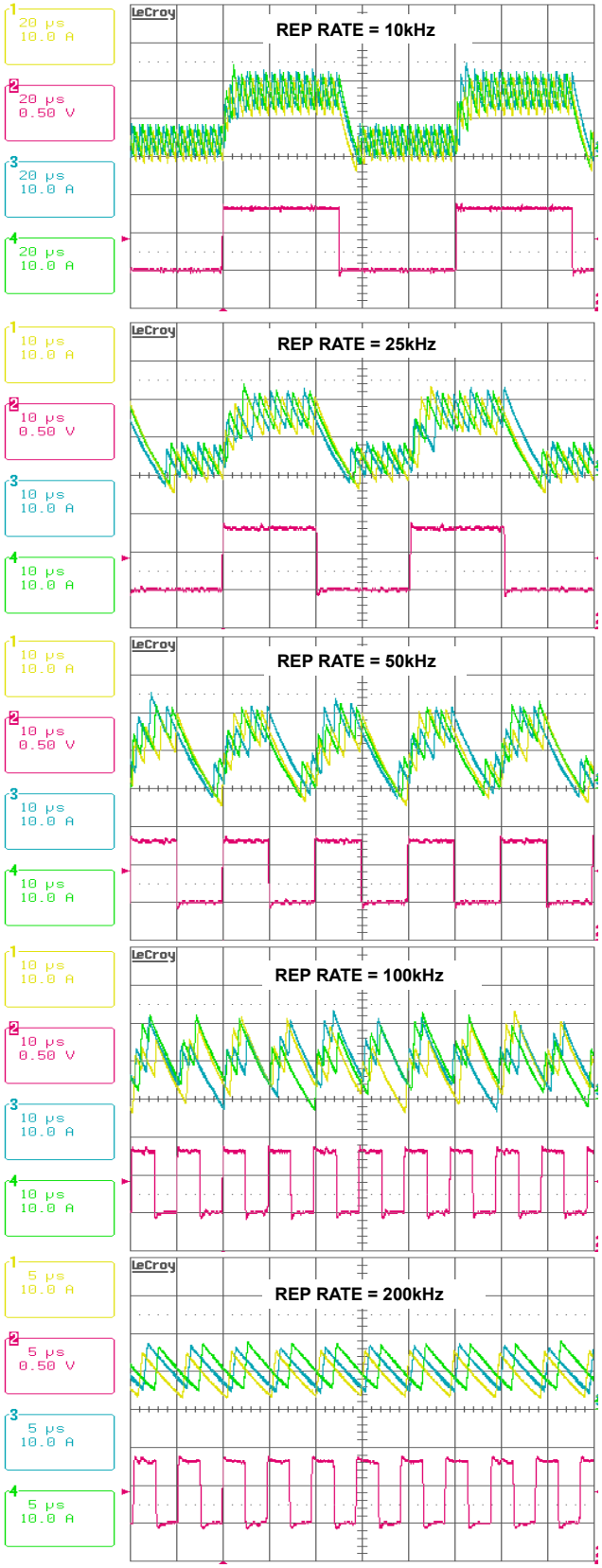


FIGURE 33. CURRENT BALANCING DURING DYNAMIC OPERATION. CH1: I_{L1}, CH2: I_{LOAD}, CH3: I_{L2}, CH4: I_{L3}

Current-Sense Circuit Adjustments

Once a Voltage Regulator, VR, is designed and a functional prototype has been assembled, adjustments may be necessary to correct for non-ideal components or assembly and printed circuit board parasitic effects. These are effects that are usually not known until the design has been realized. The following adjustments should be considered when refining a product design.

VERIFICATION OF INDUCTOR DCR CURRENT-SENSE POLE-ZERO MATCHING

Recall that if the inductor DCR is used as the phase current-sense element, it is necessary to select the capacitor C_n such that the current-sense transfer function pole at ω_{sns}, matches the zero at ω_L. The ideal response to a load step, with DC load line (i.e., "droop") enabled, is shown in Figure 34.

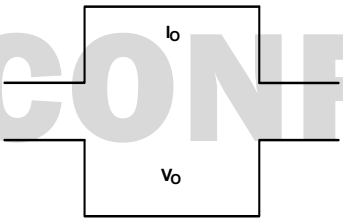


FIGURE 34. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

Figure 35 shows the load step transient response when C_n is too large. V_{CORE} droop response (rising or falling) lags in settling to its final value.

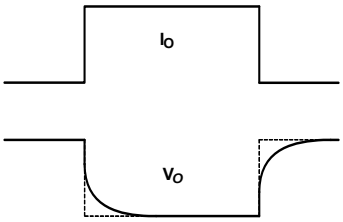


FIGURE 35. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO LARGE

Figure 36 shows the load step response when C_n is too small.

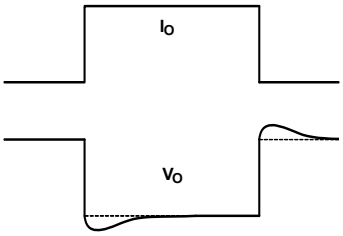


FIGURE 36. LOAD TRANSIENT RESPONSE WHEN C_n IS TOO SMALL

V_{CORE} response is underdamped and overshoots before settling to its final voltage.

Once the regulator design is complete, the measured load step response is compared to Figures 34 through 36. C_n should be adjusted if necessary to obtain the behavior of Figure 34.

CURRENT-SENSE SENSITIVITY ERROR

The current sense, IMON, and DC load line (droop) network component values should be designed according to the instructions in "Programming of Output Overcurrent Protection, I_{droop} and IMON" on page 26 and "Programming the DC Load Line" on page 26. This will ensure the correct *ratio* of V_{IMON} to I_{droop} (which determines R_{LL}) for the chosen system design parameters, for which no adjustment should be required. However, testing of the resulting circuit may reveal a measurement *sensitivity* error factor, which should effect V_{IMON} and I_{droop} equally. This error may be seen as a too-large R_{LL} value (droop voltage per load current) and as a too-large IMON voltage for a given load current. A single component modification will correct both errors.

The current-sense resistance value per phase (either a discrete sense resistor, or the inductor DCR) is typically very small, on the order of 1mΩ. The solder connections used in the assembly of such sense elements may contribute significant resistance to these sense elements, resulting in a larger load-dependent voltage drop than due to the sense element alone. Thus, the sensed output current value is greater than intended for a given load current. If this is the case, then the value of R_i (the ISUMN pin resistor) should be increased by the factor of the sensitivity error. For example, if the current-sense value is 3% larger than intended, then R_i should be increased by 3%. Changing R_i will change the sensitivity, with respect to I_{OUT}, of V_{IMON} and I_{droop} by the same factor, thus simultaneously correcting the IMON voltage error and the load line resistance, while preserving the intended ratio between the two parameters.

Note that the assembly procedure for installing the current-sense elements (sense resistors or inductors) can have a significant impact on the effective total resistance of each sense element. It is important that any adjustments to R_i be performed on circuits that have been assembled with the same procedures that will be used in mass production. The current measurement sensitivity error should be determined on a sufficient number of samples to avoid adjusting sensitivity to correct what may be a component-tolerance outlier.

DCR CURRENT SENSE OFFSET ERROR

When using the inductor DCR current-sensing, nonlinearity of the R_{SUM} resistors can induce a small positive offset in the ISUMP voltage and thus, in the IMON pin current (viewed as a positive offset in the ICC register value) and also in the droop current (viewed as an output voltage negative offset). The offset error occurs as follows: for each inductor, the instantaneous voltage across its R_{SUM} resistor is approximately $V_{RSUM} = V_{PHASE} - V_{VOUT}$. During that phase's on time, $V_{PHASE} = V_{VIN}$, giving $V_{RSUM-ON} = V_{VIN} - V_{VOUT}$. During the off time, V_{PHASE} = 0V and so $V_{RSUM-OFF} = -V_{VOUT}$. For the example of V_{VOUT} = 1.8V and V_{VIN} = 12V, $V_{RSUM-ON}$ = 10.2V, and $V_{RSUM-OFF}$ = –1.8V, a sign-dependent magnitude difference exceeding 8V. Inexpensive thick film resistors can have a voltage nonlinearity of 25ppm/volt or more, with the device resistance decreasing with increasing voltage. Because of this R_{SUM} resistor nonlinearity, each R_{SUM}'s (positive) current into the common ISUMP node (during its on-time) is biased slightly greater than the nominal V/R value expected. Each R_{SUM}'s (negative) current (during its off-time) will also be biased negatively due to the

resistor nonlinearity, but less so because the R_{SUM} voltage magnitude is always much less during the off-time than during the on-time. This nonlinearity bias-current polarity mismatch causes a small positive offset error in V_{ISUMP}. Note that this offset error will not occur if using discrete resistors as current-sense elements.

The exact magnitude of this offset error is difficult to predict. It depends on an attribute of the sense resistors that is typically not specified or controlled and so not reliably quantified. It also varies with the input voltage and the output voltage. If battery powered, the input voltage can vary significantly. The output voltage is subject to the VID setting and to a lesser extent on the droop voltage. A further complication is that the nonlinearity offset changes with the number of active phases. For a 3-phase configuration in PS0, three R_{SUM} resistors are subjected to the high difference in on-time compared to off-time voltage magnitudes. But in PS1, one or two phases are disabled (based on PROG2 setting) with the respective PHASE nodes approximately following the output. Thus, V_{RSUM} for the disabled phases is approximately zero for the entire switching cycle, reducing the offset error by 1/3 to 2/3. In PS2, only one phase is active and two phases are disabled, leaving only a third of the PS0 offset error.

The most direct solution to the phenomenon of current-sense offset due to resistor nonlinearity is to use highly linear summing resistors, such as thin film resistors. But the magnitude of the offset error typically does not warrant the considerably greater expense of doing so. Instead, a correcting fixed offset is introduced to the current-sense network.

For the example case described, with each thick film R_{SUM} = 3.65kΩ and an $I_{CC(MAX)}$ setting of 100A, the current-sense offset error in PS0 typically represents less than 1% of full-scale and is always positive. It has been found empirically that a 10MΩ pull-down resistor, from the ISUMP node to ground, provides a good correcting offset compromise slightly undercorrecting in PS0 and slightly overcorrecting in PS2, however meeting processor vendor specification tolerances with adequate margin in all cases. For other applications, a suitable compromise pull-down resistor is determined empirically by testing over the full range of expected operating conditions and power states. It is recommended that this resistor be included in any VR design layout to allow population of the pull-down resistor if required. Because of the high value of resistance, two smaller valued resistors in series may be preferred, to reduce the environmental sensitivity of high resistance value devices.

PHASE CURRENT BALANCING

Phase current imbalance should be measured on a functioning circuit. First verify the correct assembly of the current balancing mechanism by measuring, on a stable operating regulator, the voltage difference between the ISEN1 pin and the remaining ISEN*n* pins (of all the operational phases) with various static loads applied. Whether using the simple circuit of Figure 31, or the PCB trace resistance compensating circuit of Figure 32, the voltage difference between any pair of the ISEN*n* pins should be very small, usually less than 1mV. If not, there may be an assembly error.

Then, again with various static loads applied, measure the voltage directly across each active sense element (sense resistor or inductor). Any discrepancy in the phase sense element voltages beyond what are attributed to the sense element resistance tolerance must be due to PCB trace resistance deviations. Install the cross-coupling resistors of Figure 37 and again compare the sense element voltages. Now the sense element voltages should be the same among the phases in all cases (to within the tolerance of the cross-coupling resistors) and the phase current balance is within the parametric tolerance of the sense element resistance, independently of the PCB trace resistance differences.

The decision to populate the cross-coupling phase sense resistors will depend upon the magnitude and system tolerance of the uncorrected imbalance current.

LOAD STEP RINGBACK

Figure 37 shows the output voltage ringback problem during load transient response with DC load line (i.e., “droop”) enabled. The load current I_O has a fast step change, but the inductor current I_L cannot accurately follow. Instead, I_L responds in first order system fashion due to the nature of current loop. The ESR and ESL effect of the output capacitors makes the output voltage V_O dip quickly upon load current change. However, the controller regulates V_O according to the droop current i_{droop}, which is a real-time representation of I_L. Therefore it pulls V_O back to the level dictated by I_L, causing the ringback problem. This phenomenon is not observed when the output capacitor bank has very low ESR and ESL, such as if using only ceramic capacitors.

Figure 38 shows two optional circuits for reduction of the ringback.

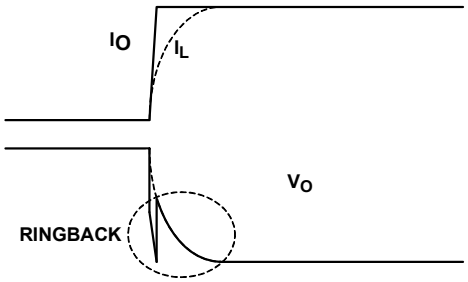


FIGURE 37. OUTPUT VOLTAGE RINGBACK PROBLEM

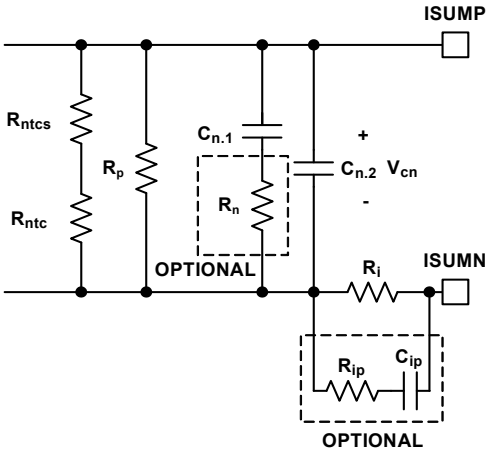


FIGURE 38. OPTIONAL CIRCUITS FOR RINGBACK REDUCTION

C_n is the capacitor used to match the inductor time constant. It often takes the paralleling of multiple capacitors to get the desired value. Figure 38 shows that two capacitors $C_{n.1}$ and $C_{n.2}$ are in parallel. Resistor R_n is an optional component to reduce the V_o ring back. At steady state, $C_{n.1} + C_{n.2}$ provides the desired C_n capacitance. At the beginning of i_o change, the effective capacitance is less because R_n increases the impedance of the $C_{n.1}$ branch. As Figure 36 on page 30 shows, V_o tends to dip when C_n is too small and this effect will reduce the V_o ringback. This effect is more pronounced when $C_{n.1}$ is much larger than $C_{n.2}$. It is also more pronounced when R_n is bigger. However, the presence of R_n increases the ripple of the V_n signal if $C_{n.2}$ is too small. It is recommended to keep $C_{n.2}$ greater than 2200pF. R_n value usually is a few ohms. $C_{n.1}$, $C_{n.2}$, and R_n values should be determined through tuning the load transient response waveforms directly on the target system circuit board.

R_{ip} and C_{ip} form an R-C branch in parallel with R_i, providing a lower impedance path than R_i at the beginning of I_{OUT} change. R_{ip} and C_{ip} do not have any effect at steady state. Through proper selection of R_{ip} and C_{ip} values, I_{droop} can more closely resemble I_{OUT} rather than i_L and V_o will not ring back. The recommended value for R_{ip} is 100Ω. C_{ip} should be determined by observing the load transient response waveforms in a physical circuit. The recommended range for C_{ip} is 100pF~2000pF. However, it should be noted that the R_{ip}-C_{ip} branch may distort the I_{droop} waveform. Instead of being triangular as the real inductor current, I_{droop} may have sharp spikes, which may adversely affect I_{droop} average value detection and therefore may affect OCP accuracy.

Compensator

Intersil provides a Microsoft Excel-based spreadsheet to help design the compensator and the current-sensing network for each output of the ISL95866. The spreadsheet helps in designing each VR to achieve constant output impedance as a stable system. Please go to www.intersil.com/en/support to request the spreadsheet for the ISL95866.

A VR with active droop function is a dual-loop system consisting of a voltage loop and a droop loop, which is a current loop. However, neither loop alone is sufficient to describe the entire system. The spreadsheet shows two loop gain transfer functions, T1(s) and T2(s), that describe the entire system. Figure 39 conceptually shows T1(s) measurement setup and Figure 40 conceptually shows T2(s) measurement setup. The VR senses the inductor current, multiplies it by a gain of the load line slope, then adds it on top of the sensed output voltage and feeds it to the compensator. T1(s) is measured after the summing node and T2(s) is measured in the voltage loop before the summing node. The spreadsheet gives both T1(s) and T2(s) plots. However, only T2(s) is actually measured on an ISL95866 regulator.

T1(s) is the total loop gain of the voltage loop and the droop loop. It always has a higher crossover frequency than T2(s) and has more impact on system stability.

T2(s) is the voltage loop gain with closed droop loop. It has more impact on output voltage response.

Design the compensator to get stable T1(s) and T2(s) with sufficient phase margin and output impedance equal or smaller than the load-line slope.

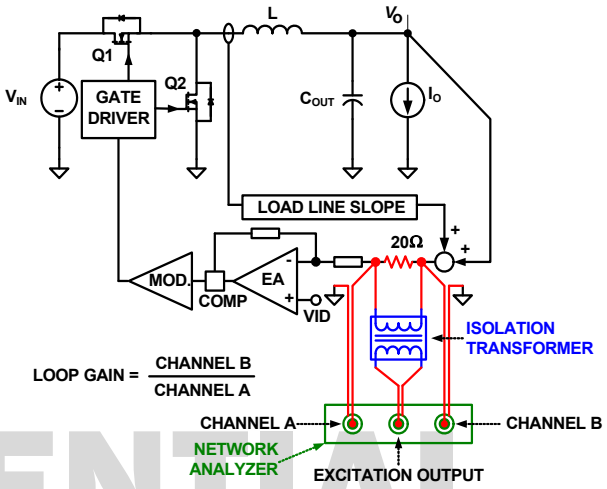


FIGURE 39. LOOP GAIN T1(s) MEASUREMENT SETUP

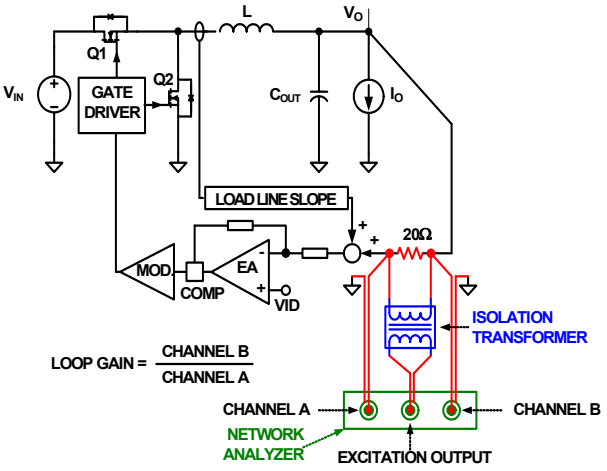


FIGURE 40. LOOP GAIN T2(s) MEASUREMENT SET-UP

Voltage Regulation

After the start-up sequence, the controller regulates the two output voltages to the value set by the VID information per Table 7 on page 33. The controller will control the no-load output voltages to an accuracy of ±0.5% over the VID voltage range. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die.

This mechanism is illustrated in Figure 30 on page 27. The VCC_{SENSE} and VSS_{SENSE} are the remote voltage sensing signals from the processor die. A unity gain differential amplifier senses the VSS_{SENSE} voltage and adds it to the DAC output. Note how the illustrated DC load line mechanism (the "droop" mechanism, described in "Programming the DC Load Line" on page 26), introduces a load-dependent reduction in the output voltage, (denoted VCC_{SENSE}), below the VID value output by the DAC. The error amplifier regulates the inverting and the non-inverting input voltages to be equal, as shown in Equation 50:

$$VCC_{SENSE} + V_{droop} = V_{DAC} + VSS_{SENSE} \quad \text{(EQ. 50)}$$

Rewriting Equation 50 and substitution of Equation 36 gives Equation 51:

$$VCC_{SENSE} - VSS_{SENSE} = V_{DAC} - R_{droop} \times I_{droop} \quad \text{(EQ. 51)}$$

Equation 51 is the ideal relationship required for load-line implementation.

The VCC_{SENSE} and VSS_{SENSE} signals are sensed at the processor die. The feedback is open circuit in the absence of the processor. As shown in Figure 30 on page 27, it is recommended to add a "catch" resistor to feed the VR local output voltage back to the compensator and add another "catch" resistor to connect the VR local output ground to the RTN pin. These resistors, typically 10Ω~100Ω, will provide voltage feedback if the system is powered up without a processor installed.

VID Table

After the start-up sequence, the controller regulates the output voltage to the value set by the VID information per Table 7. The controller will control the no load output voltage to an accuracy of ±0.5% over the VID voltage range. A differential amplifier allows voltage sensing for precise voltage regulation at the microprocessor die. The maximum VID is set as 1.52V.

TABLE 7. VID TABLE

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	0	0	0	0	0	0	0	0	0	0.00000
0	0	0	0	0	0	0	1	0	1	0.25000
0	0	0	0	0	0	1	0	0	2	0.25500
0	0	0	0	0	0	1	1	0	3	0.26000
0	0	0	0	0	1	0	0	0	4	0.26500
0	0	0	0	0	1	0	1	0	5	0.27000
0	0	0	0	0	1	1	0	0	6	0.27500
0	0	0	0	0	1	1	1	0	7	0.28000

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	0	0	0	1	0	0	0	0	8	0.28500
0	0	0	0	1	0	0	1	0	9	0.29000
0	0	0	0	1	0	1	0	0	A	0.29500
0	0	0	0	1	0	1	1	0	B	0.30000
0	0	0	0	1	1	0	0	0	C	0.30500
0	0	0	0	1	1	0	1	0	D	0.31000
0	0	0	0	1	1	1	0	0	E	0.31500
0	0	0	0	1	1	1	1	0	F	0.32000
0	0	0	1	0	0	0	0	1	0	0.32500
0	0	0	1	0	0	0	1	1	1	0.33000
0	0	0	1	0	0	1	0	1	2	0.33500
0	0	0	1	0	0	1	1	1	3	0.34000
0	0	0	1	0	1	0	0	1	4	0.34500
0	0	0	1	0	1	0	1	1	5	0.35000
0	0	0	1	0	1	1	0	1	6	0.35500
0	0	0	1	0	1	1	1	1	7	0.36000
0	0	0	1	1	0	0	0	1	8	0.36500
0	0	0	1	1	0	0	1	1	9	0.37000
0	0	0	1	1	0	1	0	1	A	0.37500
0	0	0	1	1	0	1	1	1	B	0.38000
0	0	0	1	1	1	0	0	1	C	0.38500
0	0	0	1	1	1	0	1	1	D	0.39000
0	0	0	1	1	1	1	0	1	E	0.39500
0	0	0	1	1	1	1	1	1	F	0.40000
0	0	1	0	0	0	0	0	2	0	0.40500
0	0	1	0	0	0	0	1	2	1	0.41000
0	0	1	0	0	0	1	0	2	2	0.41500
0	0	1	0	0	0	1	1	2	3	0.42000
0	0	1	0	0	1	0	0	2	4	0.42500
0	0	1	0	0	1	0	1	2	5	0.43000
0	0	1	0	0	1	1	0	2	6	0.43500
0	0	1	0	0	1	1	1	2	7	0.44000
0	0	1	0	1	0	0	0	2	8	0.44500
0	0	1	0	1	0	0	1	2	9	0.45000
0	0	1	0	1	0	1	0	2	A	0.45500
0	0	1	0	1	0	1	1	2	B	0.46000
0	0	1	0	1	1	0	0	2	C	0.46500
0	0	1	0	1	1	0	1	2	D	0.47000
0	0	1	0	1	1	1	0	2	E	0.47500
0	0	1	0	1	1	1	1	2	F	0.48000
0	0	1	1	0	0	0	0	3	0	0.48500
0	0	1	1	0	0	0	1	3	1	0.49000
0	0	1	1	0	0	1	0	3	2	0.49500
0	0	1	1	0	0	1	1	3	3	0.50000
0	0	1	1	0	1	0	0	3	4	0.50500

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	0	1	1	0	1	0	1	3	5	0.51000
0	0	1	1	0	1	1	0	3	6	0.51500
0	0	1	1	0	1	1	1	3	7	0.52000
0	0	1	1	1	0	0	0	3	8	0.52500
0	0	1	1	1	0	0	1	3	9	0.53000
0	0	1	1	1	0	1	0	3	A	0.53500
0	0	1	1	1	0	1	1	3	B	0.54000
0	0	1	1	1	1	0	0	3	C	0.54500
0	0	1	1	1	1	0	1	3	D	0.55000
0	0	1	1	1	1	1	0	3	E	0.55500
0	0	1	1	1	1	1	1	3	F	0.56000
0	1	0	0	0	0	0	0	4	0	0.56500
0	1	0	0	0	0	0	1	4	1	0.57000
0	1	0	0	0	0	1	0	4	2	0.57500
0	1	0	0	0	0	1	1	4	3	0.58000
0	1	0	0	0	1	0	0	4	4	0.58500
0	1	0	0	0	1	0	1	4	5	0.59000
0	1	0	0	0	1	1	0	4	6	0.59500
0	1	0	0	0	1	1	1	4	7	0.60000
0	1	0	0	1	0	0	0	4	8	0.60500
0	1	0	0	1	0	0	1	4	9	0.61000
0	1	0	0	1	0	1	0	4	A	0.61500
0	1	0	0	1	0	1	1	4	B	0.62000
0	1	0	0	1	1	0	0	4	C	0.62500
0	1	0	0	1	1	0	1	4	D	0.63000
0	1	0	0	1	1	1	0	4	E	0.63500
0	1	0	0	1	1	1	1	4	F	0.64000
0	1	0	1	0	0	0	0	5	0	0.64500
0	1	0	1	0	0	0	1	5	1	0.65000
0	1	0	1	0	0	1	0	5	2	0.65500
0	1	0	1	0	0	1	1	5	3	0.66000
0	1	0	1	0	1	0	0	5	4	0.66500
0	1	0	1	0	1	0	1	5	5	0.67000
0	1	0	1	0	1	1	0	5	6	0.67500
0	1	0	1	0	1	1	1	5	7	0.68000
0	1	0	1	1	0	0	0	5	8	0.68500
0	1	0	1	1	0	0	1	5	9	0.69000
0	1	0	1	1	0	1	0	5	A	0.69500
0	1	0	1	1	0	1	1	5	B	0.70000
0	1	0	1	1	1	0	0	5	C	0.70500
0	1	0	1	1	1	0	1	5	D	0.71000
0	1	0	1	1	1	1	0	5	E	0.71500
0	1	0	1	1	1	1	1	5	F	0.72000
0	1	1	0	0	0	0	0	6	0	0.72500
0	1	1	0	0	0	0	1	6	1	0.73000

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
0	1	1	0	0	0	1	0	6	2	0.73500
0	1	1	0	0	0	1	1	6	3	0.74000
0	1	1	0	0	1	0	0	6	4	0.74500
0	1	1	0	0	1	0	1	6	5	0.75000
0	1	1	0	0	1	1	0	6	6	0.75500
0	1	1	0	0	1	1	1	6	7	0.76000
0	1	1	0	1	0	0	0	6	8	0.76500
0	1	1	0	1	0	0	1	6	9	0.77000
0	1	1	0	1	0	1	0	6	A	0.77500
0	1	1	0	1	0	1	1	6	B	0.78000
0	1	1	0	1	1	0	0	6	C	0.78500
0	1	1	0	1	1	0	1	6	D	0.79000
0	1	1	0	1	1	1	0	6	E	0.79500
0	1	1	0	1	1	1	1	6	F	0.80000
0	1	1	1	0	0	0	0	7	0	0.80500
0	1	1	1	0	0	0	1	7	1	0.81000
0	1	1	1	0	0	1	0	7	2	0.81500
0	1	1	1	0	0	1	1	7	3	0.82000
0	1	1	1	0	1	0	0	7	4	0.82500
0	1	1	1	0	1	0	1	7	5	0.83000
0	1	1	1	0	1	1	0	7	6	0.83500
0	1	1	1	0	1	1	1	7	7	0.84000
0	1	1	1	1	0	0	0	7	8	0.84500
0	1	1	1	1	0	0	1	7	9	0.85000
0	1	1	1	1	0	1	0	7	A	0.85500
0	1	1	1	1	0	1	1	7	B	0.86000
0	1	1	1	1	1	0	0	7	C	0.86500
0	1	1	1	1	1	0	1	7	D	0.87000
0	1	1	1	1	1	1	0	7	E	0.87500
0	1	1	1	1	1	1	1	7	F	0.88000
1	0	0	0	0	0	0	0	8	0	0.88500
1	0	0	0	0	0	0	1	8	1	0.89000
1	0	0	0	0	0	1	0	8	2	0.89500
1	0	0	0	0	0	1	1	8	3	0.90000
1	0	0	0	0	1	0	0	8	4	0.90500
1	0	0	0	0	1	0	1	8	5	0.91000
1	0	0	0	0	1	1	0	8	6	0.91500
1	0	0	0	0	1	1	1	8	7	0.92000
1	0	0	0	1	0	0	0	8	8	0.92500
1	0	0	0	1	0	0	1	8	9	0.93000
1	0	0	0	1	0	1	0	8	A	0.93500
1	0	0	0	1	0	1	1	8	B	0.94000
1	0	0	0	1	1	0	0	8	C	0.94500
1	0	0	0	1	1	0	1	8	D	0.95000
1	0	0	0	1	1	1	0	8	E	0.95500

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	0	0	0	1	1	1	1	8	F	0.96000
1	0	0	1	0	0	0	0	9	0	0.96500
1	0	0	1	0	0	0	1	9	1	0.97000
1	0	0	1	0	0	1	0	9	2	0.97500
1	0	0	1	0	0	1	1	9	3	0.98000
1	0	0	1	0	1	0	0	9	4	0.98500
1	0	0	1	0	1	0	1	9	5	0.99000
1	0	0	1	0	1	1	0	9	6	0.99500
1	0	0	1	0	1	1	1	9	7	1.00000
1	0	0	1	1	0	0	0	9	8	1.00500
1	0	0	1	1	0	0	1	9	9	1.01000
1	0	0	1	1	0	1	0	9	A	1.01500
1	0	0	1	1	0	1	1	9	B	1.02000
1	0	0	1	1	1	0	0	9	C	1.02500
1	0	0	1	1	1	0	1	9	D	1.03000
1	0	0	1	1	1	1	0	9	E	1.03500
1	0	0	1	1	1	1	1	9	F	1.04000
1	0	1	0	0	0	0	0	A	0	1.04500
1	0	1	0	0	0	0	1	A	1	1.05000
1	0	1	0	0	0	1	0	A	2	1.05500
1	0	1	0	0	0	1	1	A	3	1.06000
1	0	1	0	0	1	0	0	A	4	1.06500
1	0	1	0	0	1	0	1	A	5	1.07000
1	0	1	0	0	1	1	0	A	6	1.07500
1	0	1	0	0	1	1	1	A	7	1.08000
1	0	1	0	1	0	0	0	A	8	1.08500
1	0	1	0	1	0	0	1	A	9	1.09000
1	0	1	0	1	0	1	0	A	A	1.09500
1	0	1	0	1	0	1	1	A	B	1.10000
1	0	1	0	1	1	0	0	A	C	1.10500
1	0	1	0	1	1	0	1	A	D	1.11000
1	0	1	0	1	1	1	0	A	E	1.11500
1	0	1	0	1	1	1	1	A	F	1.12000
1	0	1	1	0	0	0	0	B	0	1.12500
1	0	1	1	0	0	0	1	B	1	1.13000
1	0	1	1	0	0	1	0	B	2	1.13500
1	0	1	1	0	0	1	1	B	3	1.14000
1	0	1	1	0	1	0	0	B	4	1.14500
1	0	1	1	0	1	0	1	B	5	1.15000
1	0	1	1	0	1	1	0	B	6	1.15500
1	0	1	1	0	1	1	1	B	7	1.16000
1	0	1	1	1	0	0	0	B	8	1.16500
1	0	1	1	1	0	0	1	B	9	1.17000
1	0	1	1	1	0	1	0	B	A	1.17500
1	0	1	1	1	0	1	1	B	B	1.18000

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	0	1	1	1	1	0	0	B	C	1.18500
1	0	1	1	1	1	0	1	B	D	1.19000
1	0	1	1	1	1	1	0	B	E	1.19500
1	0	1	1	1	1	1	1	B	F	1.20000
1	1	0	0	0	0	0	0	C	0	1.20500
1	1	0	0	0	0	0	1	C	1	1.21000
1	1	0	0	0	0	1	0	C	2	1.21500
1	1	0	0	0	0	1	1	C	3	1.22000
1	1	0	0	0	1	0	0	C	4	1.22500
1	1	0	0	0	1	0	1	C	5	1.23000
1	1	0	0	0	1	1	0	C	6	1.23500
1	1	0	0	0	1	1	1	C	7	1.24000
1	1	0	0	1	0	0	0	C	8	1.24500
1	1	0	0	1	0	0	1	C	9	1.25000
1	1	0	0	1	0	1	0	C	A	1.25500
1	1	0	0	1	0	1	1	C	B	1.26000
1	1	0	0	1	1	0	0	C	C	1.26500
1	1	0	0	1	1	0	1	C	D	1.27000
1	1	0	0	1	1	1	0	C	E	1.27500
1	1	0	0	1	1	1	1	C	F	1.28000
1	1	0	1	0	0	0	0	D	0	1.28500
1	1	0	1	0	0	0	1	D	1	1.29000
1	1	0	1	0	0	1	0	D	2	1.29500
1	1	0	1	0	0	1	1	D	3	1.30000
1	1	0	1	0	1	0	0	D	4	1.30500
1	1	0	1	0	1	0	1	D	5	1.31000
1	1	0	1	0	1	1	0	D	6	1.31500
1	1	0	1	0	1	1	1	D	7	1.32000
1	1	0	1	1	0	0	0	D	8	1.32500
1	1	0	1	1	0	0	1	D	9	1.33000
1	1	0	1	1	0	1	0	D	A	1.33500
1	1	0	1	1	0	1	1	D	B	1.34000
1	1	0	1	1	1	0	0	D	C	1.34500
1	1	0	1	1	1	0	1	D	D	1.35000
1	1	0	1	1	1	1	0	D	E	1.35500
1	1	0	1	1	1	1	1	D	F	1.36000
1	1	1	0	0	0	0	0	E	0	1.36500
1	1	1	0	0	0	0	1	E	1	1.37000
1	1	1	0	0	0	1	0	E	2	1.37500
1	1	1	0	0	0	1	1	E	3	1.38000
1	1	1	0	0	1	0	0	E	4	1.38500
1	1	1	0	0	1	0	1	E	5	1.39000
1	1	1	0	0	1	1	0	E	6	1.39500
1	1	1	0	0	1	1	1	E	7	1.40000
1	1	1	0	1	0	0	0	E	8	1.40500

TABLE 7. VID TABLE (Continued)

VID								HEX		V_O (V)
7	6	5	4	3	2	1	0			
1	1	1	0	1	0	0	1	E	9	1.41000
1	1	1	0	1	0	1	0	E	A	1.41500
1	1	1	0	1	0	1	1	E	B	1.42000
1	1	1	0	1	1	0	0	E	C	1.42500
1	1	1	0	1	1	0	1	E	D	1.43000
1	1	1	0	1	1	1	0	E	E	1.43500
1	1	1	0	1	1	1	1	E	F	1.44000
1	1	1	1	0	0	0	0	F	0	1.44500
1	1	1	1	0	0	0	1	F	1	1.45000
1	1	1	1	0	0	1	0	F	2	1.45500
1	1	1	1	0	0	1	1	F	3	1.46000
1	1	1	1	0	1	0	0	F	4	1.46500
1	1	1	1	0	1	0	1	F	5	1.47000
1	1	1	1	0	1	1	0	F	6	1.47500
1	1	1	1	0	1	1	1	F	7	1.48000
1	1	1	1	1	0	0	0	F	8	1.48500
1	1	1	1	1	0	0	1	F	9	1.49000
1	1	1	1	1	0	1	0	F	A	1.49500
1	1	1	1	1	0	1	1	F	B	1.50000
1	1	1	1	1	1	0	0	F	C	1.50500
1	1	1	1	1	1	0	1	F	D	1.51000
1	1	1	1	1	1	1	0	F	E	1.51500
1	1	1	1	1	1	1	1	F	F	1.52000

The maximum VID (output voltage command) value supported is 1.52V. Any VID command (or sum of VID command and VID offset) above 2.3V is ignored.

Dynamic VID Operation

The ISL95866 receives VID commands via the Serial VID (SVID) port. It responds to VID changes by slewing to the new voltage at a slew rate indicated in the SetVID command. There are three SetVID slew rates: SetVID_fast, SetVID_slow, and SetVID_decay.

SetVID_fast command prompts the controller to enter PS0 and to actively drive the output voltage to the new VID value at the programmed fast slew rate.

SetVID_slow command prompts the controller to enter PS0 and to actively drive the output voltage to the new VID value at the programmed slow slew rate (1/2 of the fast slew rate).

SetVID_decay command prompts the controller to enter Power State PS2, with DEM (FCCM goes low). The output voltage will decay down to the new VID value at a slew rate determined by the load. If the voltage decay rate is too fast, the controller will limit the voltage slew rate to approximately -6mV/µs.

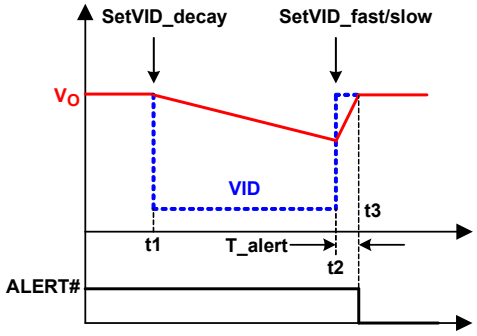


FIGURE 41. SETVID DECAY PREEMPTIVE BEHAVIOR

ALERT# is asserted (low) upon completion of all non-zero VID transitions. Figure 41 shows a SetVID Decay Preemptive response, which occurs whenever a new VID command is received before completion of a previous SetVID Decay command.

The example scenario of Figure 41 shows the controller receives a SetVID_decay command at t1. The VR enters DEM and the output voltage V_O decays down slowly. At t2, before V_O reaches the intended VID target of the SetVID_decay command, the controller receives a SetVID_fast (or SetVID_slow) command to go to a voltage higher than the actual V_O. The controller will preempt the decay to the lower voltage and slew V_O to the new target voltage at the slew rate specified by the SetVID command. At t3, V_O reaches the new target voltage and the controller asserts the ALERT# signal.

Slew Rate Compensation Circuit for VID Transition

In executing a SetVID command, the VID DAC steps through the VID table to the destination voltage at the specified step rate. For example, for a SetVID_fast command the DAC will step a minimum of six ticks (30mV minimum) per 1µs, for an output voltage slew rate of at least 30mV/µs. For a SetVID_slow command, the DAC step rate is a minimum of three ticks per 1µs, commanding output voltage slew rate of at least 15mV/µs. The actual slew rate is indicated in the "Electrical Specifications" on page 9. Figure 42 shows the waveforms of VID transition.

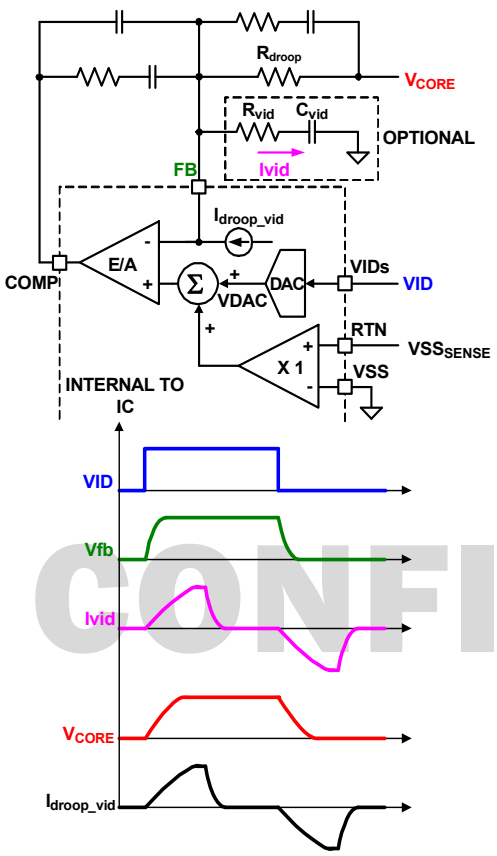


FIGURE 42. SLEW RATE COMPENSATION CIRCUIT FOR VID TRANSITION

During VID transition, the output capacitor is being charged and discharged, causing C_{out} x dV_{CORE}/dt current on the inductor. The controller senses the inductor current increase during the rising VID transition (as the I_{droop_vid} waveform shows) and will droop the output voltage V_{CORE} accordingly, adding damping to the V_{CORE} slew response. Similar behavior occurs during the falling VID transition. To improve V_{CORE} VID slew response, one can add the R_{vid}-C_{vid} branch, whose current I_{vid} compensates for I_{droop_vid}. Choose the R, C values from the reference design as a starting point, then adjust the actual values on the board to get the best performance.

Fault Protection

The ISL95866 provides overcurrent, current balance, and overvoltage fault protection on each VR output. The controller also provides over-temperature protection on both outputs.

The controller determines Overcurrent Protection (OCP) by comparing the average value of the droop current I_{droop} with an internal current source threshold listed in Table 2 on page 18 or Table 3 on page 19 depending on the output. It declares OCP when I_{droop} is above the threshold for 120µs, maximum. Note that the output circuitry must be able to survive an I_{OCP} violation for at least 120µs based on this maximum timing.

The controller monitors the ISEN pin voltages to determine current balance protection. If the difference of one ISEN pin voltage and the average ISENs pin voltage is greater than 9mV (for at most 4ms), the controller will declare a fault and latch off.

The controller takes the same actions for all of the above fault protections: deassertion of VR_READY and turn-off of all the high-side and low-side power MOSFETs. Any residual inductor current will decay through the MOSFET body diodes.

The controller will detect an Overvoltage Protection (OVP) fault if the voltage of the ISUMN pin (approximately the output voltage) exceeds the OVP threshold, which is the VID set value plus 300mV. When this happens, the controller will immediately declare an OV fault, deassert PGOOD and take action through the PWM signals to turn on the low-side power MOSFETs. The low-side power MOSFETs remain on until the output voltage is pulled down below the VID set value. If the output voltage rises above the OVP threshold voltage again, the protection process is repeated. This behavior provides the maximum amount of protection against shorted high-side power MOSFETs while preventing the output to ringing below ground.

The overvoltage fault threshold is 2.45V when output voltage ramps up from 0V during soft-start. The overvoltage fault threshold reverts to VID + 300mV after the output voltage settles to V_{BOOT}.

A fault on either ISL95866 voltage regulator output will result in both outputs being shut down. All the previously mentioned fault conditions are reset by bringing VR_ENABLE low or by bringing VDD below the POR threshold. When VR_ENABLE and VDD return to their high operating levels, the controller will soft-start both outputs.

Table 10 summarizes the fault protections.

TABLE 8. FAULT PROTECTION SUMMARY

FAULT TYPE	FAULT DURATION BEFORE PROTECTION	PROTECTION ACTION	FAULT RESET
Overcurrent	120µs (maximum)	PWM tri-state, VR_READY latched low	VR_ENABLE toggle or VDD toggle
Phase Current Unbalance	4ms		
Overvoltage: V_{OUT} > VID + 300mV	Immediate	VR_READY latched low. Actively pulls the output voltage to below VID value, then tri-state.	
2.45V Overvoltage During Output Voltage Ramp-Up from 0V During Soft-Start			

VR_HOT#/ALERT# Behavior

The controller drives a 10µA current source out of the NTC pin. The current source flows through an NTC resistor network connected from the NTC pin to GND and creates a voltage that is monitored by the controller. The NTC thermistor is placed at a thermal point on the motherboard that is the hottest point for the output stage. Typically, this will result in the NTC thermistor being located next to the MOSFETs of Channel 1 of the associated VR output.

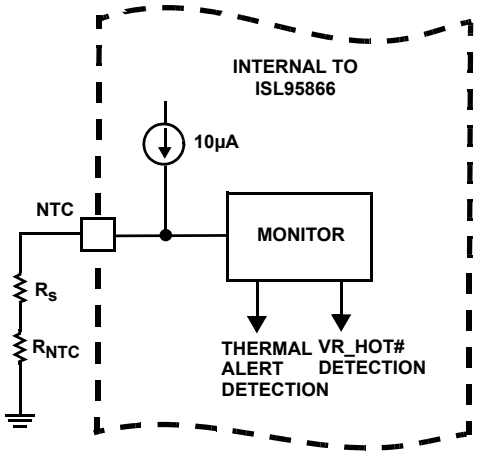


FIGURE 43. NTC CIRCUITRY

The NTC pin voltage will drop as board temperature rises and the thermistor resistance changes with the thermal increase at the point monitored. When the NTC pin voltage drops below the thermal alert trip threshold, see "Electrical Specifications" on page 9, the controller sets the status register and asserts the ALERT# signal. The CPU reads the status register to know that alert assertion has occurred and the controller clears ALERT#. If system temperature continues to rise and NTC pin voltage continues to fall, it will pass through the VR_HOT# trip threshold and the controller will assert the VR_HOT# signal. The CPU reduces power consumption and the system temperature gradually drops. As the NTC pin voltage rises through the VR_HOT# reset threshold, the controller deasserts VR_HOT#. If system temperature continues to drop and the NTC pin voltage rises above the thermal alert reset threshold, the controller changes the status register and asserts ALERT# for the CPU to read the cleared status register.

To disable the NTC function, connect the NTC pin to VDD using a pull-up resistor.

Serial Interfaces

Serial VID (SVID) Supported Data and Configuration Registers

The device is compliant with Intel IMVP8™ SVID protocol. To ensure proper CPU operation, refer to this document for SVID bus design and layout guidelines; each platform requires different pull-up impedance on the SVID bus, while impedance matching and spacing among DATA, CLK, and ALERT# signals must be followed. Common mistakes are insufficient spacing among signals and improper pull-up impedance.

The controller supports the following data and configuration registers, accessible via the SVID interface.

TABLE 9. SUPPORTED DATA AND CONFIGURATION REGISTERS

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
00h	Vendor ID	Uniquely identifies the VR vendor. Assigned by Intel.	12h

TABLE 9. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
01h	Product ID	Uniquely identifies the VR product. Intersil assigns this number.	56h
02h	Product Revision	Uniquely identifies the revision of the VR control IC. Intersil assigns this data.	00h
05h	Protocol ID	Identifies what revision of SVID protocol the controller supports.	05h
06h	Capability	Identifies the SVID VR capabilities and which of the optional telemetry registers are supported.	81h
10h-11h	Status	Four separate status registers for reading each active rail.	00h
15h	Output Current	Three separate data registers showing digitalized value of output current read by rail selection.	
1Bh	Input Power	Data register showing system input power information. This register can only be read by the power domain through slave address 0Dh.	
1Ch	Status2_lastread	Single register that can be read by all rails.	00h
21h	I_{CCMAX}	Data register containing the I_{CCMAX} for each rail the platform supports. Set at start-up by PROG resistors and phase configuration.	
24h	Fast Slew Rate	Slew rate normal. The fastest slew rate the platform VR can sustain. Binary format in mV/µs. i.e., 1Eh = 30mV/µs. Single register read back for rail selection.	
25h	Slow Slew Rate	Default is 2x slower than normal. Binary format in mV/µs. i.e., 10h = 16mV/µs. Can be configured by register 2Ah. Three separate registers read by rail selection.	Set by fast slew rate and Register 2Ah
26h	V_{BOOT}	For normal run conditions, the V_{BOOT} for IA, GT, and GTUS is 0V. Three separate registers read for rail selection.	
2Ah	Slow Slew Rate Selector	Three separate registers read/written based on rail selection. xxxx_0001 = 1/2 of fast slew rate xxxx_001x = 1/4 of fast slew rate xxxx_01xx = 1/8 of fast slew rate xxxx_1xxx = 1/16 of fast slew rate	01h
2Bh	PS4 Exit Latency	Reports 88µs	7Bh

TABLE 9. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
2Ch	PS3 Exit Latency	Reports 4µs	38h
2Dh	Enable to VR_Ready Latency	Reports 704µs	ABh
30h	V_{OUT} Maximum	This register is programmed by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR will respond with “not supported” acknowledge.	FFh
31h	VID Setting	Three separate data registers containing currently programmed VID voltages based on rail selection. VID data format.	
32h	Power State	Three separate registers containing the current programmed power states based on rail selection.	00h
33h	Voltage Offset	Three separate registers which set offset in VID steps added to the VID setting for voltage margining.	00h
34h	Multi VR Config	Data register that configures multiple VRs behavior on the same SVID bus.	01h
35h	SetRegADR	Serial data bus communication address	00h
42h	IVID1_VID	R/W register to set the VID value that when the DAC is below this value and above IVID1_VID and Alert# for VRsettled is asserted, the power state will be forced to PS1. Processor will change this value as necessary.	00h
43h	IVID1-I	Three separate R/W registers to set the maximum current that corresponds to IVID1_VID.	14h
44h	IVID2_VID	R/W register to set the VID value that when the DAC is below this value and above IVID2_VID and Alert# for VRsettled is asserted, the power state will be forced to PS2. Processor will change this value as necessary.	00h
45h	IVID2-I	R/W register to set the maximum current that corresponds to IVID2_VID.	14h

TABLE 9. SUPPORTED DATA AND CONFIGURATION REGISTERS (Continued)

INDEX	REGISTER NAME	DESCRIPTION	DEFAULT VALUE
46h	IVID3_VID	R/W register to set the VID value that when the DAC is below this value and above IVID3_VID and Alert# for VRsettled is asserted, the power state will be forced to PS2. Processor will change this value as necessary.	00h
47h	IVID3-I	R/W register to set the maximum current that corresponds to IVID3_VID.	05h

The SVID ALERT# signal is asserted for the following conditions:

1. When VRsettled is asserted for non-zero volt commandedVID. If the commandedVID is changed, ALERT# will deassert while the DAC is moving to the new target.
2. Therm alert changing from 0 to 1 or from 1 to 0. (Read Status1 required to clear this alert flag.)
3. $I_{CC(MAX)}$ alert changing from 0 to 1 or from 1 to 0. (Read Status1 required to clear this alert flag.)

PMBus Interface

The ISL95866 features a PMBus interface, which allows for user programmability of numerous operating parameters and for monitoring various parameters of the VR A and B regulators. The PMBus address for the ISL95866 is 1000_000.

TABLE 10. PMBus READ AND WRITE REGISTERS

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION	
D3h	R	xxh	READ_VOUT_VRA	Read only of the VR A voltage in ADC format. Reads back DAC + and OFFSET programmed. Each LSB is 5.0mV.	
D4h	R	xxh	READ_IOUT_VRA	Read only of VR A current in ADC format. FFh = 100% (7.5µA on IMON).	
D5h	Reserved				
D6h	R	xxh	READ_VOUT_VRB	Read only of the VR B voltage in ADC format. Reads back DAC + and OFFSET programmed. Each LSB is 5.0mV.	
D7h	R	xxh	READ_IOUT_VRB	Read only of VR B load current in ADC format. FFh = 100% (7.5µA on IMON).	
DEh	R/W	00h	SETVID_VRA	Set VR A VID, default set to 0mV. Each LSB is 5.0mV.	
E0h	R/W	00h	SETOFFSET_VRA	Set VR A offset. The offset range is from -640mV to +635mV. This is a 2's complement number. Bit[7] is the sign bit.	
E1h	Reserved				
E2h	R/W	00h	SETVID_VRB	Set VR B VID, default set to 0mV. Each LSB is 5.0mV.	
E3h	R/W	00h	SETOFFSET_VRB	Set VR B offset. The offset range is from -640mV to +635mV. This is a 2's complement number. Bit[7] is the sign bit.	
D8h	R/W	00h	SET_OV	Default does not change overvoltage operation. Allows override of normal operation to overvoltage of 2.455.	
D9h	R/W	00h	SET_SVID_LOCK_VRA	**VALUE**	**FUNCTIONALITY**
				00	No SETVID_VRA or SETOFFSET_VRA commands executed. Executes SVID commands. R/W of registers still active.
				01	Only SETOFFSET_VRA command accepted for small calibration offsets. SVID commands ignored. Forces PS0 while the rail is ramping and will return to the SVID power state when the ramp is complete.
				10	Only SETOFFSET_VR A command accepted for larger offsets. SVID commands ignored. Forces PS0 CCM operation until 00h is written.
				11	Accepts SETVID_VRA and SETOFFSET_VRA commands and ignores SVID commands. Forces PS0 CCM operation until 00h is written.
DAh	R/W	00h	SET_SVID_LOCK_VRB	**BIT[0] VALUE**	**FUNCTIONALITY**
				00	No SETVID_VRB or SETOFFSET_VRB commands executed. Executes SVID commands. R/W of registers still active.
				01	Only SETOFFSET_VRB command accepted for small calibration offsets. SVID commands ignored. Forces PS0 while the rail is ramping and will return to the SVI power state when the ramp is complete.
				10	Only SETOFFSET_VRB command accepted for larger offsets. SVID commands ignored. Forces PS0 CCM operation until 00h is written.
				11	Accepts SETVID_VRB and SETOFFSET_VRB commands and ignores SVID commands. Forces PS0 CCM operation until 00h is written.
DBh	R/W	0h	DROOP_EN_VRA	0h = Droop enabled; 1h = Droop disabled; Default is droop enabled for VR A. When VR_ENABLE is low this register is set back to default of droop enabled for VR A.	

TABLE 10. PMBus READ AND WRITE REGISTERS (Continued)

COMMAND CODE	ACCESS	DEFAULT	COMMAND NAME	DESCRIPTION	
DCh	R/W	00h	DROOP_EN_VRB	BIT VALUE	FUNCTIONALITY
				00	VRB default is set by PROG1 resistor configuration. When VR_ENABLE is low this register is set back to PROG1 default configuration for VRB.
				01	VRB Droop Enabled. When VR_ENABLE is low this register is set back to PROG1 default configuration for VRB.
				10	VRB Droop Disabled. When VR_ENABLE is low this register is set back to PROG1 default configuration for VRB.
DDh	R/W	0h	OCP_EN	Default is 0h = OCP active. 1h = OCP disabled. State of register impacts both VRA and VRB. The controller will take no action to protect or indicate an OCP fault has occurred if the register is set to 1h. The customer will take responsibility for providing OCP protection if required of the load device.	
DFh	R/W	00h	SET_FREQ	BIT VALUE	FUNCTIONALITY
				00	VRA and VRB switching frequency set per PROG resistor configuration, see Table 4 on page 19.
				01	Switching frequency set to 300kHz for both VRA and VRB. Toggling VR_ON will reset this register to 00h.
				10	Switching frequency set to 350kHz for both VRA and VRB. Toggling VR_ON will reset this register to 00h.
				11	Switching frequency set to 400kHz for both VRA and VRB. Toggling VR_ON will reset this register to 00h.
E4h	R/W	00h	VR A OCP Threshold Adjustment	BIT VALUE	FUNCTIONALITY
				00	VR A OCP Threshold default of 100% of nominal value.
				01	VR A OCP Threshold adjustment to 120% of nominal value.
				10	VR A OCP Threshold adjustment to 150% of nominal value.
				11	VR A OCP Threshold adjustment to 200% of nominal value.
E5h	R/W	00h	VR B OCP Threshold Adjustment	BIT VALUE	FUNCTIONALITY
				00	VR B OCP Threshold default of 100% of nominal value.
				01	VR B OCP Threshold adjustment to 120% of nominal value.
				10	VR B OCP Threshold adjustment to 150% of nominal value.
				11	VR B OCP Threshold adjustment to 200% of nominal value.
E6h	R/W	00h	VR A Droop Adjustment	BIT VALUE	FUNCTIONALITY
				00	VR A Droop default of 100% or nominal value.
				01	VR A Droop reduced to 75% of nominal.
				10	VR A Droop reduced to 50% of nominal.
				11	VR A Droop reduced to 25% of nominal.
E7h	R/W	00h	VR B Droop Adjustment	BIT VALUE	FUNCTIONALITY
				00	VR B Droop default of 100% or nominal value.
				01	VR B Droop reduced to 75% of nominal.
				10	VR B Droop reduced to 50% of nominal.
				11	VR B Droop reduced to 25% of nominal.

Layout Guidelines

PCB Layout Considerations

POWER AND SIGNAL LAYERS PLACEMENT ON THE PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with the weak analog or logic signal layers on the opposite side of the board. The ground plane layer should be adjacent to the signal layer to provide shielding.

COMPONENT PLACEMENT

There are two sets of critical components in a DC/DC converter; the power components and the small signal components. The power components are the most critical because they switch large amounts of energy. The small signal components connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first and these include MOSFETs, input and output capacitors, and the inductor. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each power train. Symmetrical layout allows heat to be dissipated equally across all power trains. Keeping the distance between the power train and the control IC short helps keep the gate drive traces short. These drive signals include the LGATE, UGATE, PGND, PHASE, and BOOT.

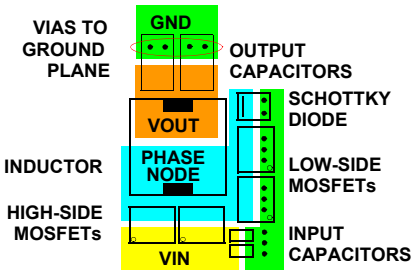


FIGURE 44. TYPICAL POWER COMPONENT PLACEMENT

When placing MOSFETs, try to keep the source of the upper MOSFETs and the drain of the lower MOSFETs as close as thermally possible (see Figure 44). Input high-frequency capacitors should be placed close to the drain of the upper MOSFETs and the source of the lower MOSFETs. Place the output inductor and output capacitors between the MOSFETs and the load. High-frequency output decoupling capacitors (ceramic) should be placed as close as possible to the decoupling target (microprocessor), making use of the shortest connection paths to any internal planes. Place the components in such a way that the area under the IC has less noise traces with high dV/dt and di/dt, such as gate signals and phase node signals.

Table 11 shows layout considerations for the ISL95866 controller by pin.

TABLE 11. LAYOUT CONSIDERATIONS FOR THE ISL95866 CONTROLLER

ISL95866 PIN	SYMBOL	LAYOUT GUIDELINES
BOTTOM PAD	GND	Connect this ground pad to the ground plane through a low impedance path. A minimum of five vias are recommended to connect this pad to the internal ground plane layers of the PCB.
1	ISEN3_B	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN_B, then through another capacitor (C_{vsumn_b}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISENx_B pin to another ISENx_B pin 2. Any ISENx_B pin to GND
2	NTC_B	The NTC thermistor must be placed close to the thermal source that is monitored to determine VR B thermal throttling. Placement at the hottest spot of VR B is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.
3	IMON_B	Current monitor resistor and capacitor should be placed near the pin. Route noisy signals away from this connection.
4	VR_HOT#	Placement of the pull-up resistor near the IC is recommended.
5	SCLK	Use good signal integrity practices
6	ALERT#	
7	SDA	
8	VR_ENABLE	No special considerations
9	PSYS	Analog input from battery charger, which needs to be routed away from noisy signals.
10	PROG	No special considerations.
11	VR_READY	Place the IMON resistor close to this pin and make a tight GND connection.
12	NTC_A	The NTC thermistor must be placed close to the thermal source that is monitored to determine VR A thermal throttling. Placement at the hottest spot of VR A is recommended. Additional standard resistors in the resistor network on this pin should be placed near the IC.
13	IMON_A	Place the IMON resistor close to this pin and make a tight GND connection.

TABLE 11. LAYOUT CONSIDERATIONS FOR THE ISL95866 CONTROLLER (Continued)

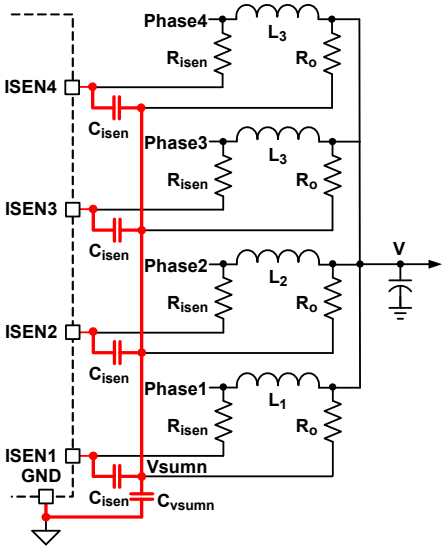
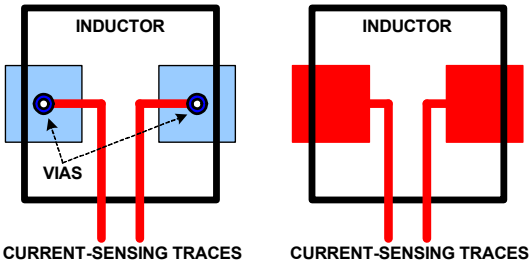
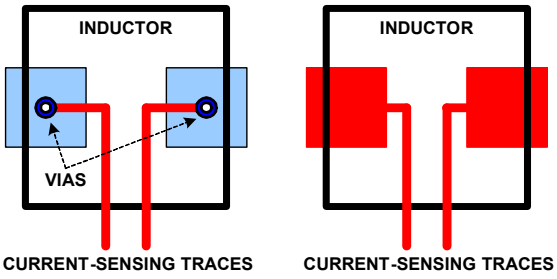
ISL95866 PIN	SYMBOL	LAYOUT GUIDELINES
14	ISEN4_A	Each ISEN pin has a capacitor (C_{isen}) decoupling it to V_{sumn} and then through another capacitor (C_{vsumn}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISEN pin to another ISEN pin 2. Any ISEN pin to GND The red traces in the following drawing show the loops to be minimized. 
15	ISEN3_A	
16	ISEN2_A	
17	ISEN1_A	
18	ISUMP_A	Place the current-sensing circuit in general proximity of the controller. Place capacitor C_n very close to the controller. Place the NTC thermistor next to VR A Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of V_{SUMP} and V_{SUMN} signals to the controller. Run these two signals traces in parallel fashion with decent width (>20 mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current-sensing traces. 
19	ISUMN_A	
20	RTN_A	Place the RTN filter in close proximity of the controller for good decoupling.
21	PROG2	
22	FB_A	Place the compensation components in general proximity of the controller.
23	COMP_A	
24	VDD	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin with the filter resistor nearby the IC.
25	BOOT1_A	Use a wide trace width (>30 mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
26	PHASE1_A	These two signals should be routed together in parallel. Each trace should have sufficient width (>30 mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE1_A to the VR A Channel 1 high-side MOSFET source pin instead of a general connection to PHASE1_A copper is recommended for better performance.
27	UGATE1_A	
28	LGATE1_A	Use sufficient trace width (>30 mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.

TABLE 11. LAYOUT CONSIDERATIONS FOR THE ISL95866 CONTROLLER (Continued)

ISL95866 PIN	SYMBOL	LAYOUT GUIDELINES
29	BOOT2_A	Use a wide trace width (>30 mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
30	PHASE2_A	These two signals should be routed together in parallel. Each trace should have sufficient width (>30 mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE2_A to the VR A Channel 2 high-side MOSFET source pin instead of a general connection to PHASE2_A copper is recommended for better performance.
31	UGATE2_A	
32	VDDP	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin.
33	LGATE2_A	Use sufficient trace width (>30 mil). Avoid routing this signal near any sensitive analog signal traces or crossing over them.
34	LGATE1_N	
35	PHASE1_B	These two signals should be routed together in parallel. Each trace should have sufficient width (>30 mil). Avoid routing these signals near sensitive analog signal traces or crossing over them. Routing PHASE1_B to the high-side MOSFET source pin instead of a general connection to the PHASE1_B copper is recommended for better performance.
36	UGATE1_B	
37	BOOT1_B	Use a wide trace width (>30 mil). Avoid routing any sensitive analog signal traces close to or crossing over this trace.
38	PWM3_A	PWM output to MOSFET driver/Powerstage, which needs to be routed away from noisy signals.
39	PWM4_A	
40	PWM2_B	
41	PWM3_B	
42	I2CLK	Use good signal integrity practices
43	I2DATA	
44	VIN	A high quality, X7R dielectric MLCC capacitor is recommended to decouple this pin to GND. Place the capacitor in close proximity to the pin.
45	COMP_B	Place the compensation components in general proximity of the controller.
46	FB_B	
47	PROG3	
48	RTN_B	Place the RTN filter in close proximity of the controller for good decoupling.
49	ISUMN_B	Place the current-sensing circuit in general proximity of the controller. Place capacitor C_n very close to the controller. Place the NTC thermistor next to VR B Channel 1 inductor so it senses the inductor temperature correctly. Each phase of the power stage sends a pair of V_{SUMP} and V_{SUMN} signals to the controller. Run these two signals traces in parallel fashion with decent width (>20 mil). IMPORTANT: Sense the inductor current by routing the sensing circuit to the inductor pads. If possible, route the traces on a different layer from the inductor pad layer and use vias to connect the traces to the center of the pads. If no via is allowed on the pad, consider routing the traces into the pads from the inside of the inductor. The following drawings show the two preferred ways of routing current-sensing traces. 
50	ISUMP_B	
51	ISEN1_B	Each ISEN pin has a capacitor (C_{isen}) decoupling it to VSUMN_B, then through another capacitor (C_{vsumn_nb}) to GND. Place C_{isen} capacitors as close as possible to the controller and keep the following loops small: 1. Any ISENx_B pin to another ISENx_B pin 2. Any ISENx_B pin to GND
52	ISEN2_B	

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 28, 2016	FN8821.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

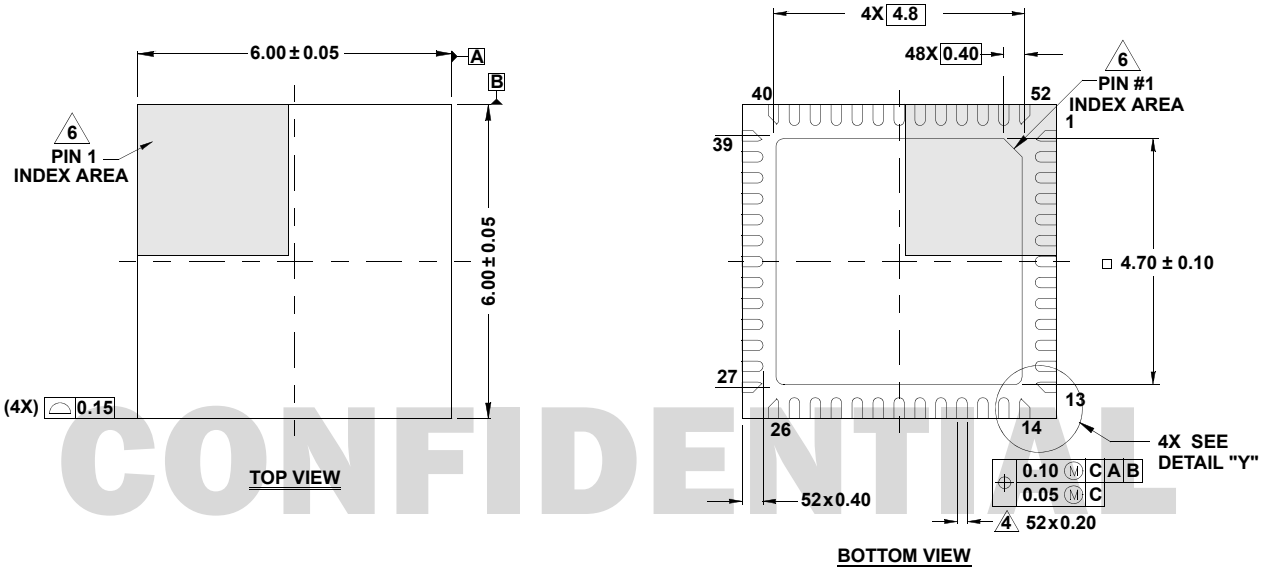
Package Outline Drawing

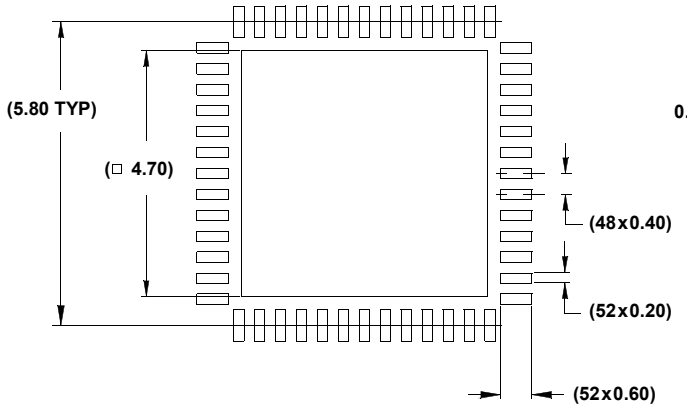
For the most recent package outline drawing, see L52.6x6A.

L52.6X6A

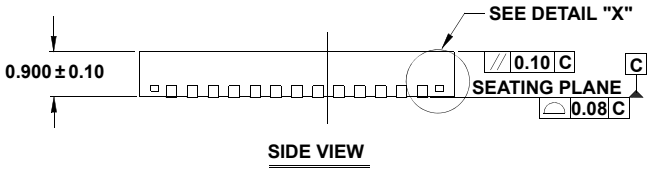
52 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE CHAMFERED CORNER LEADS

Rev 1, 7/14

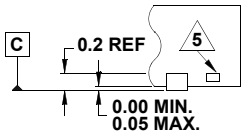




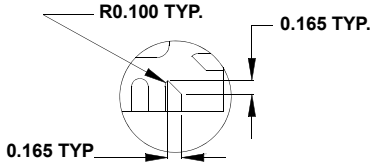
TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"



DETAIL "Y"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.