A Mobile Multi-Phase PWM Controller with Precision Current Sensing

The ISL6247 provides microprocessor core-voltage regulation by driving up to four interleaved synchronous-rectified buck-converter channels in parallel. Multi-phase buck converter architecture uses interleaved timing to multiply ripple frequency and reduce input and output ripple currents. The reduction in ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area. The ISL6247 multi-phase controller together with ISL6207 gate drivers forms the basis for a portable power supply solution to power Intel's next generation mobile microprocessors.

Intel Mobile Voltage Positioning (IMVP) is a smart voltage regulation technology which effectively reduces power dissipation in Intel® Pentium® Processors. The ISL6247 supports the IMVP-5 mobile processor voltage regulation specifications. To boost battery life, the ISL6247 operates in Active, Deep Sleep, or Deeper Sleep modes, depending upon the logic levels at the DSEN# and DRSEN pins. A 6-bit digital-to-analog converter (DAC) allows dynamic adjustment of the core output voltage from 0.8375V to 1.6V. The controller features a thermal monitor which sends a signal to the microprocessor to reduce the load before power system components exceed their maximum thermal limits, reducing the thermal design complexity and overall core-voltage regulation cost.

To improve efficiency, the ISL6247 allows users to select one of two popular lossless current sense techniques. The ISL6247 supports detection via inductor coil resistance (DCR), or the $r_{DS(ON)}$ of the lower MOSFET. Either cost and space-saving method provides feedback for precision droop, channel current balancing, and individual channel over-current protection. A unity gain, differential amplifier is provided for remote voltage sensing. The differential amplifier eliminates errors due to potential differences between remote and local grounds. Eliminating ground differences improves regulation and protection accuracy. The channel switching frequency is adjustable in the range of 200kHz to 1.0MHz, providing flexibility in managing the balance between high-speed response, target efficiency, and good thermal management.

Ordering Information

PART NUMBER	TEMP. (^{O}C)	PACKAGE	PKG. DWG. #
ISL6247CR	-10 to 100	40 Ld 6x6 QFN	L40.6X6
ISL6247CR-T	40 Lead 6x6 QFN Tape and Reel		
Lead-Free Packaging (Pb Free)			
ISL6247CRZ	-10 to 100	40 Ld 6x6 QFN	L40.6X6
ISL6247CRZ-T	40 Lead 6x6 QFN Tape and Reel		

Features

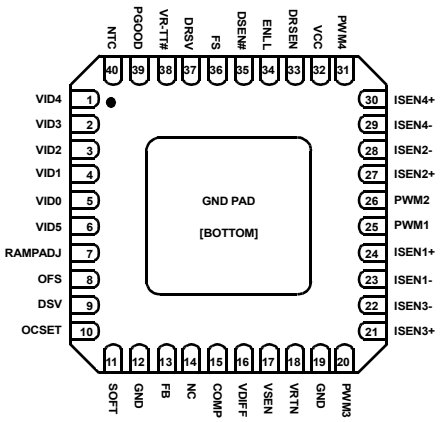
- Precision Multi-Phase Core Voltage Regulation
  - ±0.6% System Accuracy Over Temperature
- Microprocessor Voltage Identification Input
  - 6-Bit VID Input
  - 0.8375V to 1.600V in 12.5mV Steps
  - Supports VID Changes During Operation
- Multiple Current Sensing Approaches Supported
  - Lossless DCR Current Sensing
  - Precision Resistive Current Sensing
  - Low Cost $R_{DS(on)}$ Current Sensing
- Excellent Dynamic Response
  - Combined Input Voltage Feed-Forward and Pulse-by-Pulse Average Current Mode
- DSEN# and DRSEN Logic Inputs for Low Power States
- DSV Voltage Input for DEEP SLEEP Mode
- DRSV Voltage Input for DEEPER SLEEP Mode
- Thermal Monitor
- Active Channel Current Balancing
- Differential Remote Voltage Sensing
- Individual Channel Over-Current, Over-Voltage, and Under-Voltage Protection
- 2, 3, or 4-Phase Operation
- User selectable Switching Frequency of 200K - 1.0MHz
  - 400kHz - 4MHz Effective Ripple Frequency
- QFN Package Option
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile

Applications

- Notebook Computer IMVP-5 DC/DC converter

Pinout

ISL6247CR (40 LD QFN 6X6)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . .+7V
Input, Output, or I/O Voltage . . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . .Class 2

Operating Conditions

Supply Voltage, VCC . . . . . +5V ±5%
Ambient Temperature. . . . . -10°C to 100°C
Junction Temperature . . . . . -10°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JA} (°C/W)
QFN Package	32	3.5

Maximum Junction Temperature . . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . .300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
2. θ_{JC}, the "case temperature" location is the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.

Electrical Specifications

Operating Conditions: VCC = 5V, T_A = -10°C to 85°C. Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY POWER					
Operating Current	R_{FS} = 90.9K; ENLL = 1V	-	12	17	mA
Shutdown Current	R_{FS} = GND; ENLL = 0V	-	12	17	mA
POR (Power-On Reset) Threshold	VCC Rising; FB = 0V	4.20	4.35	4.50	V
	VCC Falling; FB = 0V	3.65	3.80	3.95	V
ENABLE INPUT (ENLL)					
Enable Threshold		0.5	0.6	0.7	V
High State Leakage Current	ENLL = 1.0V	-	-200	-	nA
Low State Leakage Current	ENLL = 0.0V	-	49	-	µA
REFERENCE VOLTAGE AND DAC					
System Accuracy	25°C	-0.5	-	+0.5	%VID
	V_{DAC} = 1.1000V to 1.6000V	-0.6	-	+0.6	%VID
	V_{DAC} = 0.8375V to 1.0875V	-0.7	-	+0.7	%VID
VID Input Threshold Voltage		0.4	0.6	0.8	V
VID Current	VID_X = 0.0V	-	47	-	µA
	VID_X = 1.0V	0	-1.5	-10	µA
OSCILLATOR					
Accuracy	R_{FS} = 90.9kΩ ±1%	270	300	330	kHz
Adjustment Range		200		1000	kHz
Sawtooth Ramp Amplitude	$V_{RAMPADJ}$ = 1.8V	-	1.0	-	V
Duty-Cycle Range		0	-	66	%
FS Output Voltage	R_{FS} = 90.9kΩ ±1%	1.223	1.235	1.247	V
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to Ground	-	72	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to Ground	-	18	-	MHz
Slew Rate	C_L = 100pF, R_L = 10kΩ to Ground	-	5.3	-	V/µs
Maximum Output Voltage	FB = GND; V_{DAC} = 1.1V; R_L = 10kΩ to Ground	3.6	4.2	-	V
Minimum Output Voltage	FB = 1.2; V_{DAC} = 1.1V; Sinking 300µA	-	0.2	-	V
Output Sourcing Current	VCOMP = 2V; FB = 0.75V; V_{DAC} = 1V	0.82	2.1	-	mA
Output Sinking Current	VCOMP = 1V; FB = 1.25; V_{DAC} = 1V	1.2	1.6	-	mA
Input Offset	FB = 1V; OFS = OPEN	-	0	-	mV

Electrical Specifications Operating Conditions: VCC = 5V, T_A = -10°C to 85°C. Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PIN-ADJUSTABLE OFFSET					
OFS Voltage	I_{OFS} = -20µA; Respect to GND	-	0.5	-	V
	I_{OFS} = 20µA; Respect to V_{CC}	-	-2	-	V
PWM					
PWM High State	I_{PWM} = -2.5mA	-	4.5	-	V
PWM Low State	I_{PWM} = +5mA	-	0.7	-	V
PWM Three-State	PWM = 2.5V	-1	-	1	µA
DIFFERENTIAL SENSE AMPLIFIER					
Bandwidth		-	20	-	MHz
Slew Rate		-	6	-	V/µs
Input Offset	VSEN = 1.6V; VRTN = 0.005V;	-	2	-	mV
Input Bias Current	VSEN = 1.2V	-100	-	100	nA
Pull-Down Current	VSEN = 0.6V; VDIFF = 0.7V	-	800	-	µA
Output Impedance		-	30	-	Ω
CURRENT SENSE AMPLIFIERS					
Input Offset	[(ISEN+) - (ISEN-)]	-5	-	5	mV
I_{SEN} Accuracy	ISEN1=ISEN2=ISEN3=ISEN4=50µA	-8	-	8	%
SOFT START					
Initial Soft-Start Current	SOFT < 0.5V	-	25	-	µA
SOFT Slew Current	SOFT > 0.5V	-	500	-	µA
Deeper Sleep Slew Current (Entering Only)	SOFT = 1V; DSEN = 0V; DRSEN = 2V	-	100	-	µA
POWER GOOD AND PROTECTION MONITORS					
PGOOD Low Voltage	I_{PGOOD} = -4mA; ENLL = GND	-	0.18	0.40	V
PGOOD Leakage Current	PGOOD = 5V	-1	0	1	µA
Under-Voltage Threshold	VSEN Rising	-	90	-	%VID
	VSEN Falling	84	86	88	%VID
Over-Voltage Threshold	(VID + OV Threshold)	170	200	230	mV
OCSET Voltage Accuracy	V_{DAC} = 1.325V	-	1.325	-	V
I_{SEN} Over-Current Trip Level	R_{OCSET} = 13.25kΩ; V_{DAC} = 1.325V	-	-77	-	µA
INPUT LEAKAGE CURRENT					
FB	ISEN1=ISEN2=ISEN3=ISEN4 = 0µA; OFS open	-	50	-	nA
DSV, DRSV		-	50	-	nA
RAMPADJ	RAMADJ = 1.8V	-	100	-	nA
SLEEP STATE THRESHOLDS					
Deep Sleep Enable Threshold	DSEN# Rising	1.7	-	-	V
	DSEN# Falling	-	-	1.05	V
Deeper Sleep Enable Threshold	DRSEN Rising	1.7	-	-	V
	DRSEN Falling	-	-	1.05	V
DEEP AND DEEPER SLEEP VOLTAGE					
DSV Accuracy	(V_{OUT} - DSV); DSV = 1.2V	-15	-	+15	mV
DRSV Accuracy	(V_{OUT} - DRSV); DRSV = 0.75V	-15	-	+15	mV
THERMAL MONITOR					
NTC Source Current	NTC = 0.6V	34	40	47	µA
Over-Temperature Threshold	V (NTC) Falling	0.485	0.5	0.525	V
VR-TT# On-Resistance	NTC < 0.5V; VR-TT# = -4mA; T_A = 25°C	-	12	-	Ω
VR-TT# Sinking Current	VR-TT# Voltage = 0.2V;T_A = 85°C	13	-	17.5	mA

NOTE: Differential and Error Amp of offsets are trimmed out for system accuracy.

Typical Operating Performance

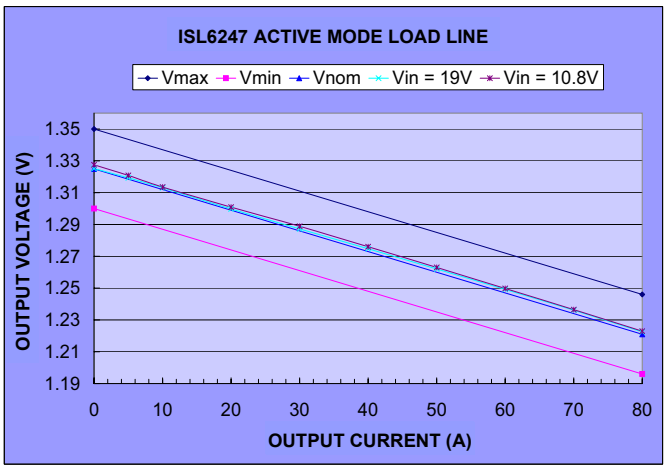


FIGURE 1. ACTIVE LOAD LINE

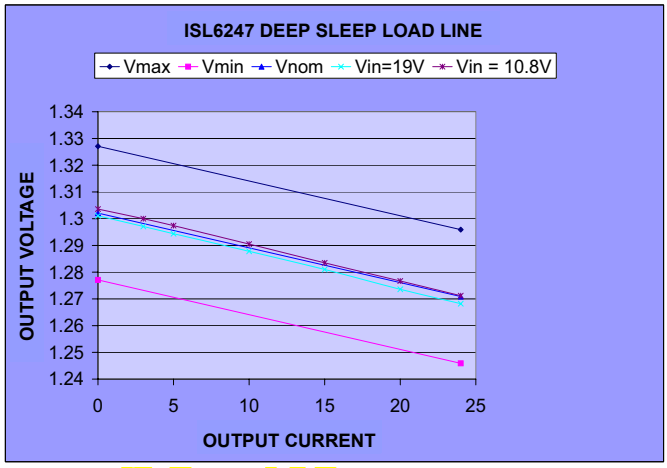


FIGURE 2. DEEP SLEEP LOAD LINE

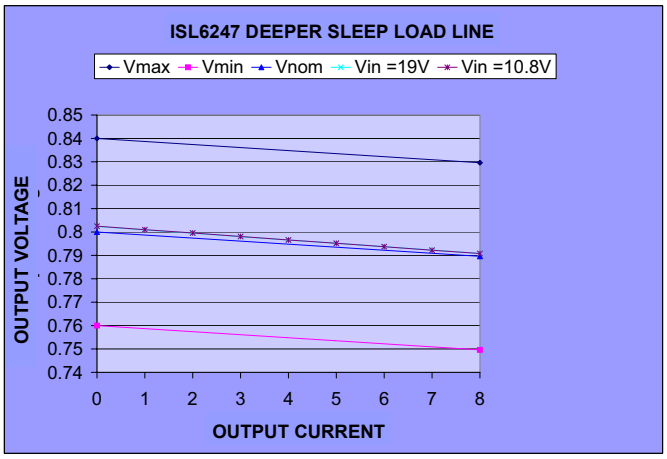


FIGURE 3. DEEPER SLEEP LOAD LINE

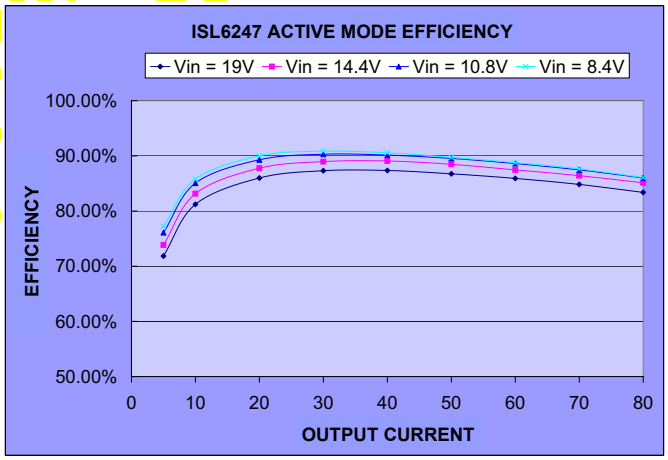


FIGURE 4. ACTIVE EFFICIENCY

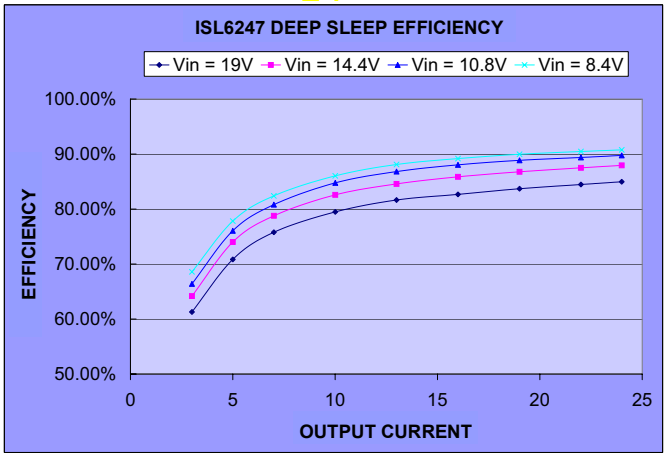


FIGURE 5. DEEP SLEEP EFFICIENCY

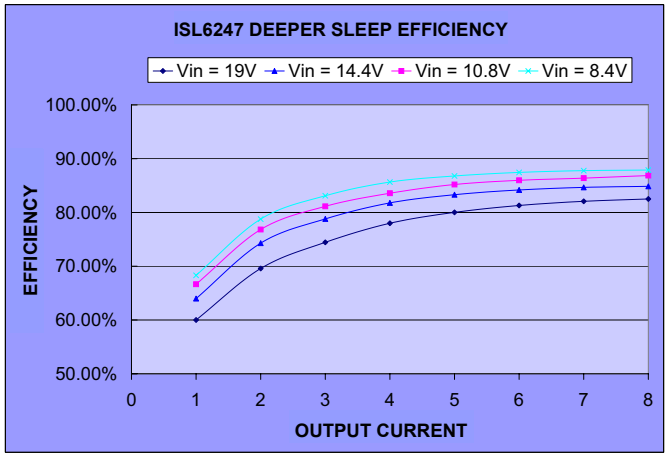


FIGURE 6. DEEPER SLEEP EFFICIENCY

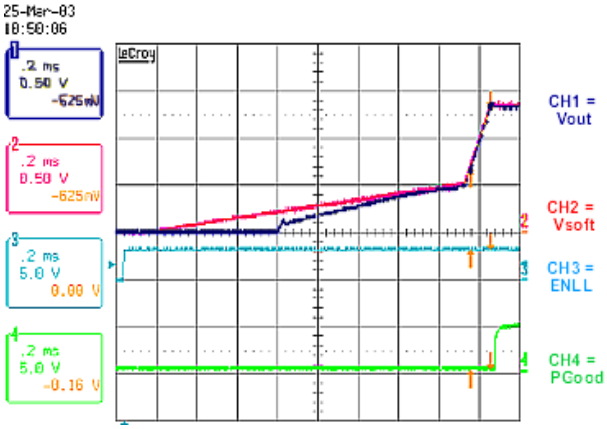


FIGURE 7. SOFT START WAVEFORM

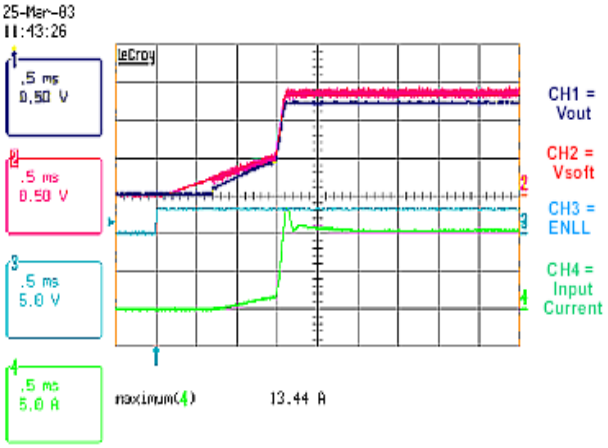


FIGURE 8. INRUSH CURRENT AT VIN 10.8V @ 80A

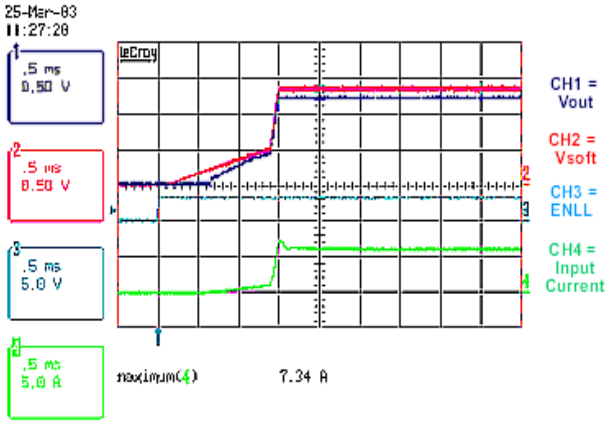


FIGURE 9. INRUSH CURRENT AT VIN 19V @ 80A

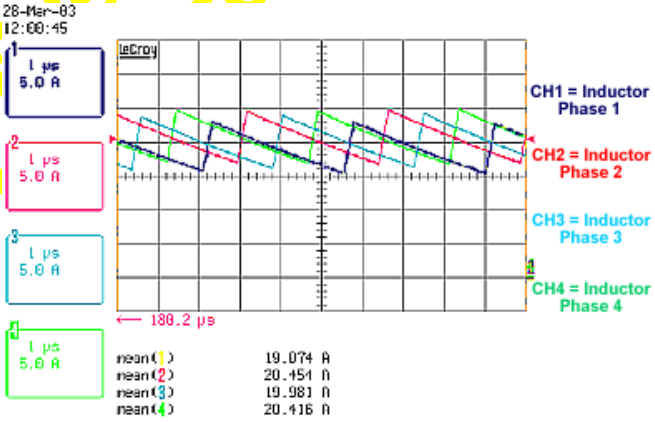


FIGURE 10. FOUR PHASE CURRENT BALANCE @ 80A

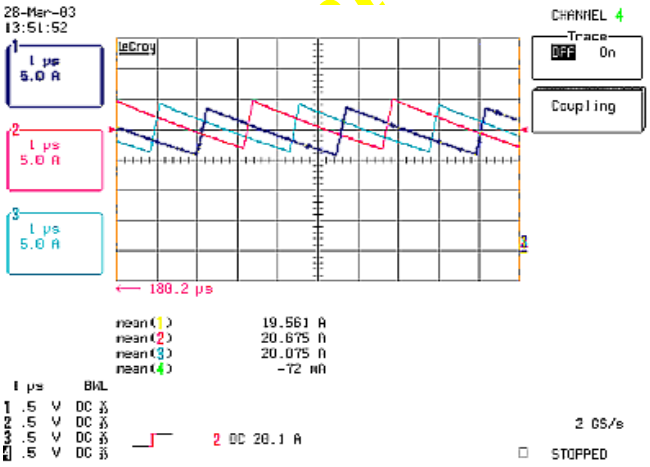


FIGURE 11. THREE PHASE CURRENT BALANCE @ 60A

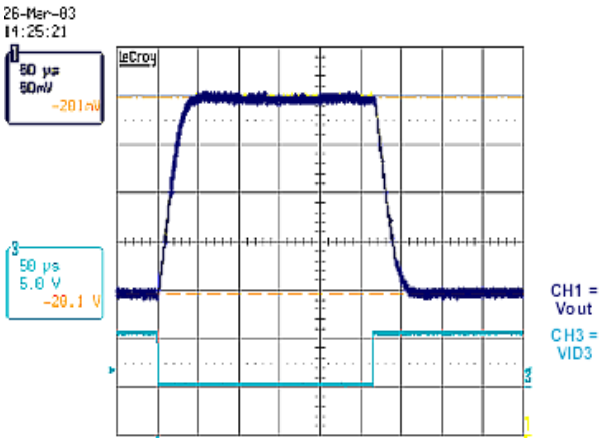


FIGURE 12. VID CHANGE FROM 1.350V TO 1.150V

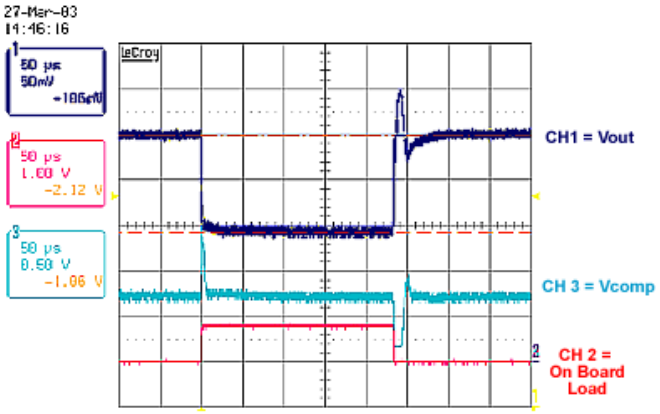


FIGURE 13. TRANSIENT WAVEFORM FROM 0A TO 80A

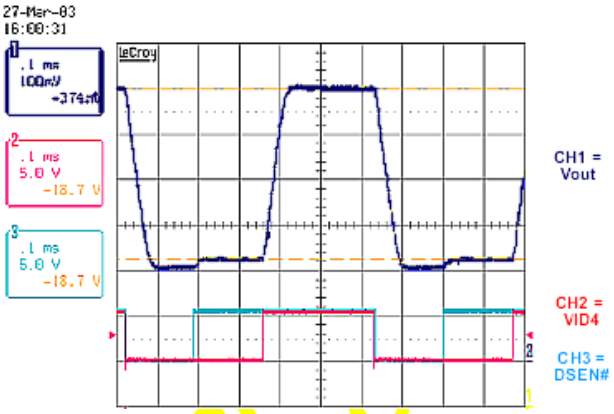


FIGURE 14. GEYSERVILLE TRANSITION

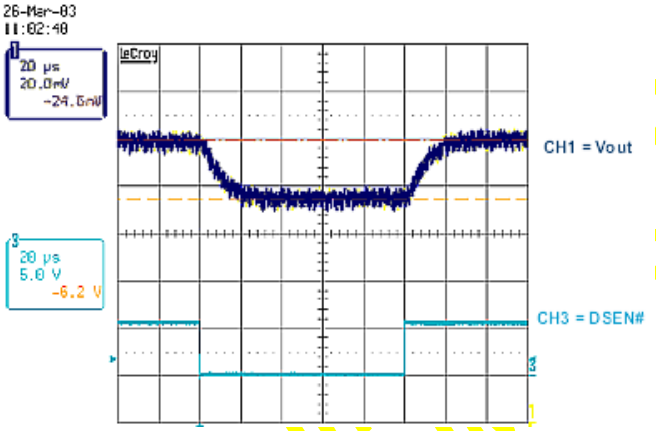


FIGURE 15. ACTIVE TO DEEP SLEEP TRANSITION

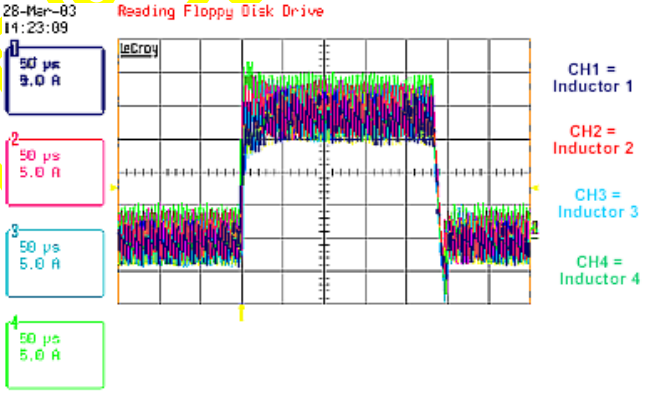


FIGURE 16. INDUCTOR CURRENT TRANSIENT

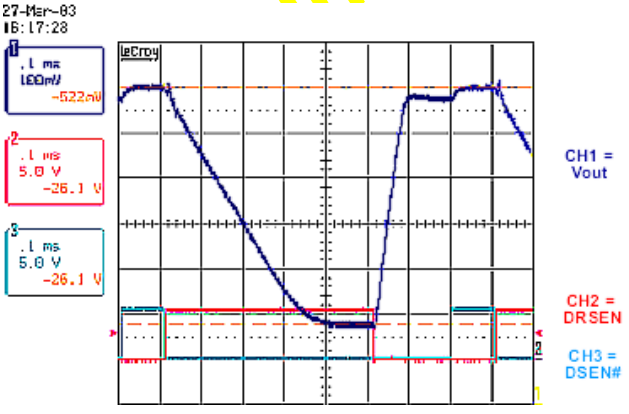


FIGURE 17. C4 TRANSITION

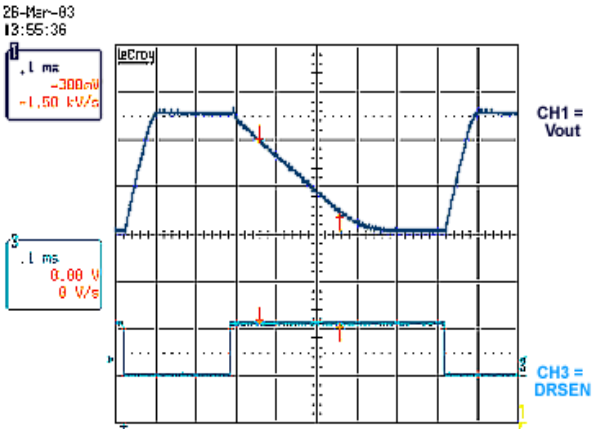
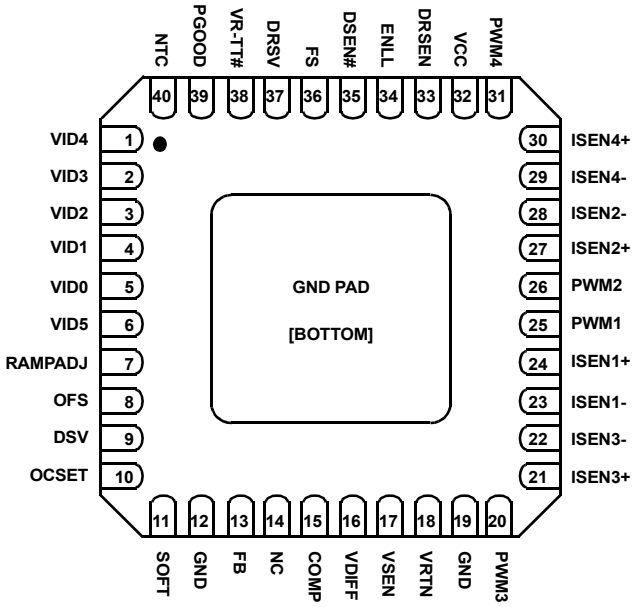


FIGURE 18. DS TO DRS TRANSITION

Functional Pin Description



VCC

Connect a +5V power supply to the VCC pin to supply all the power necessary to operate the controller. When the voltage on this pin exceeds the rising Power-On Reset (POR) threshold, the controller can begin to operate. The controller will shutdown when the voltage on the VCC pin drops below the falling POR threshold.

GND

The GND pin is the bias and signal ground for the controller.

ENLL

The ENLL pin is a logic-level enable input to the controller. Asserting a logic high (>0.6V), the controller is active, depending on the status of the internal POR and fault states. Cycling ENLL to zero will clear all fault states and prime the controller to soft start when re-enabled. ENLL is 5V capable.

FS

Connect a resistor from FS to ground to program the switching frequency. There is an inverse relationship between the value of the resistor and the switching frequency. The voltage at this pin is held at 1.235V and provides a reference for the Deeper Sleep Voltage (DRSV) divider.

VID5, VID4, VID3, VID2, VID1, VID0

The state of these six pins program the internal DAC, which provides the reference voltage for output regulation. These pins have low current (50µA) internal pull-ups. Connect these pins to either open-drain with external pull-up resistors or active-pull-up type outputs.

VDIFF, VSEN, and VRTN

VSEN and VRTN form the inputs to a differential amplifier. The differential amplifier converts the remotely sensed differential voltage of the regulated output to a single-ended voltage, referenced to the local ground of the controller. VDIFF is the amplifier output and the input to the regulation and protection circuitry. Connect VSEN and VRTN to the sense pins of the remote load.

FB and COMP

FB is the inverting input and COMP is the output of the internal error amplifier, respectively. FB is connected to VDIFF through an RC network with a DC resistive connection. COMP is tied back to FB through an external RC network with no DC connection for compensating the regulator.

RAMPADJ

Voltage on the RAMPADJ pin sets the ramp amplitude, providing feed-forward information to the voltage control loop. This should be set at 1/9th of the battery voltage input with an external resistive divider.

OFS

The OFS pin provides a programmable means to introduce a DC offset voltage to the DAC reference. The offset is generated by an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left open. The current which flows through the resistor is output on the FB pin. The magnitude of the offset is determined by the reference voltage and the ratio of the OFS programming resistor to the DC impedance of VDIFF to FB. OFS is intended for introducing offsets in a range within ±50mV of the DAC setting.

PWM1, PWM2, PWM3, PWM4

PWM1, PWM2, PWM3 and PWM4 are pulse-width modulating outputs. These logic outputs instruct the driver IC(s) when to turn-on and turn-off the synchronous buck MOSFETs of each channel. The number of active channels is determined by the state of PWM3 and PWM4. If PWM3 is tied to VCC, two channel operation is indicated to the controller. In this case, PWM4 should be left open or tied to VCC. Shorting PWM4 to VCC indicates that three channel operation is desired.

ISEN1+, ISEN1-, ISEN2+, ISEN2-, ISEN3+, ISEN3-, ISEN4+, ISEN4-

The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers. For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. The sense current is proportional to the output current, and scaled by the DCR of the inductor, divided by R_{ISEN}.

When configured for $r_{DS(ON)}$ current sensing, the ISEN1-, ISEN2-, ISEN3-, and ISEN4- pins are grounded at the lower MOSFET sources. The ISEN1+, ISEN2+, ISEN3+, and ISEN4+ pins are then held at a virtual ground, such that a resistor connected between them, and the drain terminal of the associated lower MOSFET, will carry a current proportional to the current flowing through that channel. The current is determined by the negative voltage developed across the lower MOSFET's $r_{DS(ON)}$, which is the channel current scaled by $r_{DS(ON)}$.

The sensed current is used as a reference for channel balancing, over-current protection, and load-line regulation (by way of the FB pin). Inactive channels should have their respective sense inputs left open (for example, for 3-phase operation open ISEN4+).

DSEN#

The DSEN# logic-level pin toggles the controller between Active and Deep Sleep modes. When held at logic low and DRSEN is low, the controller changes to Deep Sleep mode. The output voltage is set to the voltage on the DSV pin.

DSV

The voltage on the DSV pin programs the output voltage in Deep Sleep mode. An external resistor divider from the OCSET pin can be used to set this voltage.

DRSEN

The DRSEN pin is a logic-level enable for Deeper Sleep mode. While DSEN# is low, if the DRSEN pin is pulled high, the controller transitions from Deep Sleep to Deeper Sleep mode. The output voltage is set to the voltage on the DRSV pin.

DRSV

The voltage on the DRSV pin programs the output voltage in Deeper Sleep mode. An external resistor divider from the FS pin sets the DRSV voltage level.

SOFT

The SOFT pin programs the output slew rate for speedstep or mode of operation changes. This pin is connected to ground via a capacitor.

VR-TT#

The VR-TT# pin is the voltage regulator thermal management signal. VR-TT# is an open-drain, active low output signal.

NTC

The NTC pin commands the VR-TT# signal low when the voltage of this pin is less than 0.5V. Connect this pin to GND with a Negative Temperature Coefficient (NTC) resistor. A 40µA current source flows out this pin to set the voltage drop across the NTC resistor.

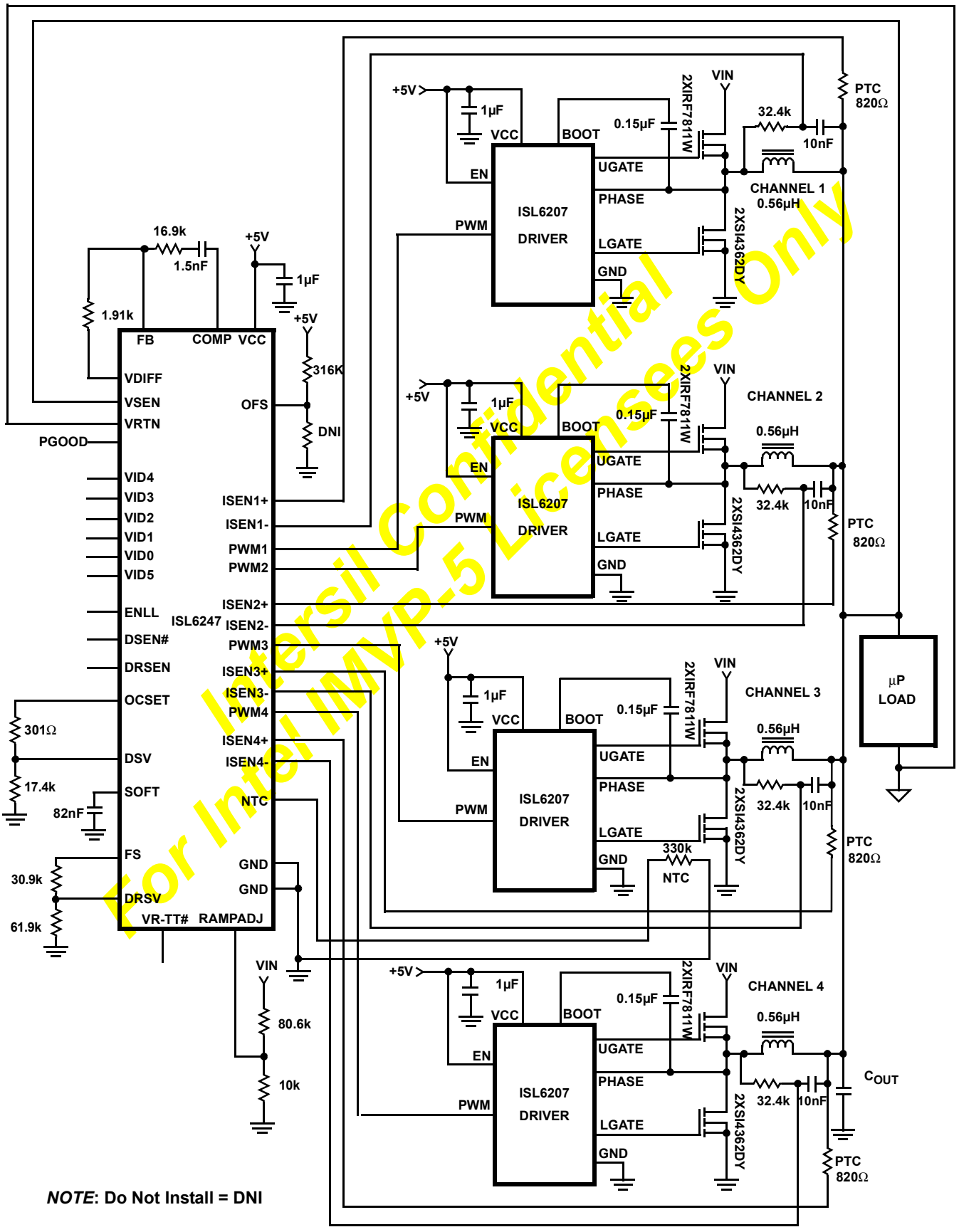
OCSET

The voltage on the OCSET pin is the DAC voltage. Resistors from OCSET to GND set the over-current protection threshold and the Deep Sleep Voltage, DSV, proportional to V_{DAC}.

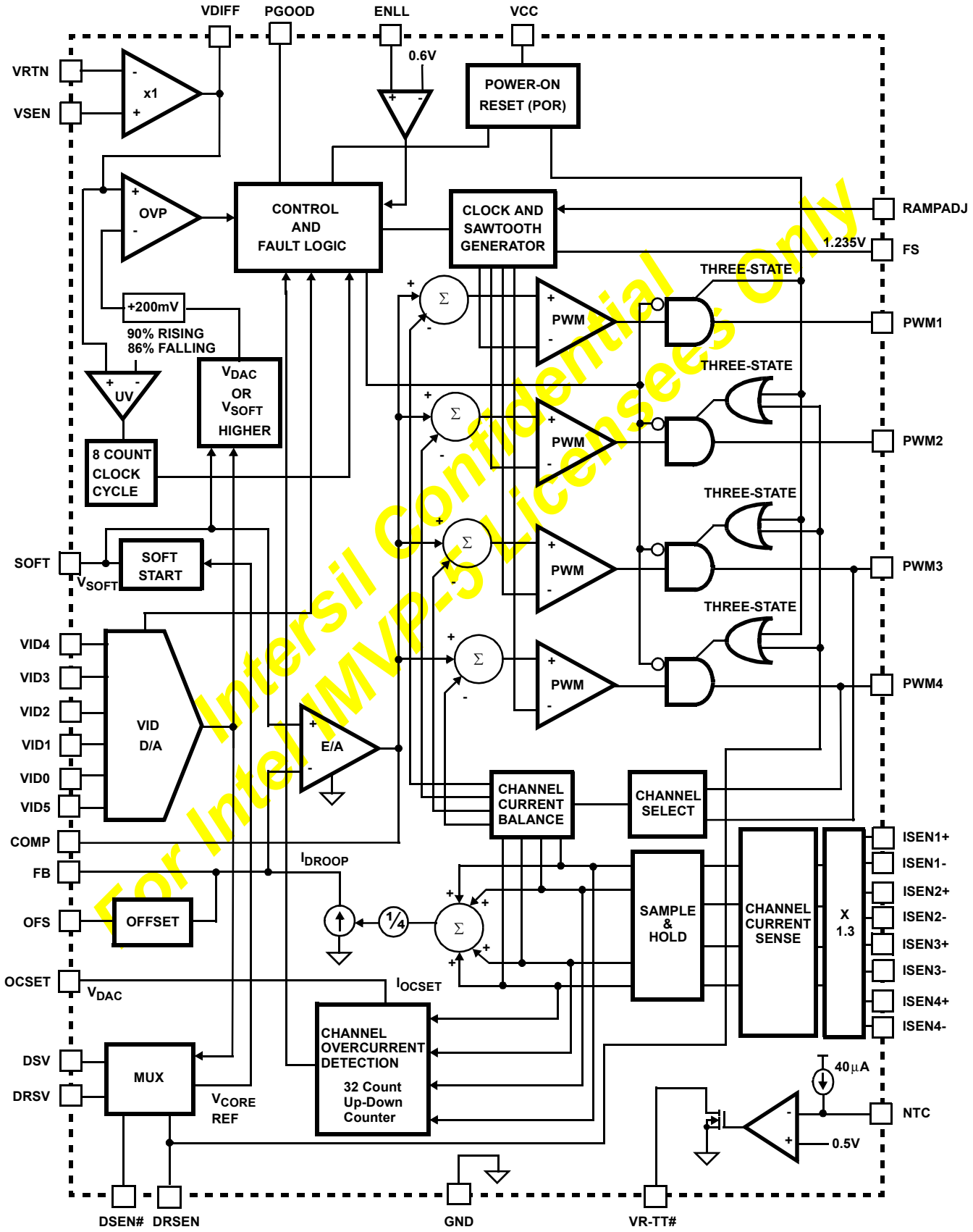
PGOOD

The PGOOD pin is an open drain output and used to indicate the status of the output voltage. PGOOD is pulled high, through an external pull-up resistor, when the output voltage is within the regulation limits.

Typical Application: 4-Phase Buck Converter With DCR Current Sensing



Block Diagram



Theory of Operation

Multi-Phase Power Conversion

Microprocessor load current profiles have advanced to a point where single-phase converter solutions face arduous thermal and cost hurdles. Although its greater complexity presents additional technical challenges, multi-phase power conversion offers cost-saving advantages with improved response time, superior ripple cancellation, and excellent thermal distribution. The ISL6247 controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram in Figure 19 provides a top level view of multi-phase power conversion using the ISL6247 controller.

Interleaving

The switching of each channel in a multi-phase converter is timed to be symmetrically out of phase with each of the other channels. In a 4-phase converter, each channel switches 1/4 cycle after the previous channel and 1/4 cycle before the following channel.

As a result, the four-phase converter has a combined ripple frequency four times greater than the switching frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). The increased ripple frequency and lower ripple amplitude, relative to a single phase approach, results in less per-channel inductance and lower total output capacitance required to meet any performance specification.

Figure 20 illustrates the multiplicative effect of a 3-channel multiphase converter on output ripple frequency. The three channel currents (IL1, IL2, and IL3), combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current waveform for each phase is about one division, and the dc components of the inductor currents combine to feed the load.

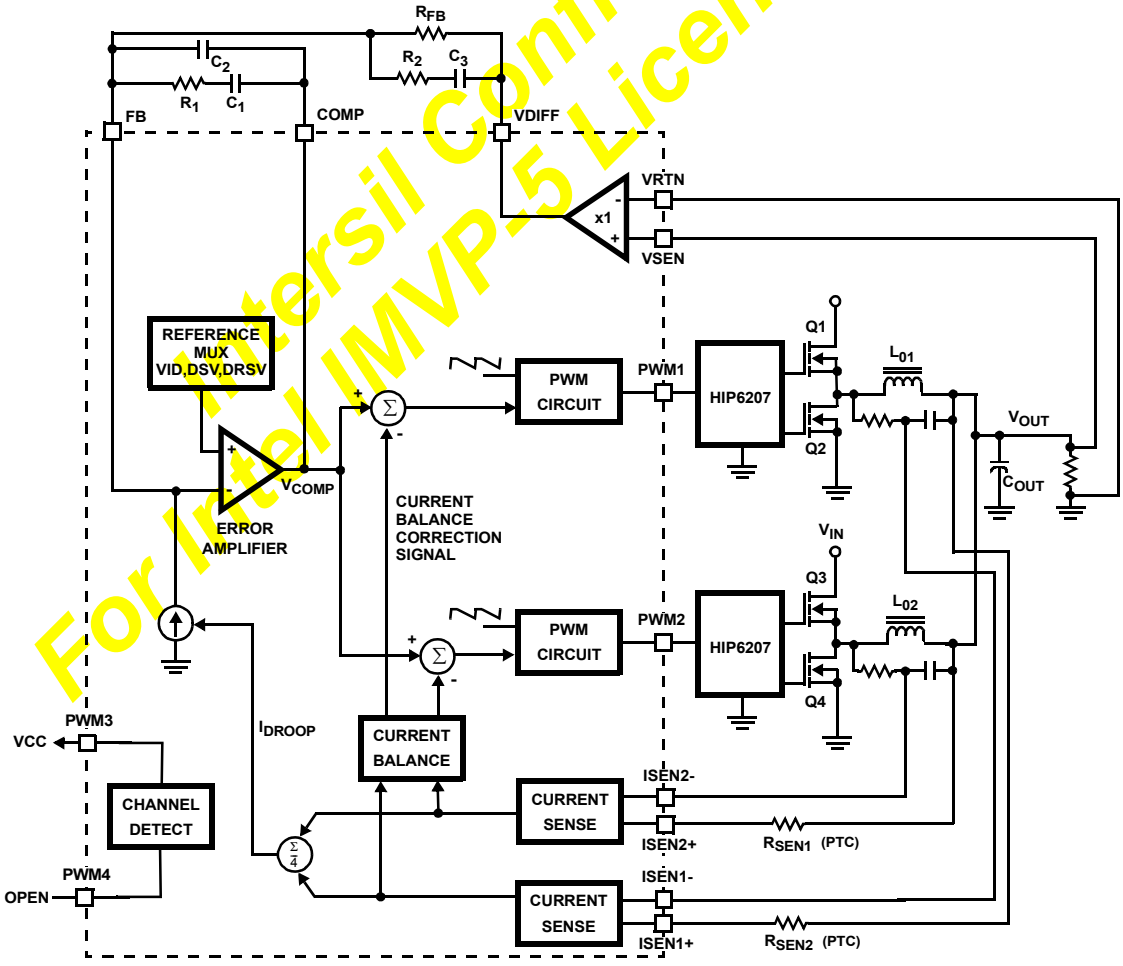


FIGURE 19. SIMPLIFIED BLOCK DIAGRAM OF THE ISL6247 IN A 2-PHASE CONVERTER WITH DCR CURRENT SENSING

Equation 1 is an individual channel's peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 1)}$$

Where, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

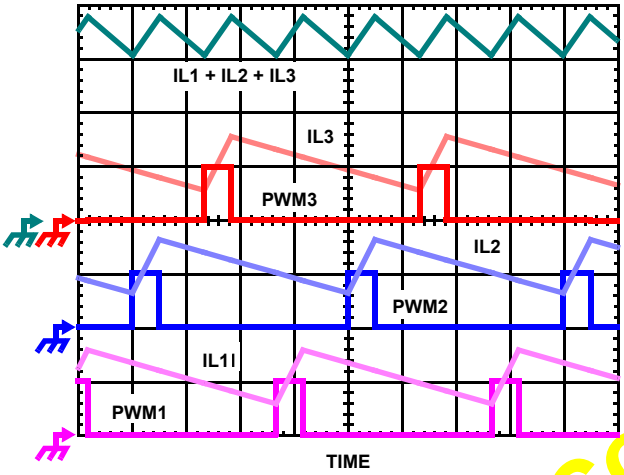


FIGURE 20. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

The output capacitor, C_{OUT}, conducts the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Equation 2 is the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N V_{OUT})V_{OUT}}{L f_S V_{IN}} \quad \text{(EQ. 2)}$$

Another benefit of interleaving is the reduction of input ripple current. Figure 21 illustrates input current reduction for a three-phase converter. Each channel current, as measured through the drain of the upper MOSFET, fills in the input capacitor current. The resulting RMS value is less than the input RMS current of a single-phase converter, at the same regulator output current.

Figures 44, 45 and 46, in the section entitled *Input Capacitor Selection,* can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution.

PWM Operation

The ISL6247 can operate as a 2, 3, or 4 phase converter. The timing of each converter is determined by the number of active channels. By default, the timing mode for the ISL6247 is 4-phase. Select 2-phase timing by connecting PWM3 to VCC and leaving PWM4 open, or by connecting PWM4 to VCC as well. Select 3-phase timing by connecting only PWM4 to VCC.

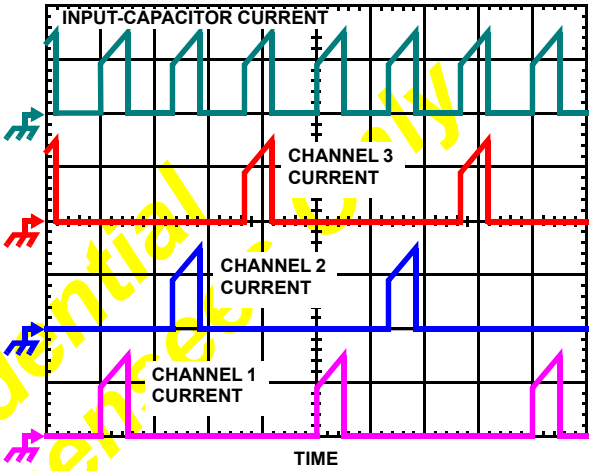


FIGURE 21. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR CURRENT FOR 3-PHASE CONVERTER

One switching cycle is defined as the time between falling PWM1 signals. The cycle time is the inverse of the switching frequency set by the resistor between the FS pin and ground. Each cycle begins when the clock signal commands the channel-1 PWM output to go low. The PWM1 transition signals the channel-1 MOSFET driver to turn off the channel-1 upper MOSFET and turn on the channel-1 synchronous MOSFET. If two-channel operation is selected, the PWM2 pulse terminates 1/2 of a cycle later. If three channels are selected, the PWM2 pulse terminates 1/3 of a cycle after PWM1, and the PWM3 output will follow after another 1/3 of a cycle. When four channels are selected, the pulse termination times are spaced in 1/4 cycle increments.

Once a PWM signal transitions low, it is held low for a minimum of 1/3 switching cycle. This forced off-time is required to ensure an accurate current sample, as described in *Current Sampling*. Once the forced off-time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal V_{COMP}, minus the current correction signal relative to the sawtooth ramp, as illustrated in Figure 19. For balanced channel current, the current correction signal is zero, and when the sawtooth ramp crosses the modified V_{COMP} voltage, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal, turns off the synchronous MOSFET, and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sampling

During the forced off-time, following a PWM transition low, the associated channel current sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. No matter the current sense method employed, the sense current (I_{SEN}) is simply a scaled version of the inductor current. The sample window time, t_{SAMPLE}, is fixed and equal to 1/3 of the switching period, t_{SW} as illustrated in Figure 22.

$$t_{SAMPLE} = \frac{t_{SW}}{3} = \frac{1}{3 \cdot f_{SW}} \quad \text{(EQ. 3)}$$

The sample current, at the end of the t_{SAMPLE}, is proportional to the inductor current and held until the next switching period sample. The sample current is used for current balance, load-line regulation, and over-current protection.

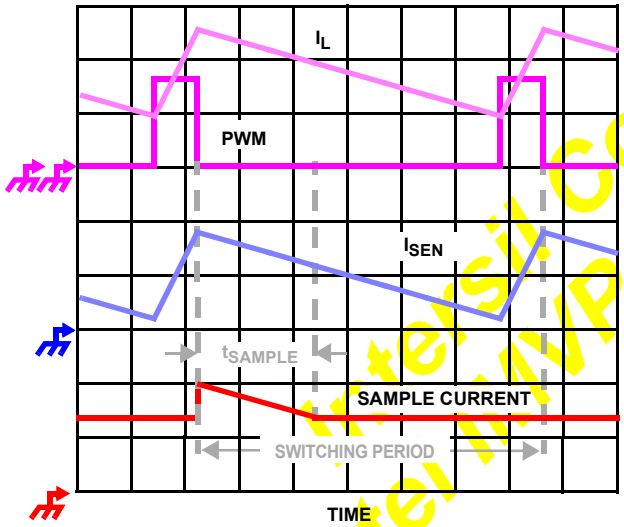


FIGURE 22. SAMPLE AND HOLD TIMING

Current Sensing

The ISL6247 supports inductor DCR sensing, MOSFET $R_{DS(ON)}$ sensing, or resistive current sensing techniques. The internal circuitry, shown in Figures 23, 24, and 25, represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM3 and PWM4 pins, as described in the *PWM Operation* section.

INDUCTOR DCR SENSING

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 23. The channel current I_L, flowing through the inductor, will also pass through the DCR. Equation 4 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 4)}$$

A simple R-C network across the inductor extracts the DCR voltage, as shown in Figure 23.

The voltage on the capacitor V_C, can be shown to be proportional to the channel current I_L, see Equation 5.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot RC + 1)} \cdot DCR \cdot I_L \quad \text{(EQ. 5)}$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant, then V_C is equal to the voltage drop across the DCR.

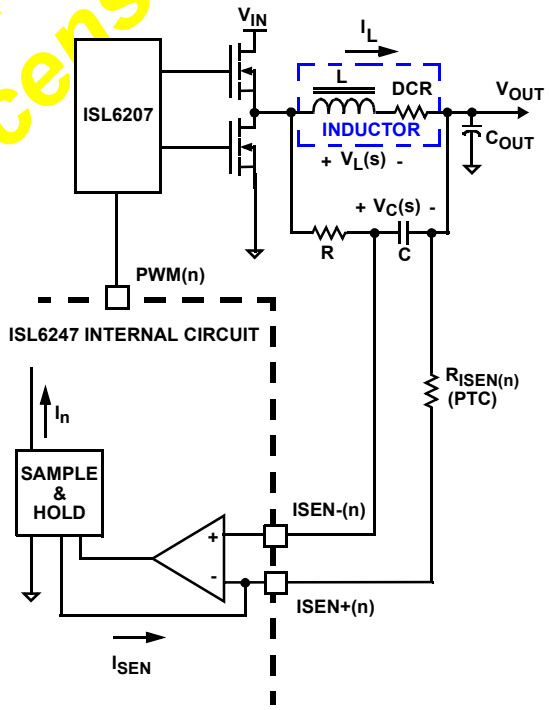


FIGURE 23. DCR SENSING CONFIGURATION

The capacitor voltage V_C, is then replicated across the sense resistor R_{ISEN}. The current through the sense resistor is proportional to the inductor current. Equation 6 shows the proportion between the channel current and the sensed current (I_{SEN}) is driven by the value of the sense resistor chosen and the DCR of the inductor.

$$I_{SEN} = 1.3 \cdot I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 6)}$$

DCR varies with temperature, so a Positive Temperature Coefficient (PTC) resistor should be selected for the sense resistor R_{ISEN}.

RESISTIVE SENSING

Independent current sensing chip resistors in series with each output inductor can serve as the sense element, as shown in Figure 24. This technique reduces overall converter efficiency due to the addition of a lossy element directly in the output path.

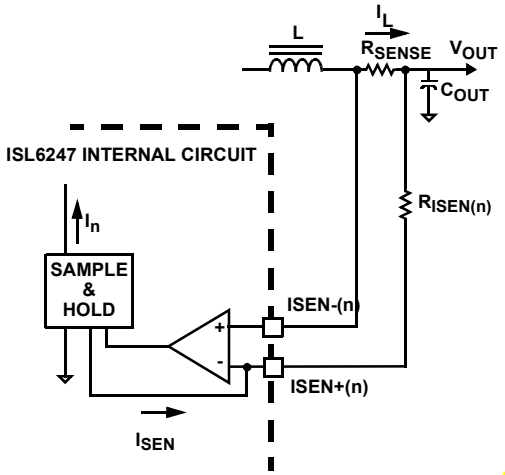


FIGURE 24. SENSE RESISTOR IN SERIES WITH INDUCTORS

The voltage across R_{ISEN} is equivalent to the voltage drop across the current sensing chip resistor, R_{SENSE}. The resulting current into the ISEN+ pin is proportional to the channel current I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 24, Equation 7 derives I_{SEN} relative to the ratio between the current sensing chip resistor and the ISEN resistor to the channel current I_L.

$$I_{SEN} = 1.3 \cdot I_L \frac{R_{SENSE}}{R_{ISEN}} \quad \text{(EQ. 7)}$$

One significant advantage of employing high quality current sensing chip resistors is their tight resistance tolerance over a wide operating temperature range. Typical converter temperature ranges fall well within this range and remove the need for any temperature correction.

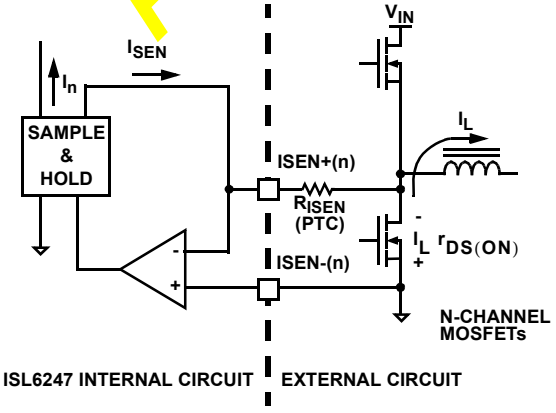


FIGURE 25. MOSFET $R_{DS(ON)}$ CURRENT-SENSING CIRCUIT

MOSFET $R_{DS(ON)}$ SENSING

The controller can also sense the channel load current by sampling the voltage across the lower MOSFET $r_{DS(ON)}$, as shown in Figure 25. The amplifier is ground-reference by connecting the ISEN- input to the source of the lower MOSFET. ISEN+ connects to the PHASE node through a resistor R_{ISEN}. The voltage across R_{ISEN} is equivalent to the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET while it is conducting. The resulting current into the ISEN+ pin is proportional to the channel current I_L. The ISEN current is sampled and held as described in the *Current Sampling* section. From Figure 25, Equation 8 derives I_{SEN} based on $r_{DS(ON)}$ of the lower MOSFET and the channel current I_L.

$$I_{SEN} = 1.3 \cdot I_L \frac{r_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 8)}$$

Since MOSFET $r_{DS(ON)}$ increases with temperature, a PTC resistor should be chosen for R_{ISEN} to compensate for this change.

Channel-Current Balance

The sampled currents from each active channel are summed together and divided by the number of active channels. The resulting cycle average current I_{AVG}, provides a measure of the total load current demand on the converter during each switching cycle. Channel current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse-width based on the error. Intersil's patented current-balance method is illustrated in Figure 26, with error correction for channel 1 represented. In the figure, the cycle average current combines with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.

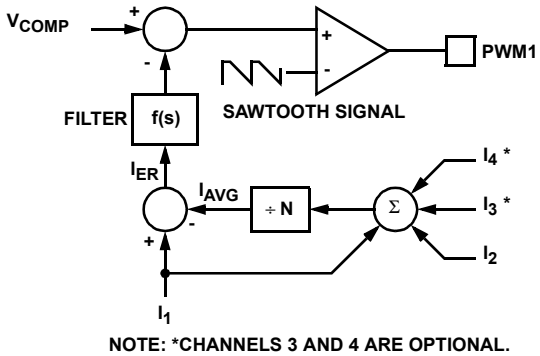


FIGURE 26. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Channel current balance is essential in realizing the thermal advantage of multi-phase operation. The heat generated in down converting is dissipated over multiple devices and a greater area. The designer avoids the complexity of driving multiple parallel MOSFETs, and the expense of using heat sinks and nonstandard magnetic materials.

Voltage Regulation

The output of the error amplifier V_{COMP}, is compared to the sawtooth waveform to modulate the pulse width of the PWM signals, as shown in Figure 26. The PWM signals control the timing of the external Intersil MOSFET drivers and regulate the converter output voltage. The regulation level of the output voltage is determined by the mode of operation signaled by the processor, see the *Modes Of Operation* section for more detail.

FEED-FORWARD RAMP COMPENSATION

The ISL6247 features a RAMPADJ pin for setting the pulse width modulator gain. The RAMPADJ voltage is set by a resistor divider network from the battery voltage, as illustrated in Figure 27. The RAMPADJ voltage sets the peak-to-peak voltage of the ramp oscillator relative to the battery voltage. By feeding the battery voltage forward, the pulse width modulation gain, G_{mod}, is independent of battery voltage, see Equation 9.

$$G_{mod} = \frac{d_{MAX} \cdot V_{BATTERY}}{\frac{R_{ADJ2}}{R_{ADJ1} + R_{ADJ2}} \cdot V_{BATTERY}} = \frac{2/3}{\frac{1}{9}} = 6.0 \quad \text{(EQ. 9)}$$

The ramp modulator gain is then set by the ratio of the maximum duty cycle, d_{MAX}, to the amount of attenuation programmed by the resistor network on the RAMPADJ pin. For IMVP-5 applications, select R_{ADJ1} to be 8 times the value of R_{ADJ2} for an 1/9 attenuation of the battery voltage, resulting in a constant pulse width modulator gain of 6.0 over the entire range of battery voltage.

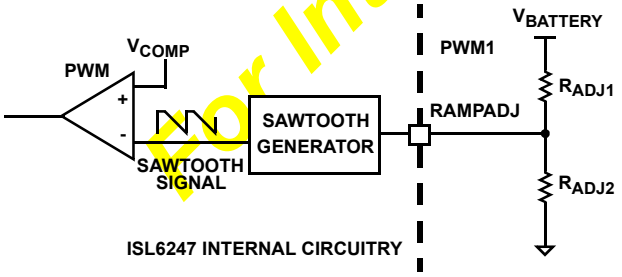


FIGURE 27. BATTERY VOLTAGE FEED-FORWARD COMPENSATION

REFERENCE VOLTAGE SELECTION

The reference voltage applied to the non-inverting input of the error amplifier is set by an internal multiplexer, as shown in Figure 28. The multiplexer selects one of three modes of operation: Active, Deep Sleep, or Deeper Sleep. Depending on the mode selected, the multiplexer applies one of three user programmed voltage levels to the non-inverting input of the error amplifier. During mode changes, the voltage transition from one level to the next is managed by the soft-start circuitry. The output voltage transitions linearly from one level to the next.

In Active mode, a digital-to-analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID0 through VID5. The DAC decodes the 6-bit voltage identification codes (VID) into one of the discrete voltages shown in Table 1. Each VID pin is pulled to 0.95V by an internal 50µA current source and accepts open-collector, open-drain, or standard low-voltage TTL or CMOS signals.

Deep Sleep mode is entered when the DSEN# signal from the processor is a logic low and DRSEN is low. The multiplexer switches the reference voltage to the voltage level externally programmed on the DSV pin. The soft-start circuitry linearly transitions the reference voltage from the Active mode DAC level to the new Deep Sleep mode DSV level. When the DSEN# signal returns to a logic high, the reference voltage linearly transitions to the DAC voltage programmed by the VID pins.

The Deeper Sleep mode is entered when the DRSEN signal goes high and DSEN# is low. The multiplexer then switches the reference voltage to the voltage level externally programmed on the DRSV pin. The reference voltage transitions linearly due to the soft-start circuitry from the DSV level to the DRSV level. When the DRSEN level returns low, the reference voltage is returned to the Deep Sleep mode DSV level.

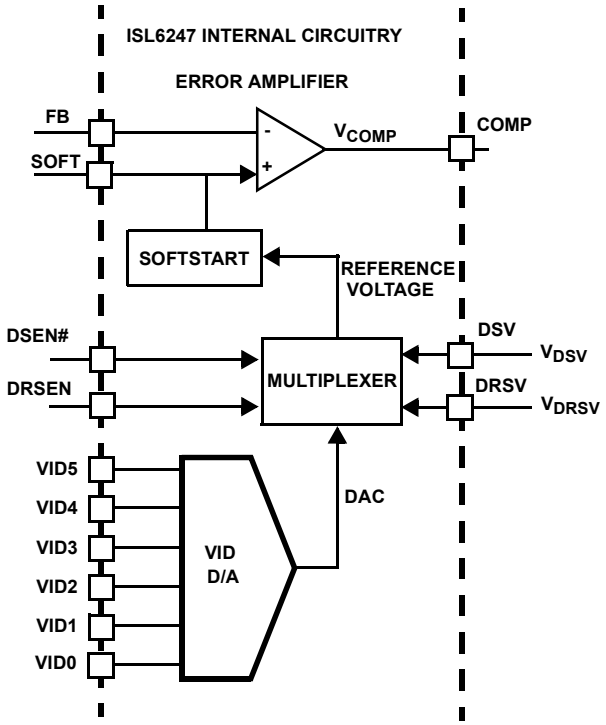


FIGURE 28. REFERENCE VOLTAGE MULTIPLEXER CONNECTIONS

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID5	VDAC
0	1	0	1	0	0	0.8375V
0	1	0	0	1	1	0.8500V
0	1	0	0	1	0	0.8625V
0	1	0	0	0	1	0.8750V
0	1	0	0	0	0	0.8875V
0	0	1	1	1	1	0.9000V
0	0	1	1	1	0	0.9125V
0	0	1	1	0	1	0.9250V
0	0	1	1	0	0	0.9375V
0	0	1	0	1	1	0.9500V
0	0	1	0	1	0	0.9625V
0	0	1	0	0	1	0.975V0
0	0	1	0	0	0	0.9875V
0	0	0	1	1	1	1.0000V
0	0	0	1	1	0	1.0125V
0	0	0	1	0	1	1.0250v
0	0	0	1	0	0	1.0375V
0	0	0	0	1	1	1.0500V
0	0	0	0	1	0	1.0625V
0	0	0	0	0	1	1.0750V
0	0	0	0	0	0	1.0875V
1	1	1	1	1	1	OFF
1	1	1	1	1	0	OFF
1	1	1	1	0	1	1.1000V
1	1	1	1	0	0	1.1125V
1	1	1	0	1	1	1.1250V
1	1	1	0	1	0	1.1375V
1	1	1	0	0	1	1.1500V
1	1	1	0	0	0	1.1625V
1	1	0	1	1	1	1.1750V
1	1	0	1	1	0	1.1875V
1	1	0	1	0	1	1.2000V
1	1	0	1	0	0	1.2125V
1	1	0	0	1	1	1.2250V
1	1	0	0	1	0	1.2375V
1	1	0	0	0	1	1.2500V
1	1	0	0	0	0	1.2625V
1	0	1	1	1	1	1.2750V
1	0	1	1	1	0	1.2875V
1	0	1	1	0	1	1.3000V

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID5	VDAC
1	0	1	1	0	0	1.3125V
1	0	1	0	1	1	1.3250V
1	0	1	0	1	0	1.3375V
1	0	1	0	0	1	1.3500V
1	0	1	0	0	0	1.3625V
1	0	0	1	1	1	1.3750V
1	0	0	1	1	0	1.3875V
1	0	0	1	0	1	1.4000V
1	0	0	1	0	0	1.4125V
1	0	0	0	1	1	1.4250V
1	0	0	0	1	0	1.4375V
1	0	0	0	0	1	1.4500V
1	0	0	0	0	0	1.4625V
0	1	1	1	1	1	1.4750V
0	1	1	1	1	0	1.4875V
0	1	1	1	0	1	1.5000V
0	1	1	1	0	0	1.5125V
0	1	1	0	1	1	1.5250V
0	1	1	0	1	0	1.5375V
0	1	1	0	0	1	1.5500V
0	1	1	0	0	0	1.5625V
0	1	0	1	1	1	1.5750V
0	1	0	1	1	0	1.5875V
0	1	0	1	0	1	1.6000V

OUTPUT VOLTAGE FEEDBACK

The output voltage sense points for the converter are connected to the VSEN and VRTN inputs of an internal differential amplifier. By remote sensing the output voltage relative to its local ground, the differential amplifier eliminates voltage differences between the local ground of the controller and the remote sense point, providing a more accurate means of sensing output voltage. The remote-sense amplifier output V_{DIFF}, is then tied through an external resistor, R_{FB}, to the inverting input of the error amplifier; see the circuit illustration in Figure 29.

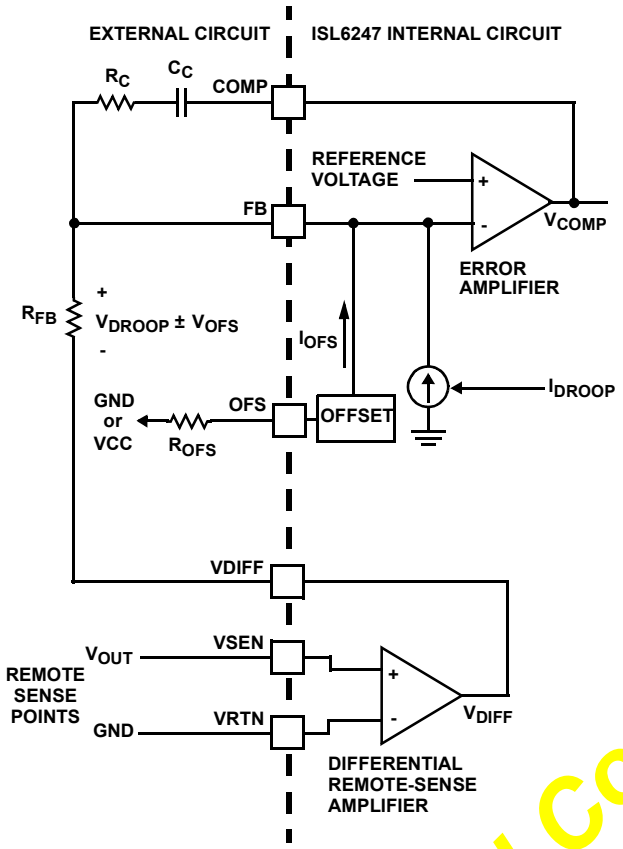


FIGURE 29. INVERTING INPUT CONNECTIONS

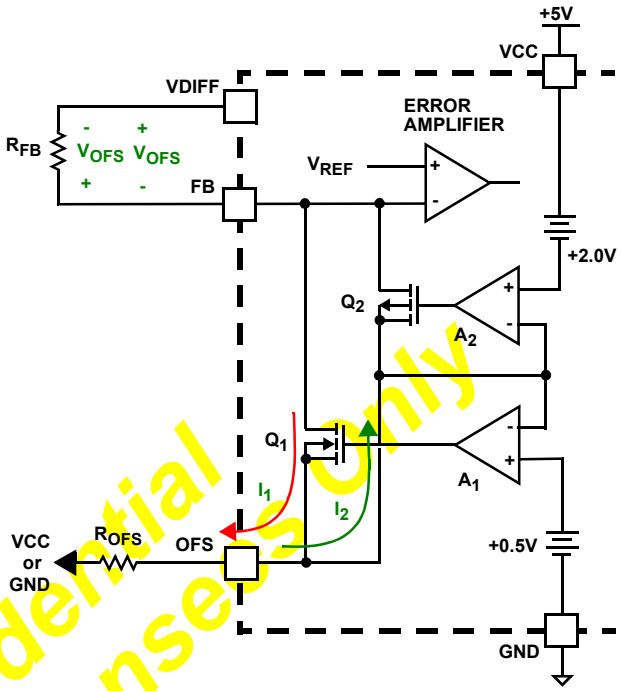


FIGURE 30. REFERENCE OFFSET CIRCUITRY

LOAD-LINE REGULATION

The ISL6247 meets the load-line requirements of Intel IMVP 5 processors by programming the output as a function of load current. The individual sample currents of all active channels I_{SEN}, are summed together and divided by four, see Figure 19. The resulting droop current I_{DROOP}, is proportional to the total output current of the converter and independent of the number of active channels. Droop current is mirrored internally and carried to the inverting input of the error amplifier. The droop current is forced out the FB pin and creates a voltage drop across the feedback resistor R_{FB}, proportional to the output current; see Figure 29. The resulting steady-state value of output voltage droop is:

$$V_{DROOP} = \sum_{(i=1)}^{N} I_{SEN} \cdot \frac{1}{4} \cdot R_{FB} \quad \text{(EQ. 10)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 10 with the appropriate sample current expression defined by the current sense method employed.

$$V_{OUT} = V_{REF} - V_{OFS} - \left[1.3\left(\frac{I_{OUT}}{4} \cdot \frac{R_X}{R_{ISEN}}\right) + I_{SEN_{OFFSET}}\right] \cdot RFB \quad \text{(EQ. 11)}$$

Where V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the sense resistor in the ISEN line, and R_{FB} is the feedback resistor. R_X has a value of DCR, $r_{DS(ON)}$, or R_{SENSE}, depending on the sensing method. $I_{SEN_{OFFSET}}$ is defined in the section titled *Sample Method Offset Resolution*.

REFERENCE OFFSET

Typical microprocessor tolerance windows are centered around a nominal DAC VID set point. Implementing a load-line can require offsetting the output voltage above or below this nominal reference voltage. This allows centering of the load-line within the static specification window. The ISL6247 features an proprietary offset circuit which allows the user to select a single resistor to set a desired fixed offset, as shown in Figure 30.

Negative Offset Below The Reference Voltage

For IMVP-5 applications, the tolerance window is centered below the nominal reference voltage, requiring a negative offset. By connecting R_{OFS} to VCC, a negative output offset is programmed. Amplifier A_2 forces the voltage on OFS to (VCC - 2V), and this sets the current I_2 flowing through R_{OFS} (per Equation 12), and I_2 flows out the FB pin. This current creates a voltage across R_{FB}, which causes a regulated output voltage that is V_{OFS} below the reference voltage.

$$I_2 = \frac{2V}{R_{OFS}} = \frac{|V_{OFS}|}{R_{FB}} \quad \text{(EQ. 12)}$$

Rearranging Equation 12, select the resistor value based on the voltage offset desired using Equation 13.

$$R_{OFS} = \frac{2V \cdot R_{FB}}{|V_{OFS}|} \quad \text{(EQ. 13)}$$

Positive Offset Above The Reference Voltage

For a positive offset of the output voltage, connect the offset resistor, R_{OFS}, to ground. By connecting the external resistor to ground, amplifier A_1 forces the voltage on OFS to +0.5V. This results in a known current I_1, flowing through R_{OFS} (see Equation 14) which is pulled out of the FB pin. This creates an offset voltage V_{OFS}, across R_{FB}, as shown in Figure 30, reducing the voltage at the inverting input of the error amplifier relative to the magnitude of I_1.

$$I_1 = \frac{0.5V}{R_{OFS}} = \frac{V_{OFS}}{R_{FB}} \quad \text{(EQ. 14)}$$

Using the relationship between the current set by R_{OFS} and the voltage offset created by this current through R_{FB}, Equation 15 results for selection of R_{OFS}.

$$R_{OFS} = \frac{0.5V \cdot R_{FB}}{V_{OFS}} \quad \text{(EQ. 15)}$$

The integrating compensation network (R_C and C_C), shown in Figure 29, assures that the steady-state error in the output voltage is minimized. The ISL6247 system accuracy, specified in the *Electrical Specification Table*, includes all variations in current sources, amplifiers and the DAC reference over temperature.

Sample Method Offset Resolution

A sample current offset results from the timing scheme of the sampling method, see the *Current Sampling* section for more detail. The sample current translates to a droop current offset derived in Equation 16. Adjust the R_{OFS} value accordingly to account for this offset.

$$I_{SEN_{OFFSET}} = 1.3 \cdot \frac{V_{OUT}}{L \cdot fws} \cdot \left[\frac{1}{6} - \frac{d}{2}\right] \cdot \frac{R_X}{R_{ISEN}} \quad \text{(EQ. 16)}$$

Where V_{OUT} is the output voltage, f_{sw} is the switching frequency, and d is the duty cycle.

Switching Frequency

Resistor R_{FS}, connected between the FS pin and ground, sets the frequency of the internal oscillator. Figure 31 provides a graph of oscillator frequency vs. R_{FS}. The maximum recommended channel frequency is 1.0MHz.

During the selection process, attention should be paid to the MOSFET loss calculations which establish the upper limit for the switching frequency. The requirements for fast-transient response and small output voltage ripple establish the lower limit. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

FIGURE 31. R_{FS} vs SWITCHING FREQUENCY

Once a switching frequency value is chosen, use Equation 17 to select the value of R_{FS} (Ω), where f_{SW} is in Hertz.

$$R_{FS} = 10^{[11.15 - 1.13\log(f_{SW})]} \quad \text{(EQ. 17)}$$

Operation Initialization

Converter operation is initialized with a soft-start interval. Once the output voltage is within the proper window of operation, the PGOOD output changes state to update an external system monitor.

Enable and Disable

The PWM outputs are held in a high-impedance state, which insures the ISL6207 drivers remain off while in shutdown mode. Three separate input conditions must be met before the ISL6247 is released from shutdown mode (Figure 32).

First, the internal power-on reset circuit (POR) prevents the ISL6247 from starting before the bias voltage at VCC reaches the POR-rising threshold, as defined in *Electrical Specifications*. The POR-rising threshold is high enough to guarantee that all parts of the controller can perform their functions properly. Built-in hysteresis between the rising and falling thresholds insures that once enabled, the controller will not inadvertently turn off unless the bias voltage drops substantially. When VCC is below the POR-rising threshold, the PWM outputs are held in a high-impedance state to assure the drivers remain off.

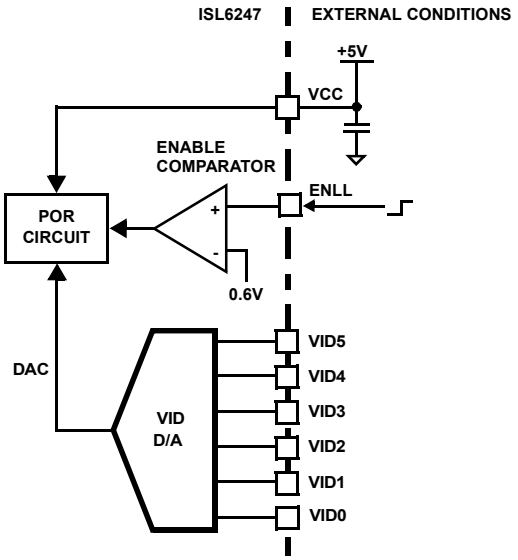


FIGURE 32. ENABLE AND DISABLE INPUTS

After power on, the ISL6247 remains in shut-down mode until the voltage at the enable input ENLL, rises above the enable threshold. Once this threshold is exceeded, the controller will start up, given all the enable inputs are in the proper state.

The 111111 and 011111 VID codes are reserved as signals to the controller that no load is present. The controller will latch and enter shutdown mode after receiving this code.

To enable the controller, VCC must be greater than the POR threshold, the voltage on ENLL must be greater than the enable threshold, and VID cannot be equal to 111111 or 011111. Once these conditions are true, the controller immediately initiates a soft-start sequence.

Soft-Start Interval

Once the ISL6247 is enabled, a capacitor, C_{SOFT}, must be present between the SOFT pin and ground as shown in Figure 33. Two internal current sources, which flow out the SOFT pin, charge the capacitor at two distinct rates. The

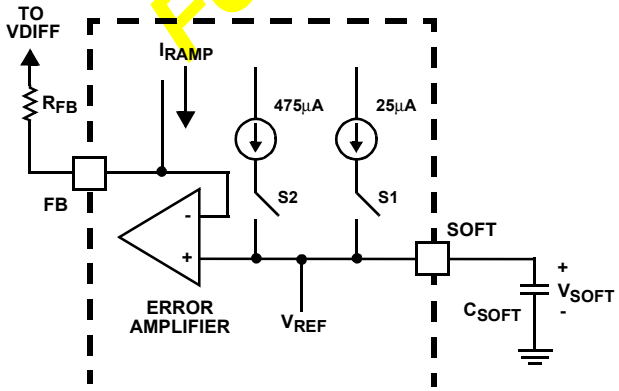


FIGURE 33. SOFT-START SLEW RATE CONTROL

voltage on the SOFT pin provides a slow rising reference voltage to the non-inverting input of the error amplifier. A controlled rise in output voltage avoids encountering an over-current condition, described in *Fault Monitoring and Protection*, by slowly charging the discharged output capacitors.

In Figure 34, a soft-start interval is illustrated from start to finish. The first interval, from t_1 to t_2, is a wait period for the soft-start circuitry to initialize. Equation 18 shows the wait period in terms of switching frequency.

$$t_{1-2} = 32 \cdot \frac{1}{f_{SW}} \quad \text{(EQ. 18)}$$

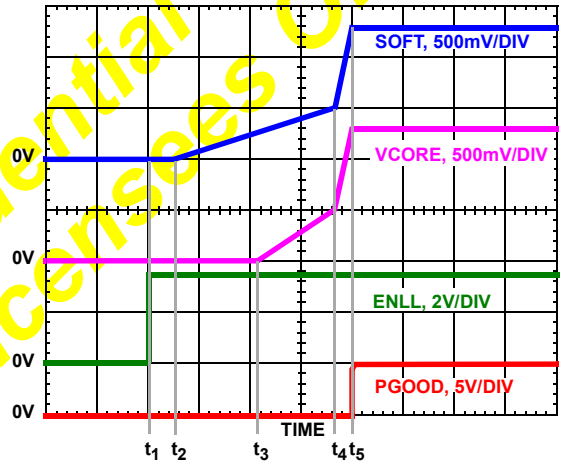


FIGURE 34. SOFT-START INTERVAL WAVEFORMS

Once the wait period has expired, the second interval, from t_2 to t_4, begins. Switch S1 closes and a 25µA current source begins charging the C_{SOFT} capacitor. Simultaneously, a current I_{RAMP} begins flowing out the FB pin. I_{RAMP} linearly ramps from 140 to 0µA over the same time span V_{SOFT} rises from 0 to 0.5V. During the sub-interval t_2 to t_3, the offset voltage across R_{FB}, due to I_{RAMP}, is greater than V_{SOFT}. Once V_{SOFT} exceeds this offset, the first PWM pulses are produced and the output voltage linearly slews to 0.5V. Second interval duration is based on the charging time of C_{SOFT} to 0.5V; see Equation 19.

$$t_{2-4} = \frac{(0.5V)(C_{SOFT})}{25\mu A} \quad \text{(EQ. 19)}$$

The final interval of the soft-start interval, t_4 to t_5, begins with switch S2 closing. The second current source adds to the first, for a total charging current of 500µA. The I_{RAMP} current has expired and the output voltage follows the voltage rise on C_{SOFT}. When V_{SOFT} reaches the VID programmed reference voltage, switches S1 and S2 open. Equation 20 defines the third interval of the soft-start interval.

$$t_{4-5} = \frac{(VID - 0.5V)(C_{SOFT})}{500\mu A} \quad \text{(EQ. 20)}$$

The total soft-start interval is the sum of Equations 18, 19, 20. Selection of the soft-start capacitor is driven by the maximum slew rate in (V/s) required by the IMVP-5 specification, addressed in *Modes of Operation*.

Once the output voltage rises above 90% of the VID setting, the power good signal (PGOOD) changes to a high state, as shown in Figure 34. Once high, PGOOD will only transition low when the controller is disabled or a fault condition is detected. See the *Power Good Signal* sub-section of the *Fault Monitoring and Protection* section for additional information on the capability of this pin.

Modes of Operation

The ISL6247 supports power state optimization transitions per the IMVP-5 specification for Fixed Mobile Solutions (FMS). Three distinct modes of operation, signaled by the processor, are determined by the state of the STP_CPU# and DPRSLPVR signals. These inputs connect to DSEN# and DRSEN respectively and cycle the controller through Active, Deep Sleep, and Deeper Sleep modes as shown in Figure 35.

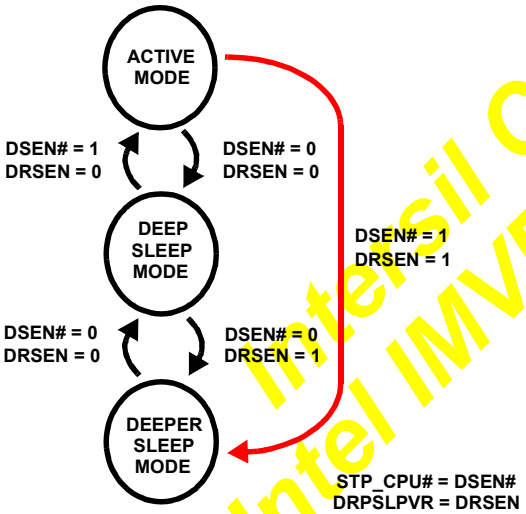


FIGURE 35. POWER OPTIMIZATION STATES

Active Mode

When DSEN# is high and DRSEN is low, active mode is selected by the processor. The ISL6247 determines the output voltage from the processor controlled VID codes. The corresponding DAC voltage provides the reference voltage, V_{REF}, to the error amplifier and consequently the converter output voltage.

The ISL6247 supports Enhanced Intel SpeedStep transitions, designed to maximize processor performance in notebook systems. When the notebook power source is changed from an AC outlet to a battery, the processor drops to a lower operation voltage. The processor communicates this change by adjusting the VID codes. The ISL6247 detects the VID change and immediately begins slewing the output voltage to the new setting. Figure 36 illustrates a VID

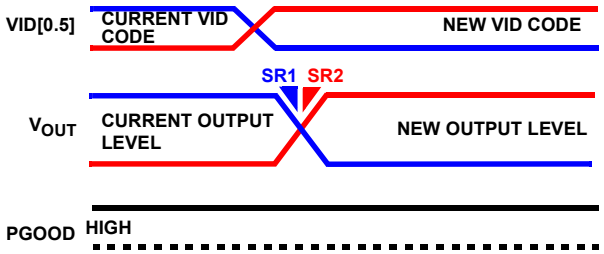


FIGURE 36. SPEEDSTEP OUTPUT VOLTAGE CHANGE

change in either direction. The slew rate in either direction, SR1 and SR2, is equivalent and set by the SOFT capacitor.

Slew Rate Selection

The IMVP-5 timing requirements define the minimum slew rate during a set VID change. Referencing Figure 33, the size of the SOFT capacitor sets the maximum slew rate of the ISL6247. Equation 21 outlines how to select the capacitor based on the slew rate (V/s) targeted.

$$C_{SOFT} = \frac{SOFT_{SlewCurrent}}{SlewRate} \quad \text{(EQ. 21)}$$

Take into account the capacitor tolerance when sizing C_{SOFT} to prevent violation of the IMVP-5 minimum timing specification, where SlewRate is defined in the IMVP-V specification.

Deep Sleep Mode

While in active mode, the controller monitors the state of the mode selection pins. When DSEN# goes low, the ISL6247 enters deep sleep mode. An internal multiplexer changes the reference voltage to the deep sleep voltage level externally set on the DSV pin. The converter immediately begins slewing the output voltage to the deep sleep voltage. The output voltage slew rate into and out of deep sleep mode (SR1 and SR2) is equivalent to the SpeedStep transition. Active to deep sleep mode transition and vice versa is shown in Figure 37.

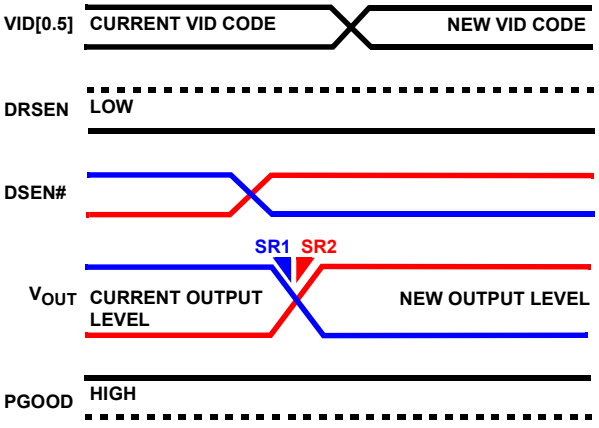


FIGURE 37. DEEP SLEEP STATE TIMING

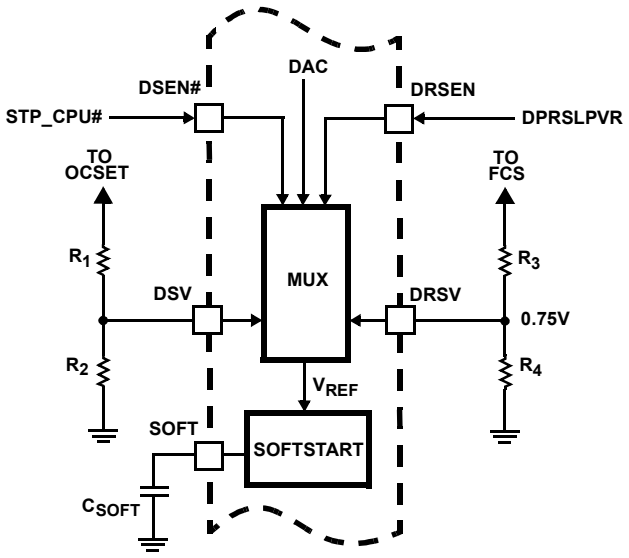


FIGURE 38. REFERENCE VOLTAGE SELECTION

Figure 38 illustrates the multiplexing between the three modes of operation and the reference voltage. A resistor divider from the OCSET pin is shown for selection of the deep sleep voltage. Using this configuration, the DSV level is proportional to the DAC, since the OCSET voltage is the DAC voltage.

Deeper Sleep Mode

Once in deep sleep mode, a high on DRSEN signals entry into deeper sleep mode. The controller immediately switches to single-phase operation and the multiplexer makes the reference voltage the deeper sleep voltage level, DRSV. Current feedback from the previously active channels and the VID inputs are ignored by the controller while in this mode. The SOFT slew current is reduced during the transition into deeper sleep mode. The voltage slew rate from DSV to DRSV is slowed as a result; see Figure 39.

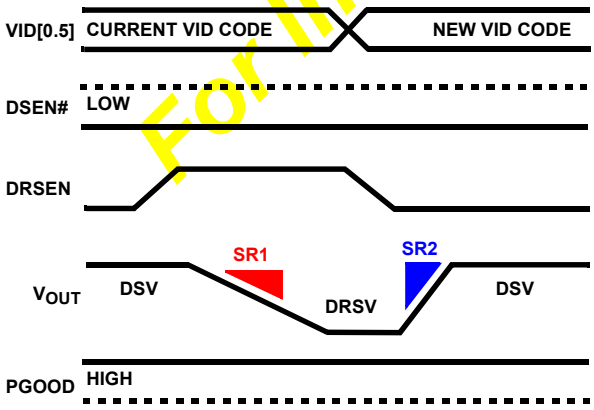


FIGURE 39. DEEPER SLEEP STATE TIMING

The controller exits deeper sleep mode when DRSEN returns low. The controller enables the previously active channels and returns the reference voltage to the DSV level. The SOFT slew current returns to the previous level of 500µA to provide the required swift re-entry into deep sleep mode.

The state diagram in Figure 35 shows a direct path from active mode to deeper sleep highlighted in red. The path is not a valid IMVP-5 state transition and will not be entered by processor controlled enable lines.

Fault Monitoring and Protection

The ISL6247 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output which indicates when the converter is operating within the IMVP-5 specifications and externally set over-current threshold. The schematic in Figure 40 outlines the interaction between the fault monitors and the PGOOD state.

PGOOD pulls low during shutdown and remains low when the controller is enabled, as described in *Enable and Disable*. During a soft-start interval, PGOOD releases high once the output voltage passes through the under-voltage (UV) rising threshold.

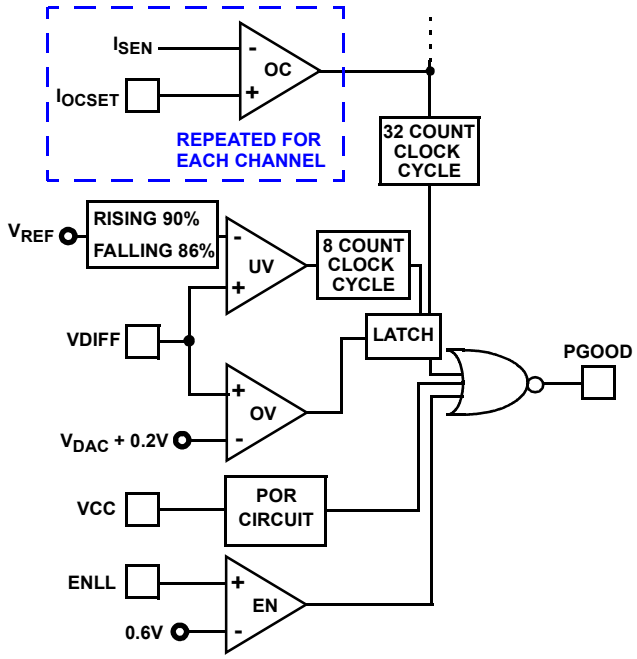


FIGURE 40. POWER GOOD DETECTION INPUTS

PGOOD transitions low immediately following ENLL descending below the enable threshold, VCC dropping below the falling POR threshold, or a SpeedStep transition to one of the no-CPU codes (011111 or 111111). PGOOD will return high following ENLL rising above the enable threshold, VCC rising above the POR rising threshold.

PGOOD pulls low and is latched when an under-voltage, over-voltage or over-current condition is detected as illustrated in Figure 40. Once latched, PGOOD will remain low until VCC is cycled below the POR falling threshold or ENLL is toggled below 0.6V.

Under-Voltage Protection

The under-voltage rising threshold is 90% of the reference voltage and the falling threshold is 86% of the reference voltage. During soft-start, the slowly rising VDIFF eventually exceeds the rising threshold and PGOOD releases high. If VDIFF drops below the falling threshold, see Figure 41, a counter begins tallying switching cycles. Once the counter reaches eight, the active PWM signals are placed in a high-impedance state and PGOOD pulls low.

If VDIFF rises above the UV rising threshold, within the 8 cycle window, the counter counts down and converter operation is not interrupted.

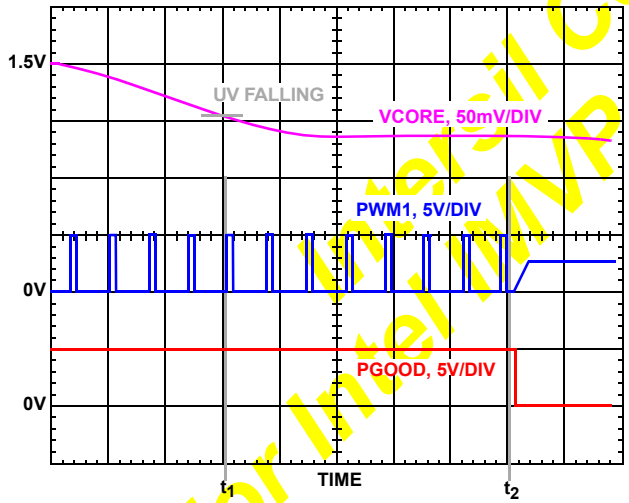


FIGURE 41. UNDER-VOLTAGE PROTECTION WAVEFORMS

Over-Voltage Protection

If VDIFF exceeds the DAC voltage by 200mV, the over-voltage comparator goes high. The change in state of the over-voltage signal prompts PGOOD to go low indicating a fault condition exists. An internal reset latch is simultaneously set to prevent a change in state of the OV signal from resetting the fault protection actions.

The protective actions begin with all PWM outputs commanded low. The ISL6207 drivers turn on the lower MOSFETs shunting the output to ground. This protection action prevents any further increase in output voltage.

Once VDIFF falls below the DAC over-voltage threshold, all PWM signals enter a high-impedance state. This prevents charge dumping of the output capacitors back through the output inductors and lower MOSFETs which would cause a negative output voltage. This architecture eliminates the need of a high-current Schottky diode on the output.

If external fault conditions cause the output voltage to rise above the over-voltage threshold again, the ISL6247 commands all PWM outputs low once again. The ISL6247 continues to protect the load in this fashion as long as the over-voltage repeats. The reset latch is cleared by cycling ENLL below the enable threshold or VCC below the POR falling threshold.

Over-Current Protection

Each active channel is protected from a sustained over-current condition. The ISL6247 takes advantage of the proportionality between the load current and the sensed current to continuously compare the channel sample current, I_{SEN}, with an externally programmed over-current trip threshold, I_{OCSET}. If any of the channel sample currents exceed I_{OCSET}, an internal 32-count up-down counter increments during each consecutive switching cycle. If a few switching cycles occur between fault detections, the counter will count down but not below zero. When the counter reaches 32, the comparator triggers the converter to shutdown and sets an internal latch preventing continued PWM operation. All PWM signals are placed in a high-impedance state commanding the ISL6207 drivers to turn off both upper and lower MOSFETs. The latch is cleared by cycling ENLL below the enable threshold or VCC below the POR falling threshold.

OCSET RESISTOR SELECTION

The programmable over-current trip threshold, illustrated in Figure 42, is set by the current flowing through the OCSET pin. The OCSET pin is held at the DAC voltage with a resistor to ground allowing for selection of I_{OCSET}. The over-current trip threshold is set relative to the scaled full load channel sense current, typically 50µA.

$$I_{OCSET} = K\left(I_{SEN_{FL}} + I_{SEN_{OFFSET}}\right) = \frac{I_{TRIP}}{I_{FL}}\left(I_{SEN_{FL}} + I_{SEN_{OFFSET}}\right) \quad \text{(EQ. 22)}$$

In Equation 22,the ratio K is set by the ratio of converter trip current, I_{TRIP}(A), to the converter full load output current, I_{FL}(A).

$$R_{OCSET} = \frac{V_{OCSET}}{I_{OCSET}} = \frac{V_{DAC}}{K\left(I_{SEN_{FL}} + I_{SEN_{OFFSET}}\right)} \quad \text{(EQ. 23)}$$

Equation 23 shows the selection criteria for R_{OCSET}. Do not add external capacitance to this pin.

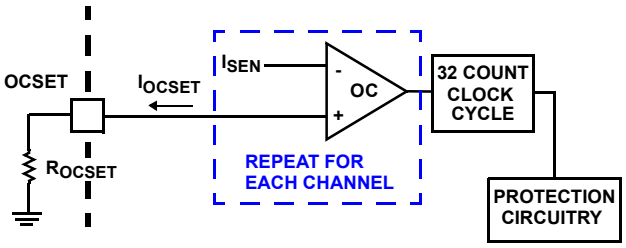


FIGURE 42. OVER-CURRENT CIRCUITRY

Voltage Regulator Thermal Throttling

Intel IMVP-5 technology supports thermal throttling of the processor to prevent catastrophic thermal damage to the voltage regulator. The ISL6247 features a thermal monitor which senses the voltage change across an externally placed negative temperature coefficient (NTC) resistor network; see Figure 43. Proper selection and placement of the NTC thermistor allows for detection of a designated temperature rise by the voltage regulator. When the temperature of the NTC thermistor reaches the prescribed level, the voltage at the NTC pin *ideally* is 0.5V. The internal comparator goes high turning on the open-drain VR-TT# pull-down. VR-TT# is connected directly to the active-low processor I/O pin named PROCHOT#. The processor's Thermal Control Circuit (TCC) is activated and thermal throttling is initiated. This function is intended to prevent catastrophic overheating of the IMVP-5 regulator components and printed wiring board (PWB). Thermal throttling by the processor degrades system performance and should not occur below normal thermal design power levels.

NTC RESISTOR NETWORK

Selection of the NTC thermistor is simplified with the addition of a second standard resistor in series, as shown in Figure 43, or in parallel, or an NTC thermistor alone. The series or parallel approach widens the standard value choices for the NTC thermistor. The NTC resistor network equivalent resistance, R_{NET}, must be equal to 12.5kΩ at the desired fault temperature. This value is set by the comparator detection threshold (0.5V) and the 40µA current source which flows out the NTC pin.

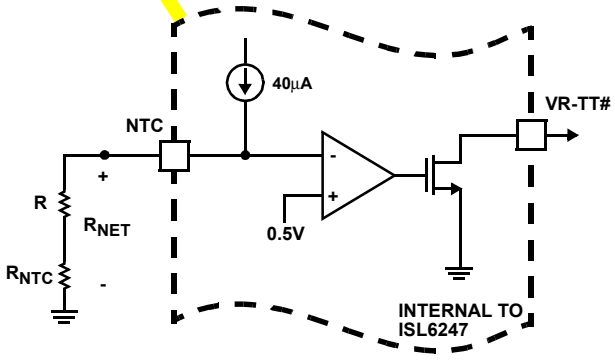


FIGURE 43. THERMAL MONITOR CIRCUITRY

The NTC thermistor resistance at room temperature, R_{25}, and a table of resistance ratios relative to R_{25} over the operating temperature range of the thermistor are provided by most manufacturers. From the thermistor resistance ratio table, follow the previously determined T_{FAULT} value across to the material tolerance type selected and determine the resistance ratio K_{FAULT} at that temperature. R_{FAULT} represents the resistance of the NTC thermistor at the selected fault temperature. Equation 24 outlines that the ratio between R_{FAULT} to R_{25} must be less than one.

$$K_{FAULT} = \frac{R_{FAULT}}{R_{25}} < 1 \qquad \text{(EQ. 24)}$$

The standard resistor value to place in series with the selected NTC thermistor is derived in Equation 25.

$$R = R_{NET} - R_{FAULT} = 12.5k\Omega - (R_{25} \cdot K_{FAULT}) \qquad \text{(EQ. 25)}$$

Application Information

Component Selection Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of material, and example board layouts specifically for IMVP-5 applications.

Power Stages

The first step in designing a multi-phase converter is to determine the number of phases. This determination depends heavily on the cost analysis which in turn depends on system constraints that differ from one design to the next. Generally speaking, the most economical solutions are those in which each phase handles between 15 and 20A. In cases where board space is the limiting constraint, current can be pushed as high as 30A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces. Intel IMVP-5 platforms require between 68A to 80A, which suggests converter designs with 3 to 4 channel operation.

MOSFET SELECTION AND CONSIDERATIONS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct; the switching frequency; the capability of the MOSFETs to dissipate heat; and the availability and nature of heat sinking and air flow. The power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between upper and lower MOSFETs according to duty cycle of the converter. Refer to the P_{UPPER} and P_{LOWER} equations below. The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFETs have significant switching losses, since the lower devices turn on and off into near zero voltage.

The following equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFETs body diode. The gate-charge losses are dissipated in the ISL6207 drivers and do not heat the MOSFETs; however, large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature, at high ambient temperature, by calculating the temperature rise according to package thermal-resistance specifications.

$$P_{LOWER} = \frac{I_o^2 \cdot R_{DS(ON)} \cdot (V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 26)}$$

$$P_{UPPER} = \frac{I_o^2 \cdot R_{DS(ON)} \cdot V_{OUT}}{V_{IN}} + \frac{I_O \cdot V_{IN} \cdot t_{SW} \cdot F_{SW}}{2}$$

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

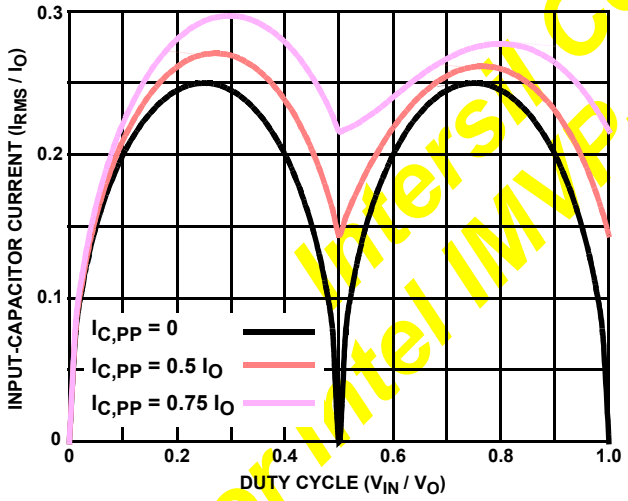


FIGURE 44. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

For a two-phase design, use Figure 44 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the combined peak-to-peak inductor current ($I_{C,PP}$) to I_O. Select a bulk capacitor with a ripple current rating which will minimize the total number of input capacitors required to support the RMS current calculated. The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage. Figures 45 and 46 provide the same input RMS current information for three and four phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

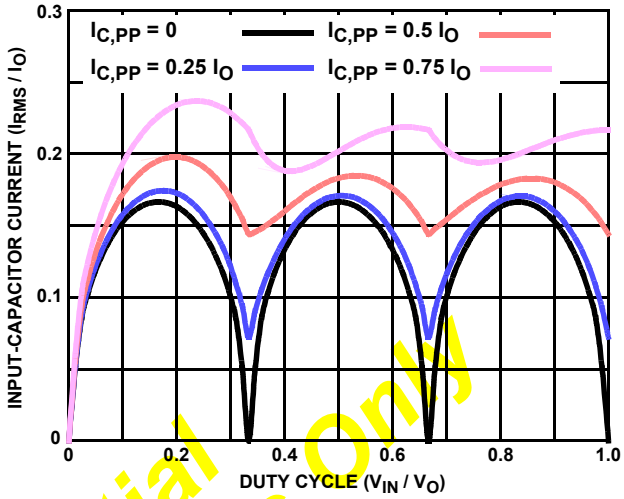


FIGURE 45. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

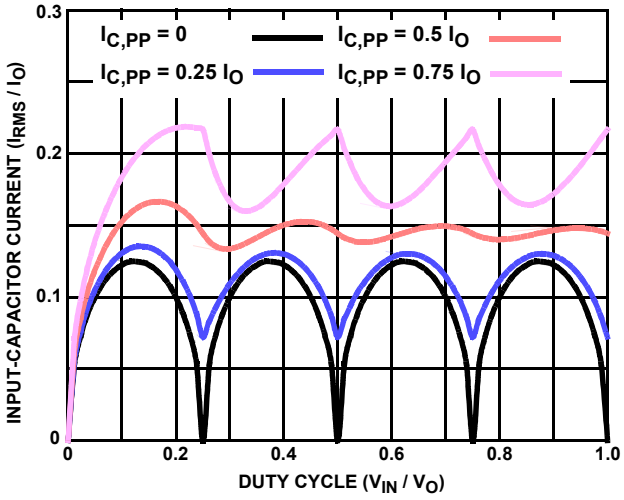


FIGURE 46. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 4-PHASE CONVERTER

Output Inductor Selection

The output inductor is selected to meet the voltage ripple requirements and minimize the converter response time to a load transient. In a multiphase converter topology, the ripple current of one active channel partially cancels with the other active channels to reduce the overall ripple current. The reduction in total output ripple current results in lower overall output voltage ripple.

The inductor selected for the power channels determines the channel ripple current. Increasing the value of inductance

reduces the total output ripple current and total output voltage ripple. However, increasing the inductance value will slow the converter response time to a load transient.

One of the parameters limiting the converter response time to a load transient is the time required to slew the inductor current from its initial current level to the transient current level. During this interval, the difference between the two levels must be supplied by the output capacitance. Minimizing the response time can minimize the output capacitance required.The channel ripple current is approximated in Equation 27.

$$\Delta I_{CHANNEL} = \frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}} \cdot \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 27)}$$

The total output ripple current can be determined from the curves in Figure 47. The curves are a function of the duty cycle and number of active channels, normalized to the parameter K_{NORM} at zero duty cycle.

$$K_{NORM} = \frac{V_{OUT}}{L \cdot f_{SW}} \quad \text{(EQ. 28)}$$

Where L is the channel inductor value.

Find the intersection of the active channel curve and duty cycle for your particular application. Find the corresponding ripple current multiplier from the y-axis. Multiply the K_{CM} value, found from Figure 47, by the normalization factor K_{NORM}, calculated per Equation 28. The result is the total output ripple current for the given application as shown in Equation 29.

$$\Delta I_{TOTAL} = K_{NORM} \cdot K_{CM} \quad \text{(EQ. 29)}$$

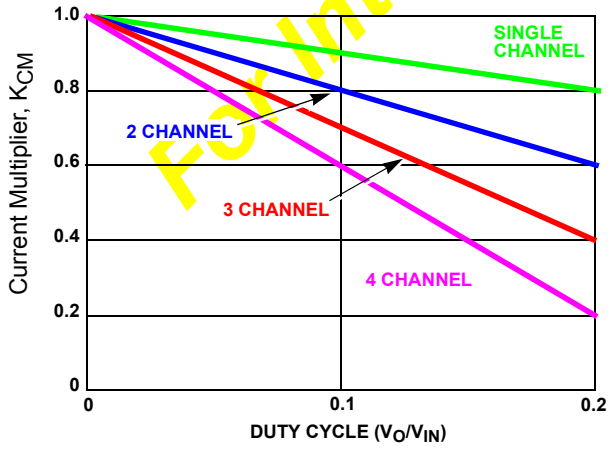


FIGURE 47. RIPPLE CURRENT vs DUTY CYCLE

Output Capacitor Selection

In high-speed converters, the output capacitor bank is usually the most costly part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI; the load-current slew rate, di/dt; and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, Equivalent Series Resistance (ESR), and Equivalent Series Inductance (ESL).

Typical output capacitor solutions are made up of a mixture of low-capacitance ceramics along with high-capacitance aluminum electrolytic or special polymer bulk capacitors. At the beginning of a load transient, the ceramic capacitors supply the initial transient current and slow the rate-of-change seen by the bulk capacitors. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL.

As the load current increases, the voltage drop across the bulk capacitor ESR increases linearly until the load current reaches it final value. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by the amount derived in Equation 30. The filter capacitor must have sufficiently low ESL and ESR such that $\Delta V < \Delta V_{MAX}$.

$$\Delta V = ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \quad \text{(EQ. 30)}$$

Intel IMVP-5 specifications outline the total number and type of output capacitors to support the transient slew rates produced by the processor.

Layout Considerations

Careful printed circuit board (PCB) layout is critical in high-frequency switching converter design. With components switching at greater than 200kHz, the resulting current transitions from one device to another induce voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, lead to device over-voltage stress, radiate noise into sensitive nodes, and increase thermal stress on critical components. Careful component placement and PCB layout minimizes the voltage spikes in the converter.

The following multi-layer printed circuit board layout strategies minimize the impact of board parasitics on converter performance and optimize the heat-dissipating capabilities of the printed-circuit board. This section highlights some important practices which should not be overlooked during the layout process.

Component Placement

Determine the total implementation area and orient the critical switching components first. Symmetry is very important in multiphase converter placement and the switching components dictate how the available space is filled. The switching components carry large amounts of energy and tend to generate high levels of noise. Addressing these issues during component placement allows for reduction of potential switching noise magnitude and radiation into critical nodes. Each power channel of the multiphase converter is made up of an output inductor, upper and lower MOSFETs, and ISL6207 driver. Orient the MOSFETs and inductor first to set the dimension of the resulting PHASE plane. Keeping the components in tight proximity will help reduce parasitic impedances once the components are routed together. Figure 48 illustrates the placement and connection of critical components for one power channel of a converter. Place the ISL6207 driver in close proximity to the PHASE plane and the gates of the MOSFETs. Keep enough open space available around the driver for placement of the BOOT capacitor, C_{BOOT} and bypass capacitor. Duplicate the resulting power channel placement as required in the given implementation area.

In Figure 48, C_{IN} and C_{OUT} represent numerous physical capacitors. Position one high-frequency ceramic input capacitor next to each upper MOSFET drain. Align the body of the capacitor such that the ground connection is coincident with the source of the lower MOSFET. Place the bulk input capacitors as close to the upper MOSFET drain(s) as dictated by the component size and dimensions. Long distances between input capacitors and MOSFETs drains results in too much trace inductance and a reduction in capacitor performance. Locate the output capacitors between the inductors and the load, while keeping them in close proximity around the microprocessor socket. Care should be taken not to add inductance in the circuit board traces that could cancel the usefulness of the low inductance components.

The ISL6247 can be placed off to one side or centered relative to the individual channel switching components. Routing of sense lines and PWM signals will guide final placement. Critical small signal components to place close to the controller include the feedback resistor R_{FB}, frequency select resistor R_{FS}, offset resistor R_{OFS}, over-current select resistor R_{OCSET}, feed-forward ramp adjustment resistors R_{ADJ1} and R_{ADJ2}, and slew rate capacitor C_{SOFT}, Deep and Deeper Sleep voltage divider resistors, and compensation components R_C and C_C. Because the remote sense traces for VSEN and VRTN may be long and routed close to switching nodes, a 1.0µF ceramic decoupling capacitor can be located between VSEN and RTN pins of the package.

The DCR sensing components, R and C, must be placed in parallel with the inductor. Place the PTC R_{ISEN} resistor just off the inductor pads to allow it to track the inductor temperature properly. The further away the PTC is placed from the inductor, the weaker the temperature correlation between the inductor and PTC.

Place the NTC thermistor, R_{NTC}, near a critical switching component which dissipates heat into the board. The standard 1% resistor, R, in the NTC network should be placed close to the ISL6247.

Bypass capacitors, C_{BP}, supply critical bypassing current for the ISL6247 and ISL6207 drivers bias supplies and must be placed next to their respective pins. Stray trace parasitics will reduce their effectiveness, so keep the distance between the VCC bias supply pad and capacitor pad to a minimum.

Plane Allocation

PCB designers typically have a set number of planes available for a converter design. Dedicate one solid layer, usually an internal layer if available, for a ground plane. The ground plane should be split into two separate planes connected together at one point. The main power ground plane which supports the high-currents demanded by the load and a noise sensitive analog ground plane. Connecting the two planes at one point minimizes the noise injection from the high-frequency current components in the power ground plane into the sensitive circuits grounded to the analog ground plane, or sometimes referred to as the signal ground plane.

Another common practice is the star ground in which all sensitive components connect together at one point and then to the power ground. This approach has the same effect as separating the power- and analog-ground planes, but is not always practical depending on the board complexity.

One additional solid layer is dedicated as a power plane and broken into smaller islands of common voltage. The remaining PCB layers are used for small signal routing and additional power or ground islands as required.

Signal Routing

If the power channel component placement guidelines are followed, stray inductance in the switch current path created by the copper filled PHASE plane is minimized. Stray inductance in these high-current paths induce large noise voltages that couple into sensitive circuitry. By keeping the PHASE plane small, the magnitude of the potential spikes is minimized. Duplicate the power channel component placement and layout for each phase.

The ISL6207 gate trace impedance must be kept low to reduce switching loss, lower switching component and board temperature, and lower output voltage ripple. Routing the driver and MOSFETs on the same layer with short, wide traces helps reduce both parasitic resistance and inductance. Size the driver gate traces to carry at least 4A of current, recommended trace width is 4mm.

Sensitive signals should be routed on different layers or some distance away from the PHASE planes on the same layer. Crosstalk due to switching noise is reduced into these lines by isolating the routing path away from the PHASE planes. Layout the PHASE planes on one layer, usually the top or bottom layer, and route the ISEN, VSEN, VRTN, and NTC traces on another layer remaining.

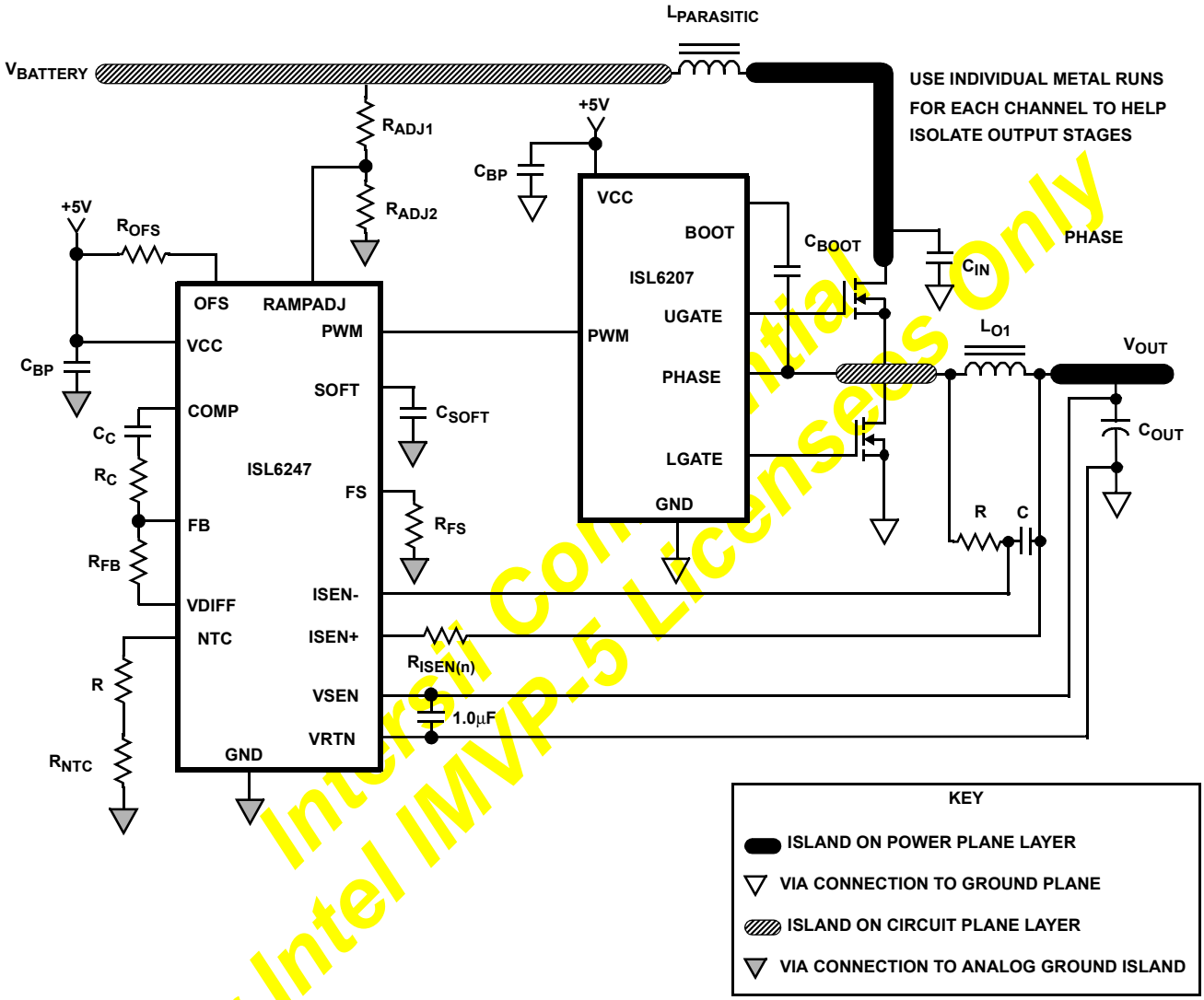
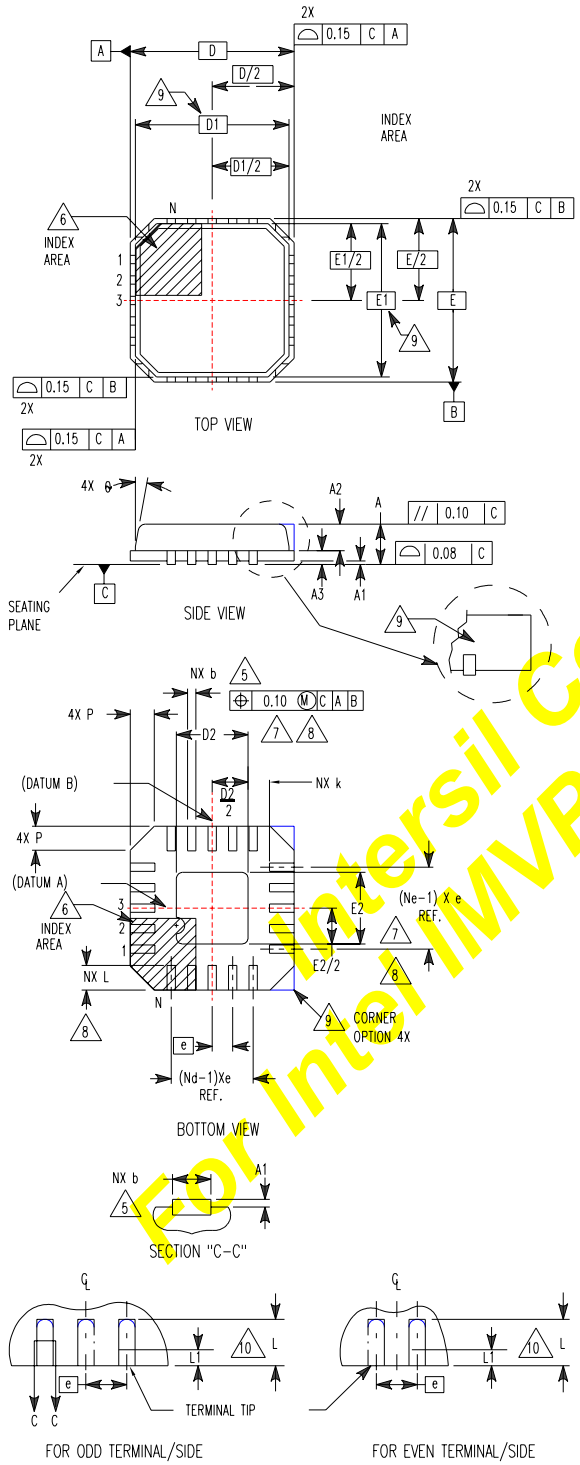


FIGURE 48. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Quad Flat No-Lead Plastic Package (QFN)



L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VJJD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		6.00 BSC		-
D1		5.75 BSC		9
D2	3.95	4.10	4.25	7, 8
E		6.00 BSC		-
E1		5.75 BSC		9
E2	3.95	4.10	4.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		40		2
Nd		10		3
Ne		10		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

BSC = basic lead spacing between centers

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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