

# IRF7904UPbF

HEXFET® Power MOSFET

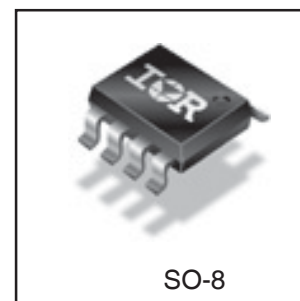
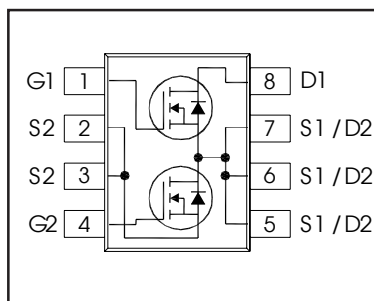
## Applications

- Dual SO-8 MOSFET for POL Converters in Notebook Computers, Servers, Graphics Cards, Game Consoles and Set-Top Box

$V_{DSS}$	$R_{DS(on)}$ max	$I_D$
30V	Q1 16.2m $\Omega$ @ $V_{GS} = 10V$	7.6A
	Q2 10.8m $\Omega$ @ $V_{GS} = 10V$	11A

## Benefits

- Very Low  $R_{DS(on)}$  at 4.5V  $V_{GS}$
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 20V  $V_{GS}$  Max. Gate Rating
- Improved Body Diode Reverse Recovery
- 100% Tested for  $R_G$
- Lead-Free



## Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
$V_{DS}$	Drain-to-Source Voltage	30		V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$		
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7.6	11	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	6.1	8.9	
$I_{DM}$	Pulsed Drain Current ①	61	89	
$P_D @ T_A = 25^\circ C$	Power Dissipation	1.4	2.0	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	0.9	1.3	
	Linear Derating Factor	0.011	0.016	W/ $^\circ C$
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150		$^\circ C$

## Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	20	20	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient ④ ⑤	90	62.5	

# IRF7904UPbF


Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA		
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	Q1	—	0.024	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA		
		Q2	—	0.024	—				
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	Q1	—	11.4	16.2	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 7.6A ③		
			—	14.5	20.5		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.1A ③		
		Q2	—	8.6	10.8		V <sub>GS</sub> = 10V, I <sub>D</sub> = 11A ③		
			—	10	13		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 8.8A ③		
V <sub>GS(th)</sub>	Gate Threshold Voltage	Q1&Q2	1.35	—	2.25	V	Q1: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 25μA Q2: V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50μA		
ΔV <sub>GS(th)</sub> /ΔT <sub>J</sub>	Gate Threshold Voltage Coefficient	Q1	—	-5.0	—	mV/°C			
		Q2	—	-5.0	—				
I <sub>DSS</sub>	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V		
		Q1&Q2	—	—	150		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C		
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V <sub>GS</sub> = 20V		
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V <sub>GS</sub> = -20V		
g <sub>fs</sub>	Forward Transconductance	Q1	17	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 6.1A		
		Q2	23	—	—		V <sub>DS</sub> = 15V, I <sub>D</sub> = 8.8A		
Q <sub>g</sub>	Total Gate Charge	Q1	—	7.5	11	nC	Q1 V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 6.1A  Q2 V <sub>DS</sub> = 15V V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 8.8A		
		Q2	—	14	21				
Q <sub>gs1</sub>	Pre-V <sub>th</sub> Gate-to-Source Charge	Q1	—	2.2	—				
		Q2	—	3.7	—				
Q <sub>gs2</sub>	Post-V <sub>th</sub> Gate-to-Source Charge	Q1	—	0.6	—				
		Q2	—	1.1	—				
Q <sub>gd</sub>	Gate-to-Drain Charge	Q1	—	2.5	—				
		Q2	—	4.8	—				
Q <sub>qodr</sub>	Gate Charge Overdrive	Q1	—	2.2	—				
		Q2	—	4.4	—				
Q <sub>sw</sub>	Switch Charge (Q <sub>gs2</sub> + Q <sub>gd</sub> )	Q1	—	3.1	—				
		Q2	—	5.9	—				
Q <sub>oss</sub>	Output Charge	Q1	—	4.5	—	nC	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V		
		Q2	—	9.1	—				
R <sub>G</sub>	Gate Resistance	Q1	—	3.2	4.8	Ω			
		Q2	—	2.9	4.4				
t <sub>d(on)</sub>	Turn-On Delay Time	Q1	—	6.9	—	ns	Q1 V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 6.1A  Q2 V <sub>DD</sub> = 15V, V <sub>GS</sub> = 4.5V I <sub>D</sub> = 8.8A Clamped Inductive Load		
		Q2	—	7.8	—				
t <sub>r</sub>	Rise Time	Q1	—	7.3	—				
		Q2	—	10	—				
t <sub>d(off)</sub>	Turn-Off Delay Time	Q1	—	10	—				
		Q2	—	15	—				
t <sub>f</sub>	Fall Time	Q1	—	3.2	—				
		Q2	—	4.6	—				
C <sub>iss</sub>	Input Capacitance	Q1	—	910	—			pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 15V f = 1.0MHz
		Q2	—	1780	—				
C <sub>oss</sub>	Output Capacitance	Q1	—	190	—				
		Q2	—	390	—				
C <sub>rss</sub>	Reverse Transfer Capacitance	Q1	—	94	—				
		Q2	—	180	—				

## Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	140	250	mJ
I <sub>AR</sub>	Avalanche Current ①	—	6.1	8.8	A

## Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	Q1	—	—	1.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		Q2	—	—	2.5		
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	Q1	—	—	61	A	
		Q2	—	—	88		
V <sub>SD</sub>	Diode Forward Voltage	Q1	—	—	1.0	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 6.1A, V <sub>GS</sub> = 0V ③
		Q2	—	—	1.0		T <sub>J</sub> = 25°C, I <sub>S</sub> = 8.8A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	Q1	—	11	17	ns	Q1 T <sub>J</sub> = 25°C, I <sub>F</sub> = 6.1A, V <sub>DD</sub> = 15V, di/dt = 100A/μs ③
		Q2	—	16	24		
Q <sub>rr</sub>	Reverse Recovery Charge	Q1	—	2.6	3.9	nC	Q2 T <sub>J</sub> = 25°C, I <sub>F</sub> = 8.8A, V <sub>DD</sub> = 15V, di/dt = 100A/μs ③
		Q2	—	6.9	10		

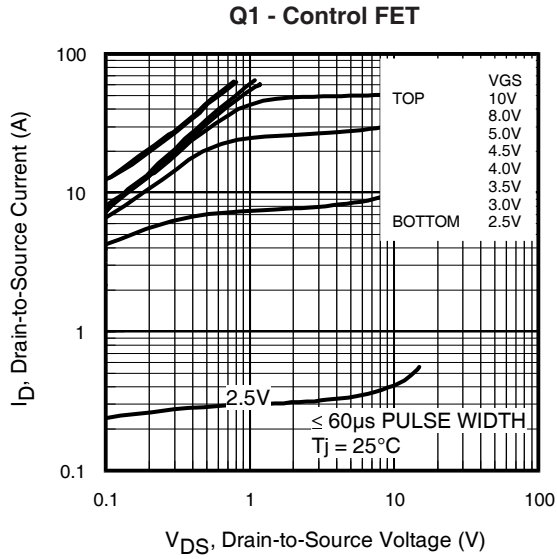


Fig 1. Typical Output Characteristics

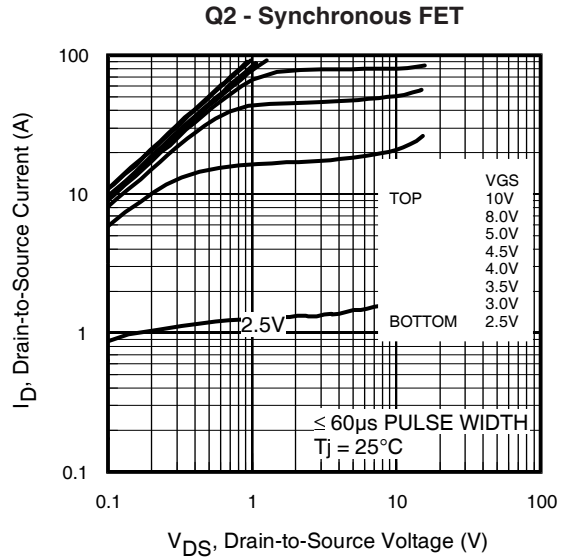


Fig 2. Typical Output Characteristics

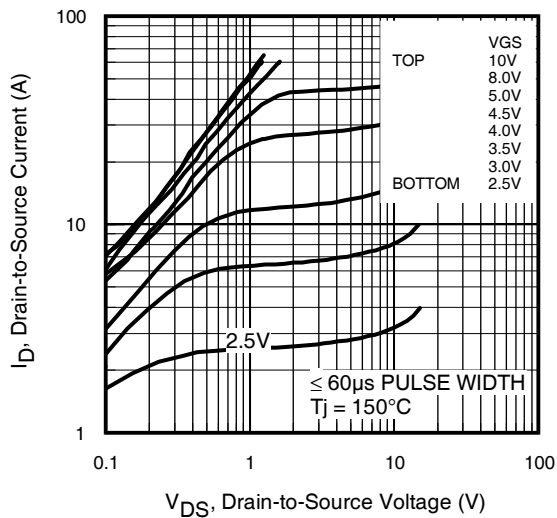


Fig 3. Typical Output Characteristics

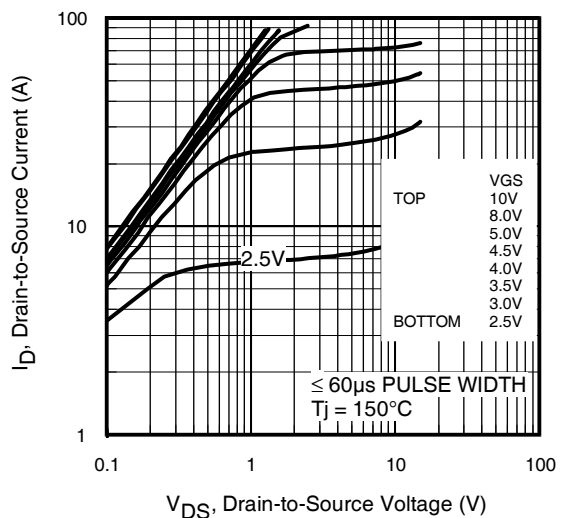


Fig 4. Typical Output Characteristics

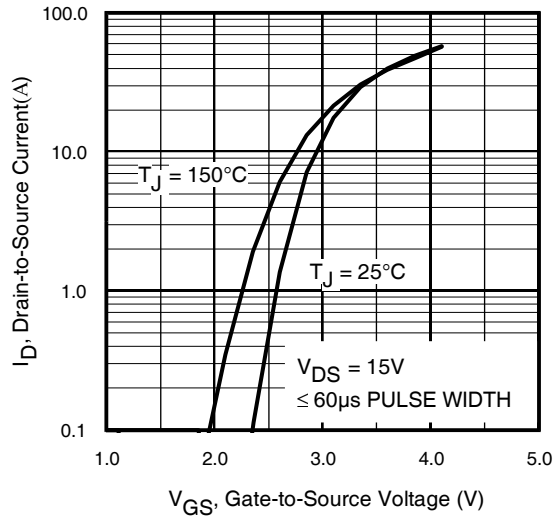


Fig 5. Typical Transfer Characteristics

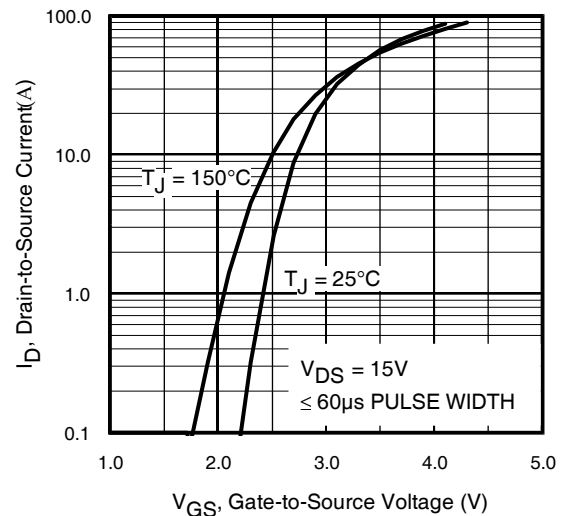
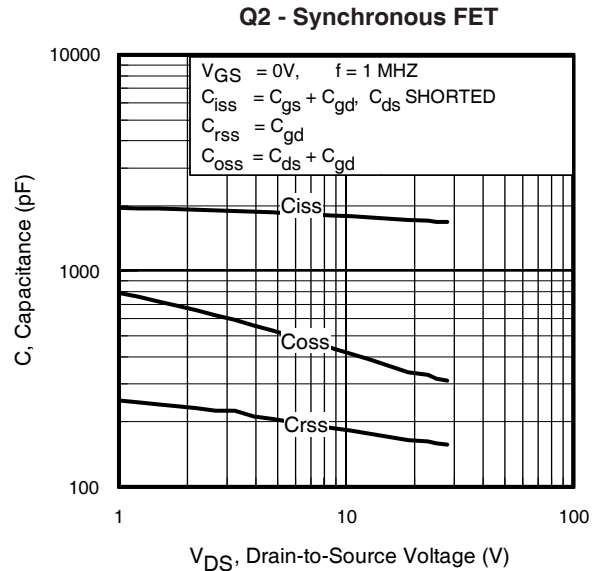
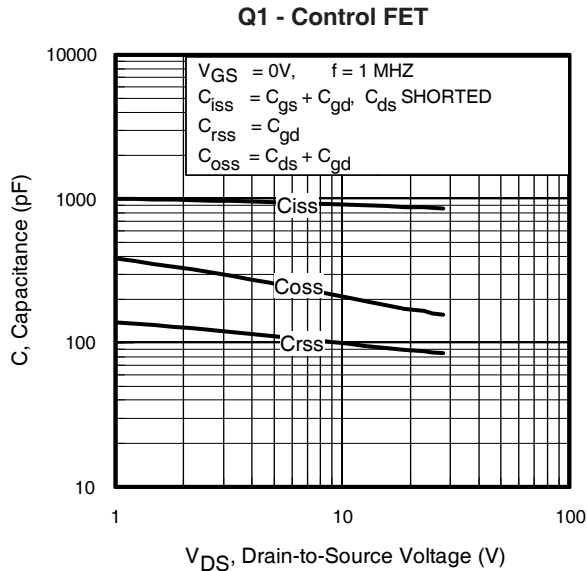
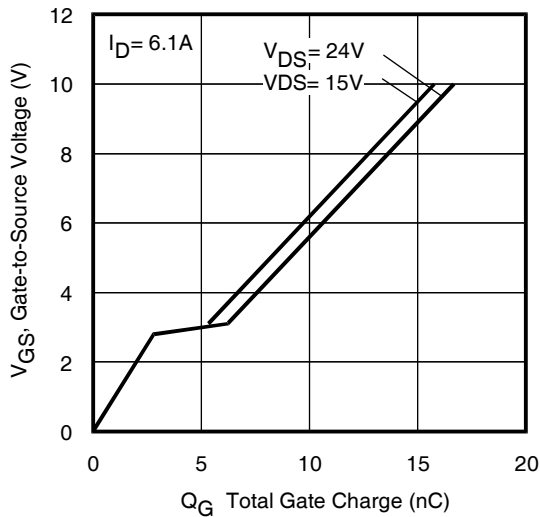


Fig 6. Typical Transfer Characteristics

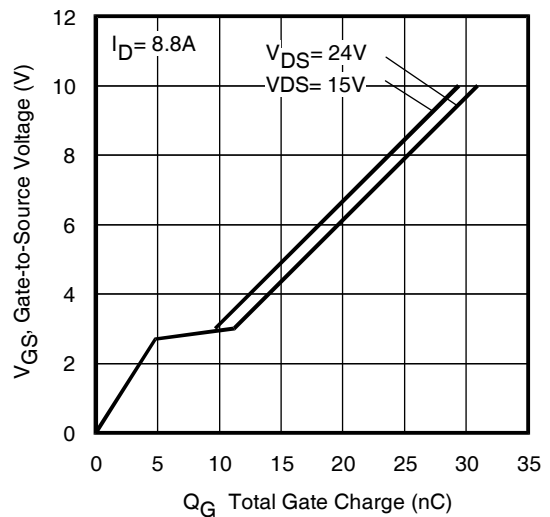


**Fig 7.** Typical Capacitance vs. Drain-to-Source Voltage

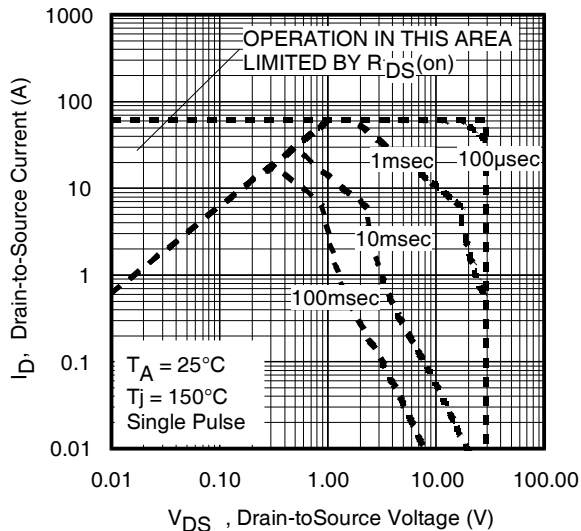
**Fig 8.** Typical Capacitance vs. Drain-to-Source Voltage



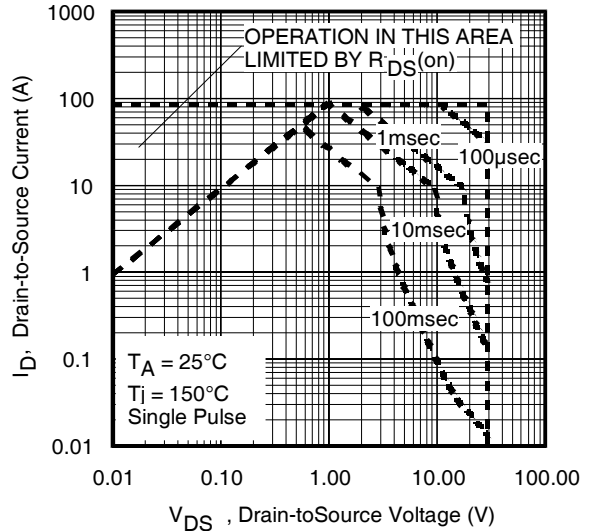
**Fig 9.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 10.** Typical Gate Charge vs. Gate-to-Source Voltage



**Fig 11.** Maximum Safe Operating Area



**Fig 12.** Maximum Safe Operating Area

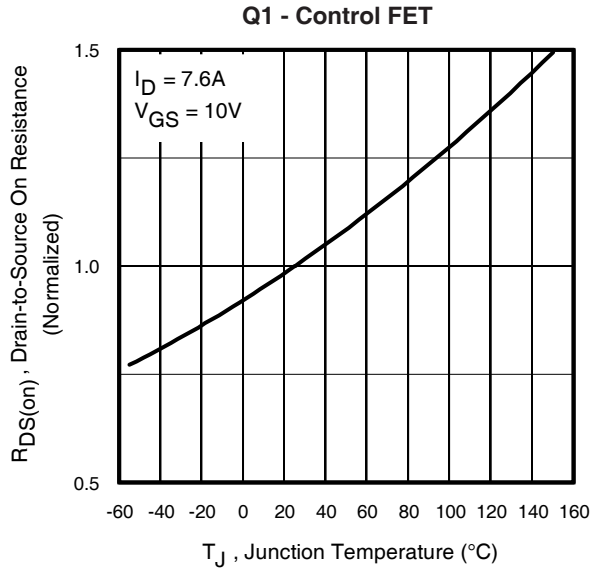


Fig 13. Normalized On-Resistance vs. Temperature

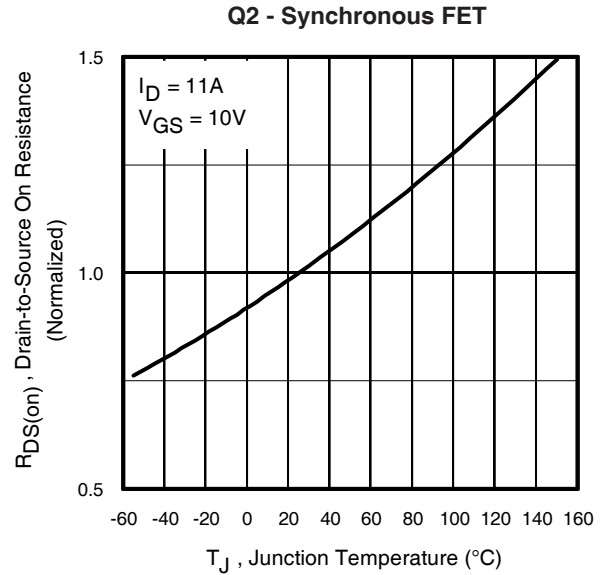


Fig 14. Normalized On-Resistance vs. Temperature

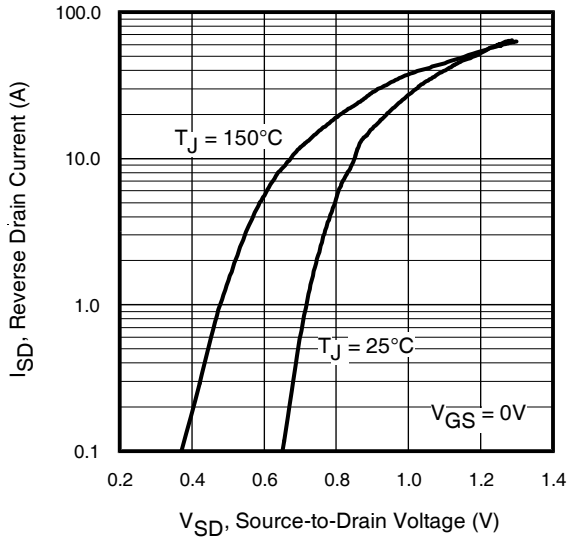


Fig 15. Typical Source-Drain Diode Forward Voltage

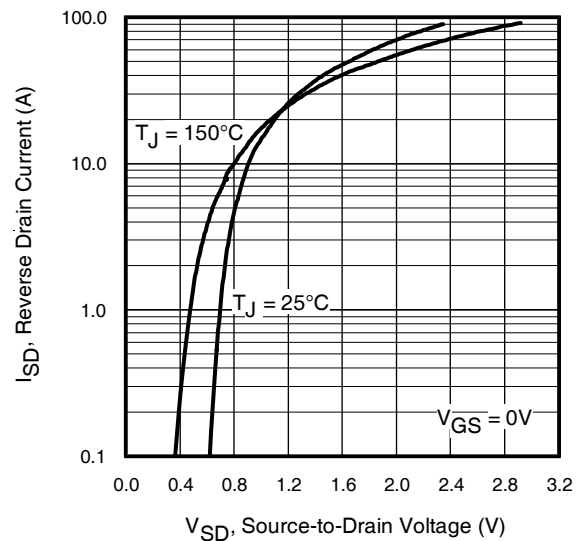


Fig 16. Typical Source-Drain Diode Forward Voltage

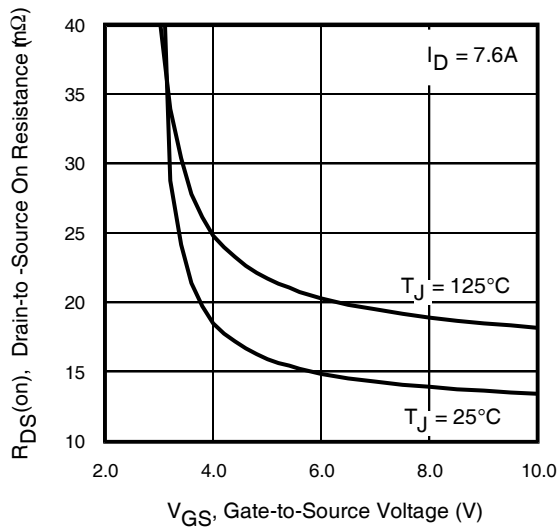


Fig 17. Typical On-Resistance vs. Gate Voltage

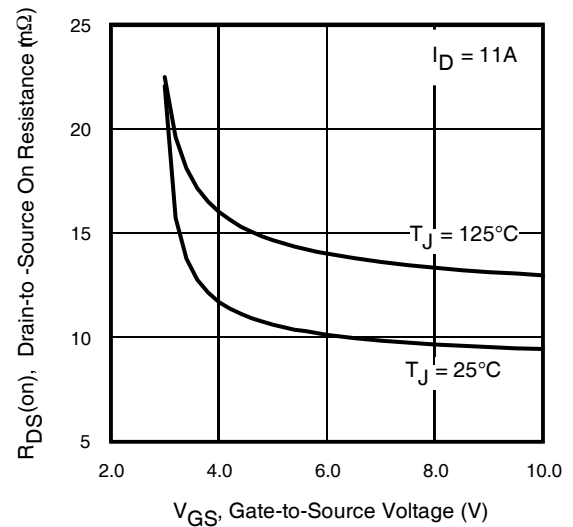
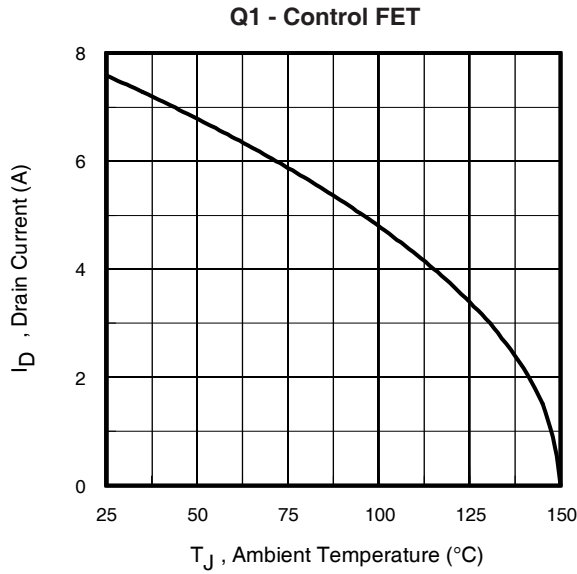
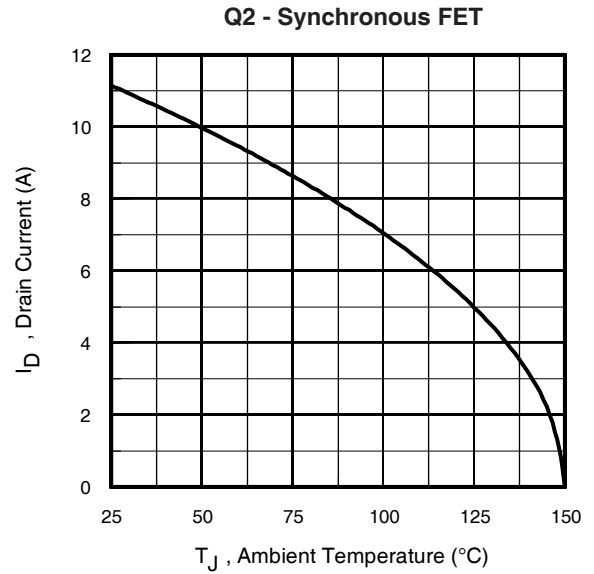


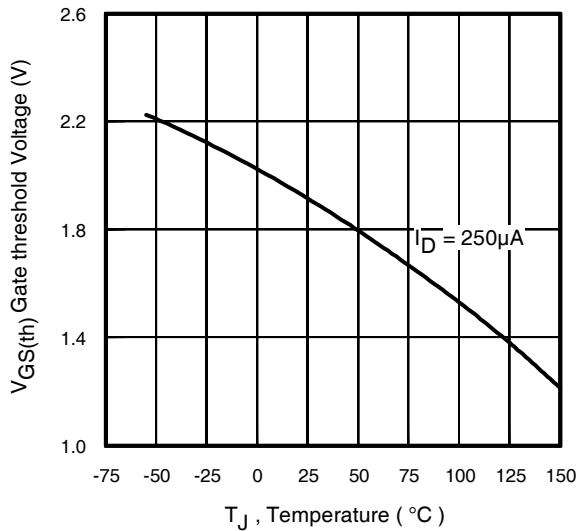
Fig 18. Typical On-Resistance vs. Gate Voltage



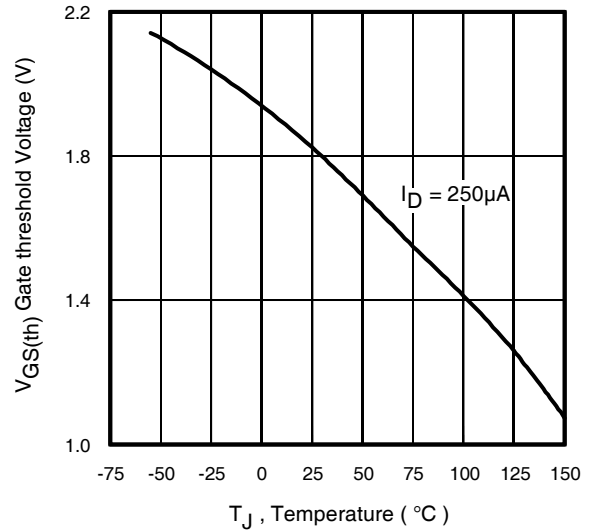
**Fig 19.** Maximum Drain Current vs. Ambient Temp.



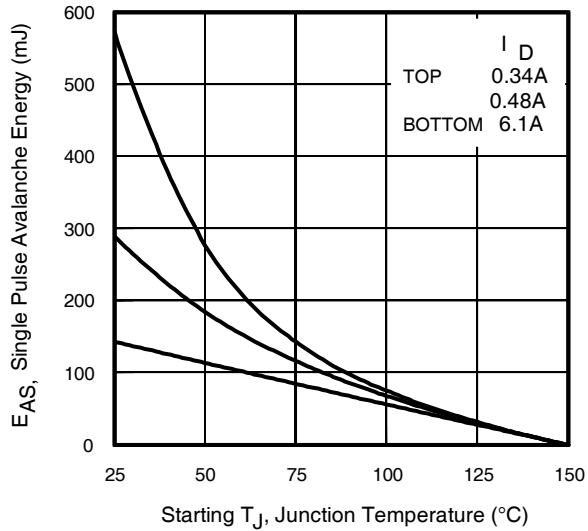
**Fig 20.** Maximum Drain Current vs. Ambient Temp.



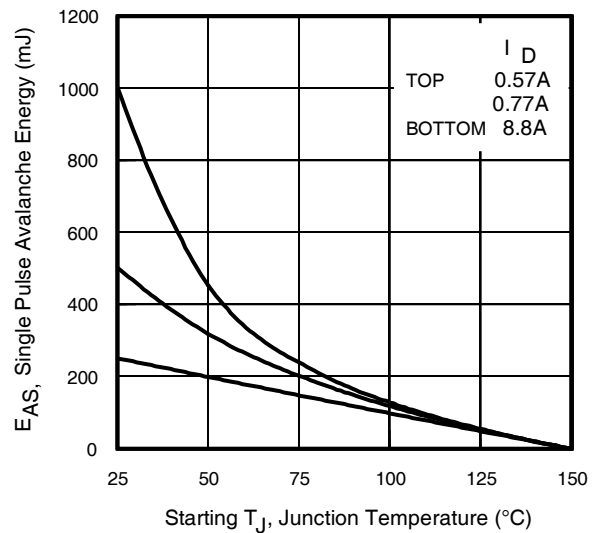
**Fig 21.** Threshold Voltage vs. Temperature



**Fig 22.** Threshold Voltage vs. Temperature



**Fig 23.** Maximum Avalanche Energy vs. Drain Current



**Fig 24.** Maximum Avalanche Energy vs. Drain Current

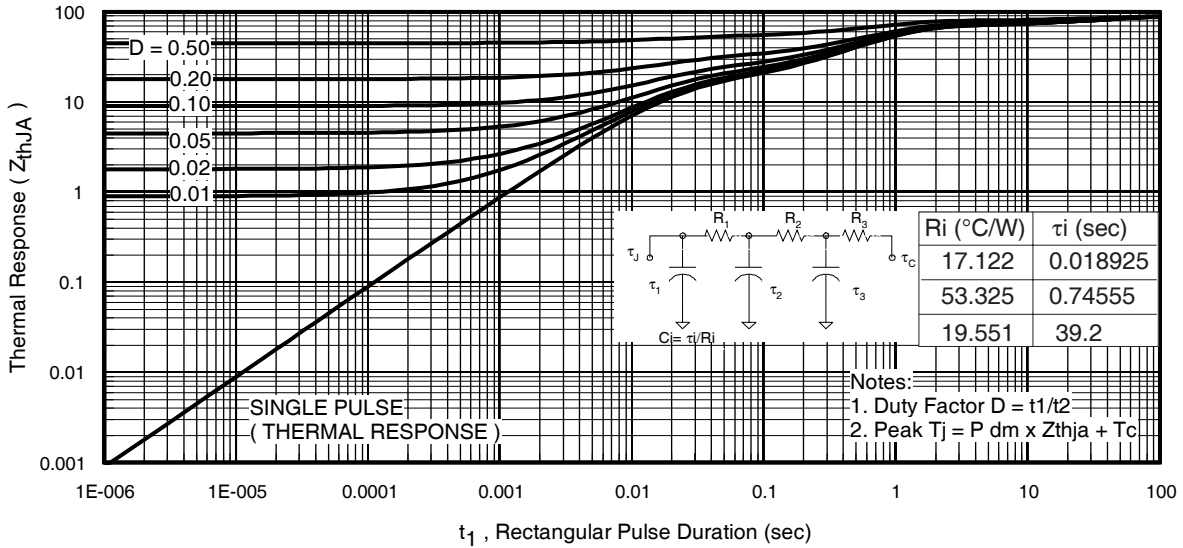


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

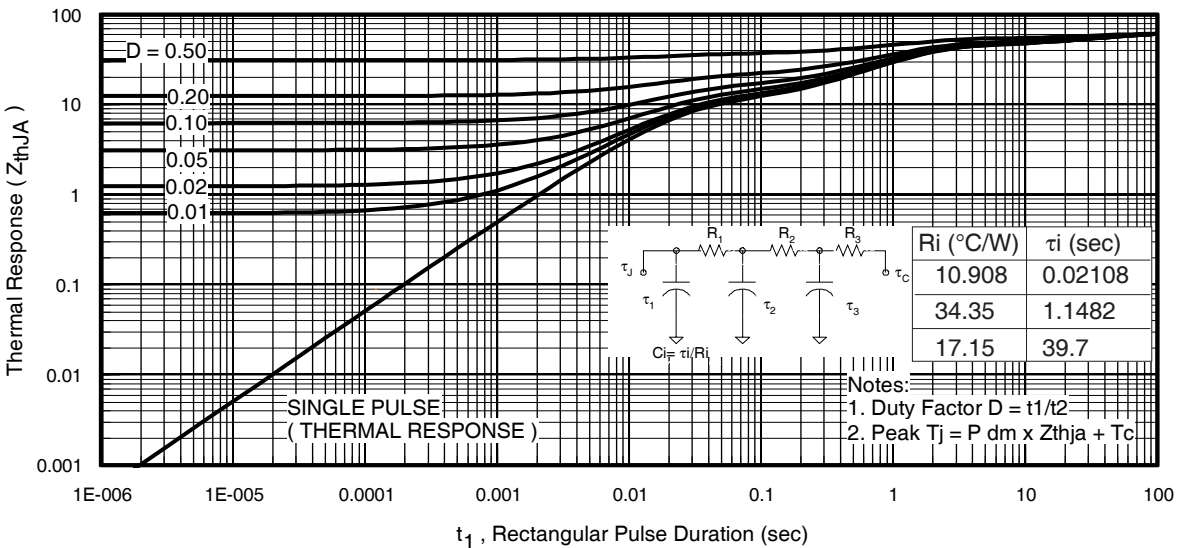


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

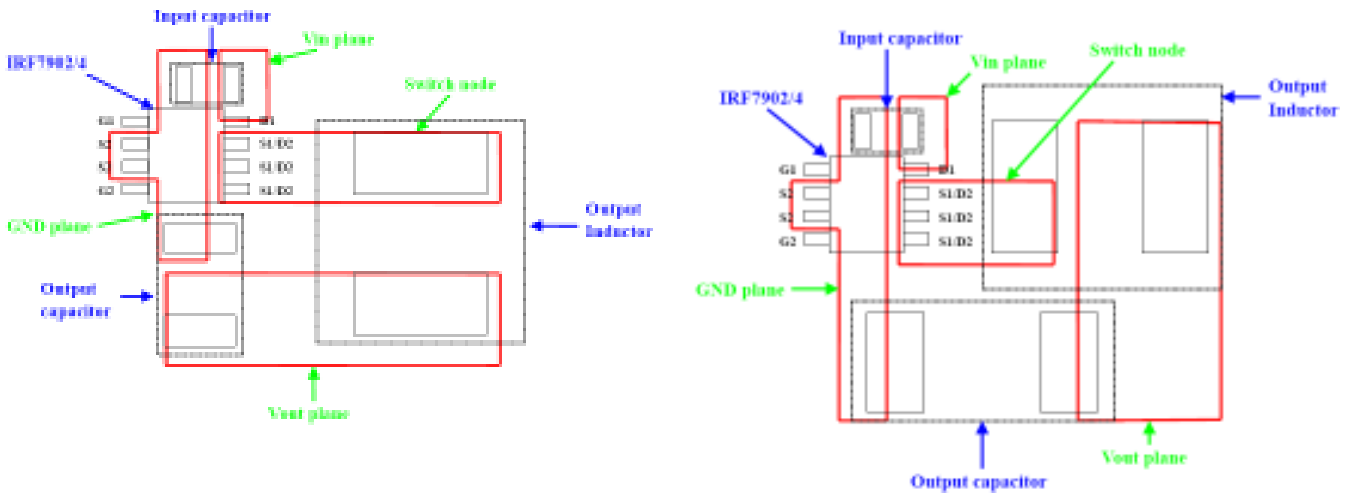
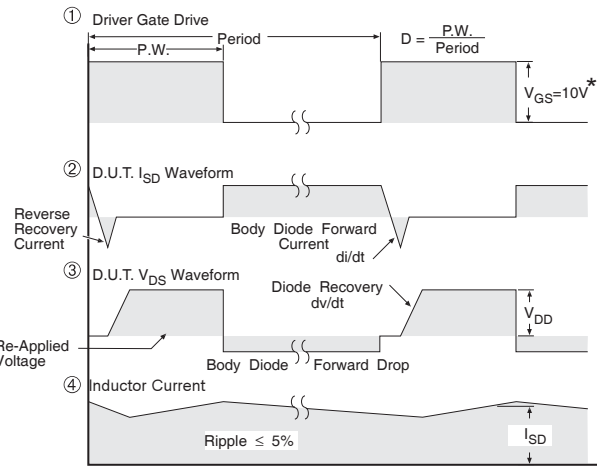
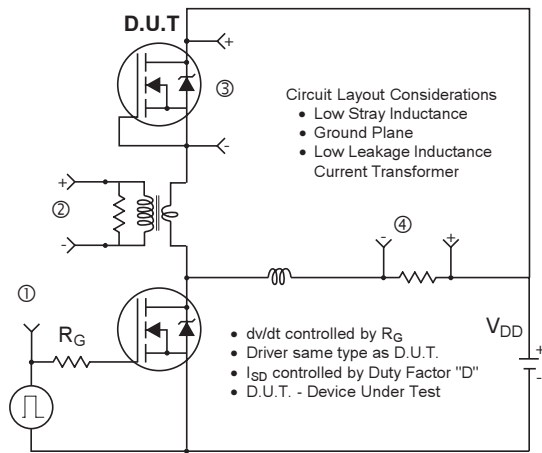
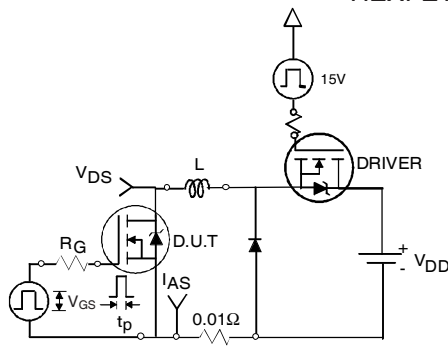


Fig 27. Layout Diagram

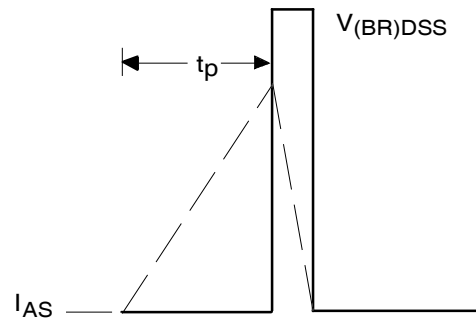


\*  $V_{GS} = 5V$  for Logic Level Devices

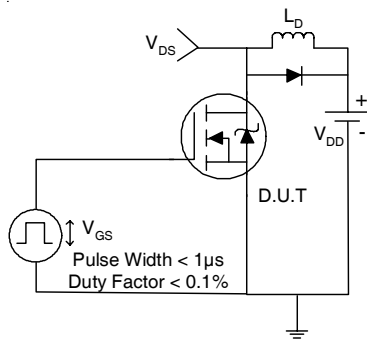
**Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



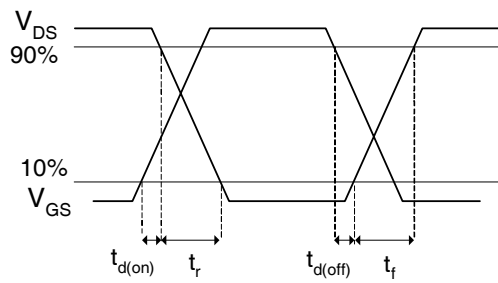
**Fig 29a. Unclamped Inductive Test Circuit**



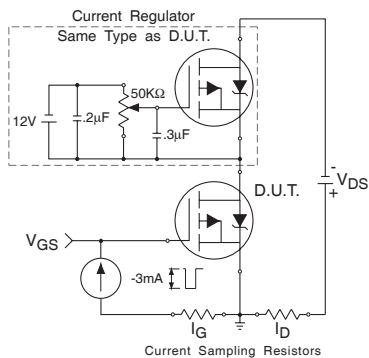
**Fig 29b. Unclamped Inductive Waveforms**



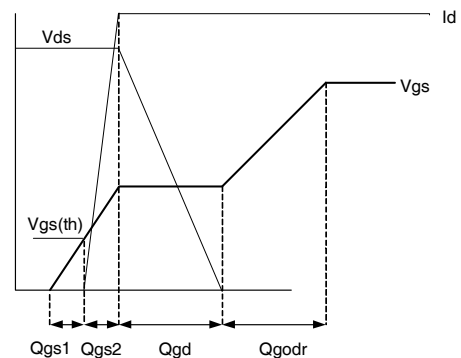
**Fig 30a. Switching Time Test Circuit**



**Fig 30b. Switching Time Waveforms**



**Fig 31a. Gate Charge Test Circuit**

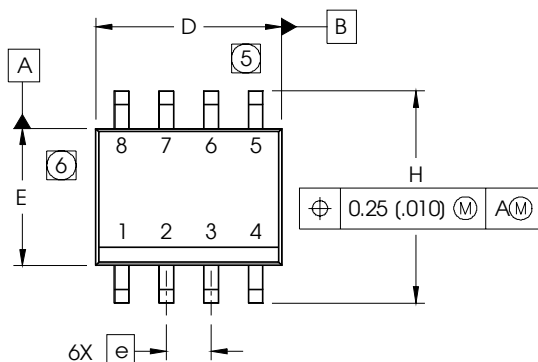


**Fig 31b. Gate Charge Waveform**

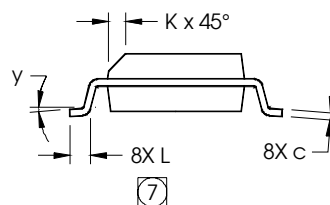
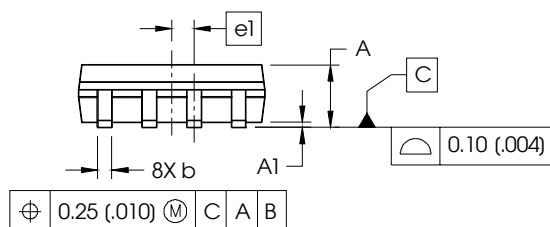


## SO-8 Package Outline

Dimensions are shown in millimeters (inches)



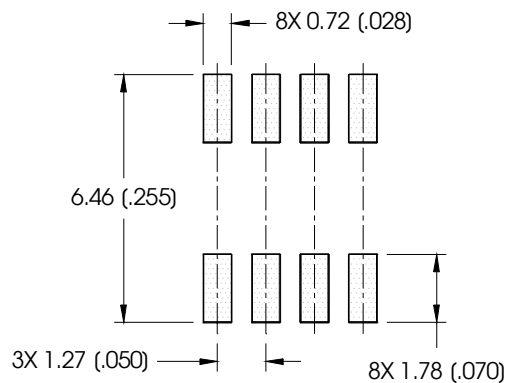
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

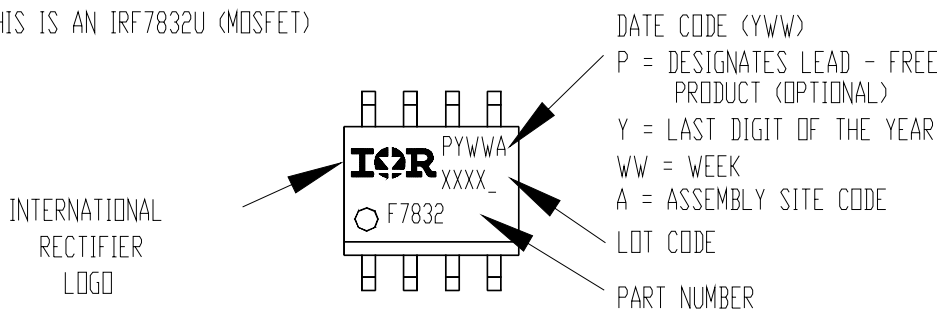
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



## SO-8 Part Marking

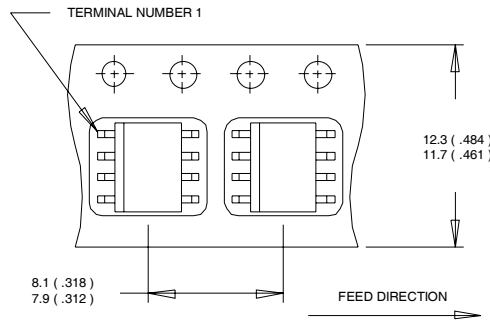
EXAMPLE: THIS IS AN IRF7832U (MOSFET)



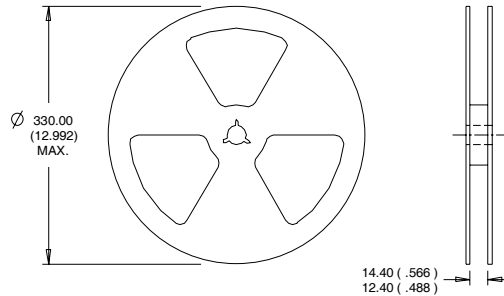
# IRF7904UPbF

## SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
  2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ , Q1:  $L = 7.7\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 6.1\text{A}$ ; Q2:  $L = 6.5\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 8.8\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ When mounted on 1 inch square copper board.
- ⑤  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Consumer market.  
 Qualification Standards can be found on IR's Web site.