512M (16Mx32) GDDR3 SDRAM

HY5RS123235FP

Revision History

Revision No.	History	Draft Date	Remark
0.1	Defined target spec.	Mar. 2004	
0.2	Page 11) Add Cas Latency 11 Page 14) Write Latency definitions Page15) DI, WR_A, AL definitions Page47) Table18 typo corrected Page48) Table19 renewered Page50) note 46 added	JULY.2004	CL WL DI/WR_A/AL Speed BIN Several Parameters tRPRE
0.3	Page4) Ballout configurations correct Appendix C) BST function description	Aug.2004	A3/A8/A9/A10
0.4	- Non-Consectutive Read to Write timing clarifications - Read to Precharge timing Clarifications	Sep.24,2004	Page28 page41 Page23
0.5	- Modified the pin descriptions and added command description for BST - Added the LP mode feature for EMRS	Nov.8,2004	Page4,6,21 Page15,16
0.6	-Added the Lead free package part number and Package dimension page	Jan.31,2005	Page3,56
1.0	- Clarified the ODT control and Data terminator disable command and its duration timing - Modify the Data termination disable mode note of EMRS - Modified the PIN description of VDDA/ VSSA(K1,12/J1,12) - Changed the tPDIX, from 4tCK to 6tCK - Changed the tXSRD, from 300tCk to 1000tCK - Added the tCJC definition - IDD spec update - DC spec Update	Apr.30,2005	Page 15,20 Page 9 Page 4,7 Page 47 Page 48 page 48 page 46 Table 12
1.1	VDD/VDDQ change, 500Mhz Speed Bin Insert, IDD value tuning & typo corrected	Jun. 2005	
1.2	VDD/VDDQ Change at 600MHz speed bin to 1.8V from 2.0V	Nov. 2005	
1.3	900MHz speed bin insert	Feb. 2006	
1.4	VDD/VDDQ change for 800MHz speed bin & IDD value change	Mar. 2006	
1.5	Changed Async parameter at 700/800/900MHz speed bin (tRAS/tRC/tRFC/tRCDW/tRP/tDAL)	Apr. 2006	

DESCRIPTION

The Hynix HY5RS123235 is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits.

The Hynix HY5RS123235 is internally configured as a eight-bank DRAM.

The Hynix HY5RS123235 uses a double data rate architecture to achieve high-speed opreration. The double date rate architecture is essentially a 4n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the Hynix HY5RS123235 consists of a 4n-bit wide, every two-clock-cycles data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the Hynix HY5RS123235 is burst oriented; accesses start at a selected locations and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ of WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0,BA1, BA2 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access. Prior to normal operation, the Hynix HY5RS123235 must be initialized.

FEATURES

- 2.2V +/-0.1V VDD/VDDQ power supply supports 900 / 800MHz
- 2.0V VDD/ VDDQ wide range min/max power supply supports 700MHz
- 1.8V VDD/ VDDQ wide range min/max power supply supports 500 / 600MHz
- Single ended READ Strobe (RDQS) per byte
- Single ended WRITE Strobe (WDQS) per byte
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Calibrated output driver
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- RDQS edge-aligned with data for READ; with WDQS center-aligned with data for WRITE
- Eight internal banks for concurrent operation
- Data mask (DM) for masking WRITE data
- 4n prefetch
- Programmable burst lengths: 4, 8
- 32ms, 8K-cycle auto refresh
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 1.8V Pseudo Open Drain I/O
- Concurrent Auto Precharge support
- tRAS lockout support, Active Termination support
- Programmable Write latency(1, 2, 3, 4, 5, 6)
- Boundary Scan Feature for connectivity test(refer to JEDEC std., not in this version of Specifications)

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
HY5RS123235FP-11	VDD=2.2V, VDDQ=2.2V	900MHz	1800Mbps/pin	POD_18	12mmx14mm 136Ball FBGA
HY5RS123235FP-12		800MHz	1600Mbps/pin		
HY5RS123235FP-14	VDD=2.0V, VDDQ=2.0V	700MHz	1400Mbps/pin		
HY5RS123235FP-16	VDD=1.8V, VDDQ=1.8V	600MHz	1200Mbps/pin		
HY5RS123235FP-2		500MHz	1000Mbps/pin		

Note) HY5RS123235FP-xx is the Lead Free Package part number

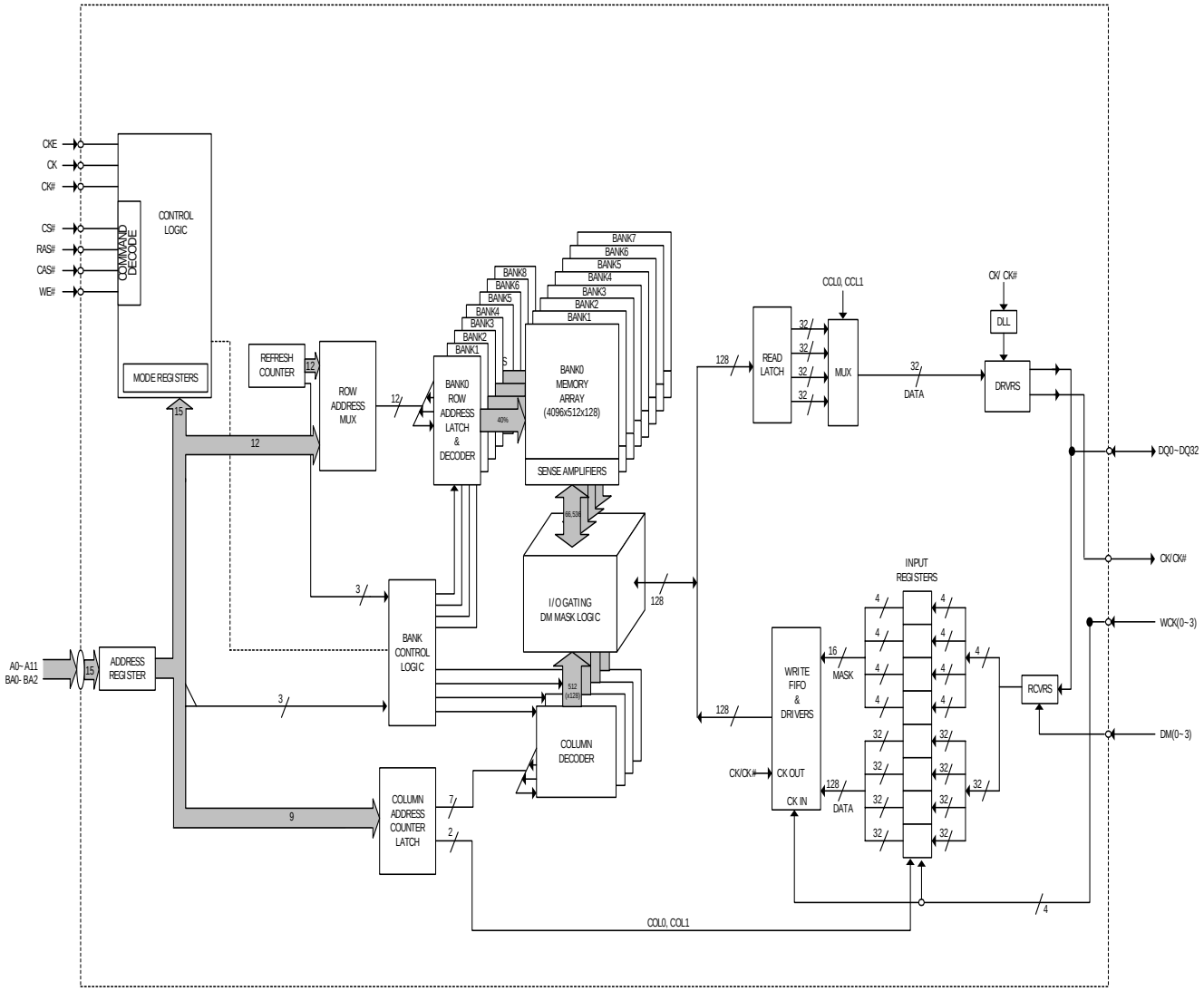
BALLOUT CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12
A	VDDQ	VDD	VSS	ZQ					MF	VSS	VDD	VDDQ
B	VSSQ	DQ0	DQ1	VSSQ					VSSQ	DQ9	DQ8	VSSQ
C	VDDQ	DQ2	DQ3	VDDQ					VDDQ	DQ11	DQ10	VDDQ
D	VSSQ	WDQS0	RDQS0	VSSQ					VSSQ	RDQS1	WDQS1	VSSQ
E	VDDQ	DQ4	DM0	VDDQ					VDDQ	DM1	DQ12	VDDQ
F	VDD	DQ6	DQ5	CAS#					CS#	DQ13	DQ14	VDD
G	VSS	VSSQ	DQ7	BA0					BA1	DQ15	VSSQ	VSS
H	VREF	A1	RAS#	CKE					WE#	BA2	A5	VREF
J	VSS	NC	RFU	VDDQ					VDDQ	CK#	CK	VSS
K	VDD	A10	A2	A0					A4	A6	A8/AP	VDD
L	VSS	VSSQ	DQ25	A11					A7	DQ17	VSSQ	VSS
M	VDD	DQ24	DQ27	A3					A9	DQ19	DQ16	VDD
N	VDDQ	DQ26	DM3	VDDQ					VDDQ	DM2	DQ18	VDDQ
P	VSSQ	WDQS3	RDQS3	VSSQ					VSSQ	RDQS2	WDQS2	VSSQ
R	VDDQ	DQ28	DQ29	VDDQ					VDDQ	DQ21	DQ20	VDDQ
T	VSSQ	DQ30	DQ31	VSSQ					VSSQ	DQ23	DQ22	VSSQ
U	VDDQ	VDD	VSS	SEN					RES	VSS	VDD	VDDQ

	16M x 32
Configuration	2M x 32 x 8 banks
Refresh Count	8 k
Bank Address	BA0 - BA2
Row Address	A0~A11
Column Address	A0~A7, A9
AP Flag	A8

FUNCTIONAL BLOCK DIAGRAM

8Banks x 2Mbit x 32 I/O Double Data Rate Synchronous DRAM



BALLOUT DESCRIPTIONS

FBGA BALLOUT	SYMBOL	TYPE	DESCRIPTION
J10, J11	CK, CK#	Input	Clock: CK and Ck# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
H4	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations(all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH.
F9	CS#	Input	Chip Select: CS# enables (registered LOW)and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
H3, F4, H9	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE#(along with CS#) define the command being entered.
E(3, 10), N(3, 10)	DM0-DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on rising and falling edges of WDQS.
G(4, 9), H10	BA0 - BA2	Input	Bank Address Inputs: BA0 and BA2 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
H(2, 11), K(2-4, 9-11), L(4, 9), M(4, 9)	A0-A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit(A8) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0 - BA2) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
B(2, 3), C(2, 3), E2, F(2, 3), G3,B(10, 11), C(10, 11), E11, F(11, 19), G10, L10, M(10, 11), N11, R(10, 11), T(10,11), L3, M(2, 3), N2,R(2, 3), T(2, 3)	DQ0-31	I/O	Data Input/Output:
D(3, 10), P(3, 10)	RDQS0-3	Output	READ Data Strobe: Output with read data. RDQS is edge-aligned with read data.
D(2, 11), P(2, 11)	WDQS0-3	Input	WRITE Data strobe: Input with write data. WDQS is center aligned to the input data.
U4	SEN	Input	Scan Enable Pin. Logic High would enable Scan Mode. Should be tied to GND when not in use. This pin is a CMOS input.
J(2, 3)	NC/RFU		No Connect

BALLOUT DESCRIPTIONS

-CONTINUE

FBGA Ball Out	SYMBOL	TYPE	DESCRIPTION
A(1, 12), C(1, 4, 9, 12), J(4, 9), N(1, 4, 9, 12), R(1, 4, 9, 12), U(1, 12)	VDDQ	Supply	DQ Power Supply: +1.8V. Isolated on the die for improved noise immunity.
B(1, 4, 9, 12), D(1, 4, 9, 12), G(2, 11), L(2, 11), P(1, 4, 9, 12), T(1, 4, 9, 12)	VSSQ	Supply	DQ Ground: Isolated on the die for improved noise immunity.
A(2, 11), F(1, 12), M(1, 12), U(2, 11) K(1, 12)	VDD	Supply	Power Supply: +1.8V.
A(3, 10), G(1, 12), L(1, 12), U(3, 10) J(1, 12)	VSS	Supply	Ground
H(1, 12)	VREF	Supply	Reference voltage.
A9	MF	Reference	Mirror Function for clamshell mounting of DRAMs
A4	ZQ	Reference	External Reference Pin for autocalibration. It should be connected to RQ(=240Ω)
U9	RES	Reference	Reset Pin. The RES pin is a VDD CMOS input.

Mirror Function

The GDDR3 SDRAM provides a mirror function(MF) ball to change the physical location of the control lines and all address lines, assisting in routing devices back to back. The MF ball will affect RAS# , CAS# , WE#, CS# and CKE on balls H3, F4, H9, F9 and H4 respectively and A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, BA0, BA1 and BA2 on balls K4, H2, K3, M4, K9, H11, K10, L9, K11, M9, K2, L4, G4, G9 and H10 respectively and only detects a DC input. The MF ball should be tied directly to VSS of VDD depending on the control line orientation desired.

When MF ball is tied low the ball orientation is as follows. RAS# -H3, CAS# -F4, WE# -H9, CS# -F9, CKE-H4, A0-K4, A1-H2, A2-K3, A3-M4, A4-K9, A5-H11, A6-K10, A7-L9, A8-K11, A9-M9, A10-K2, A11-L4, BA0-G4, BA1-G9 and BA2-H10. The high condition on the MF ball will change the location of the control balls as follows; CS# -F4, cas# -F9, ras# -H10, WE# -H4, CKE-H9, A0-K9, A1-H11, A2-K10, A3-M9, A4-K4, A5-H2, A6-K3, A7-L4, A8-K2, A9-M4, A10-K11, A11-L9, BA0-G9, BA1-G4 and BA2-H3. This Mirror Fuction does not work under Boundary Scan Test condition.

Mirror Function Signal Mapping

PIN	MF LOGIC STATE	
	HIGH	LOW
RAS#	H10	H3
CAS#	F9	F4
WE#	H4	H9
CS#	F4	F9
CKE	H9	H4
A0	K9	K4
A1	H11	H2
A2	K10	K3
A3	M9	M4
A4	K4	K9
A5	H2	H11
A6	K3	K10
A7	L4	L9
A8	K2	K11
A9	M4	M9
A10	K11	K2
A11	L9	L4
BA0	G9	G4
BA1	G4	G9
BA2	H3	H10

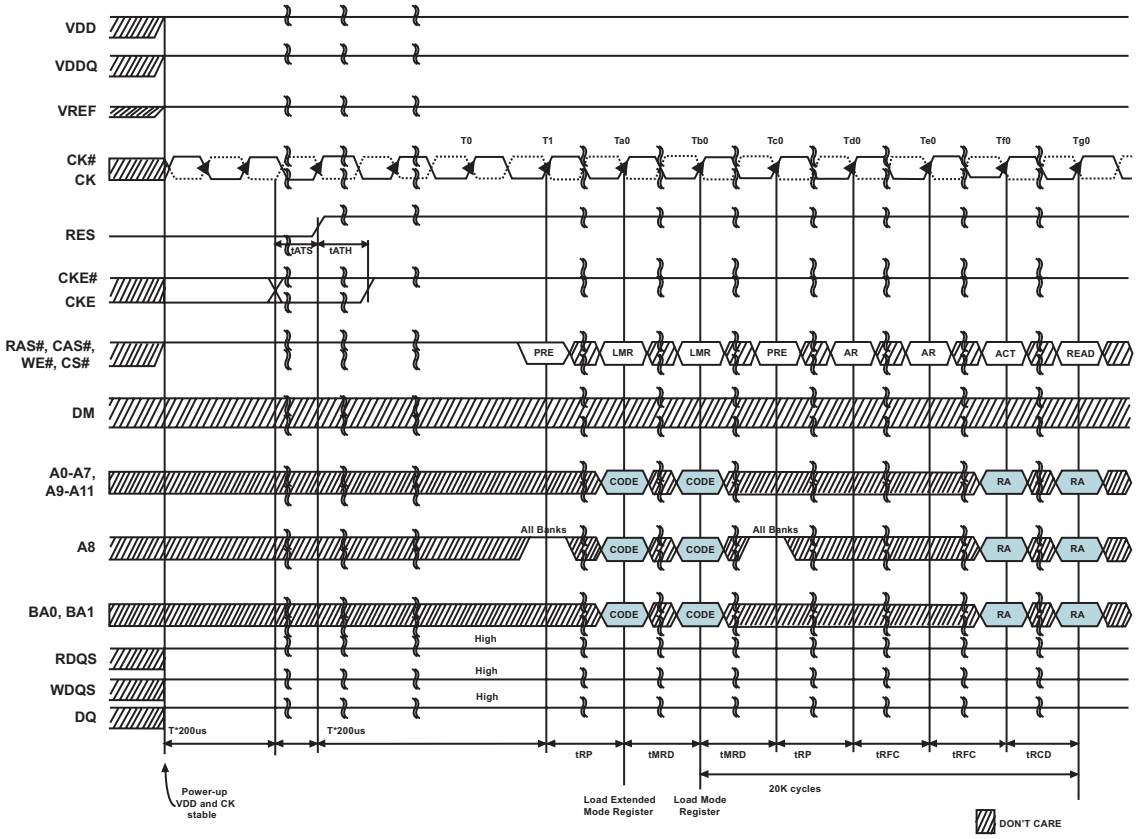
GDDR3 Initialization and Power Up

GDDR3 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must be first applied to VDD and VDDQ simultaneously or VDD first and VDDQ later, and then to VREF. VREF can be applied any time after VDDQ. Once power has been applied and the clocks are stable the GDDR3 device requires 200us before the RES pin transitions to high. Upon power-up and after the clock is stable, the on-die termination value for the address and control pins will be set, based on the state of CKE when the RES pin transitions from LOW to HIGH. On the rising edge of RES, the CKE pin is latched to determine the on die termination value for the address and control lines. If CKE is sampled at a logic LOW then the on die termination will be set to 1/2 of ZQ and, if CKE is sampled logic HIGH then the on die termination will be set to the same value as ZQ. CKE must meet tATS and tATH on the rising of RES to set the on die termination for address and control lines. Once tATH is met, set CKE to HIGH. An additional 200us is required for the address and command on die terminations to calibrate and update.

RES must be maintained at a logic LOW-level value and CS# must be maintained HIGH, during the first stage of power-up to ensure that the DQ outputs will be in a High-Z state(un-terminated).

After the RES pin transitions from LOW to HIGH, wait until a 200us delay is satisfied. Issue DESELECT on the command bus during this time. Issue a PRECHARGE ALL command. Next a LOAD MODE REGISTER command must be issued for the extended mode register (BA1 LOW and BA0 HIGH) to activate the DLL and set operating parameters, followed by the LOAD MODE REGISTER command (BA0/BA1 both LOW) to reset the DLL and to program the rest of the operating parameters. 20k clock cycles are required between the DLL reset and any READ command to allow the DLL to lock. A PRECHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be issued. Following these requirements, the GDDR3 SDRAM is ready for normal operation.



ODT Updating

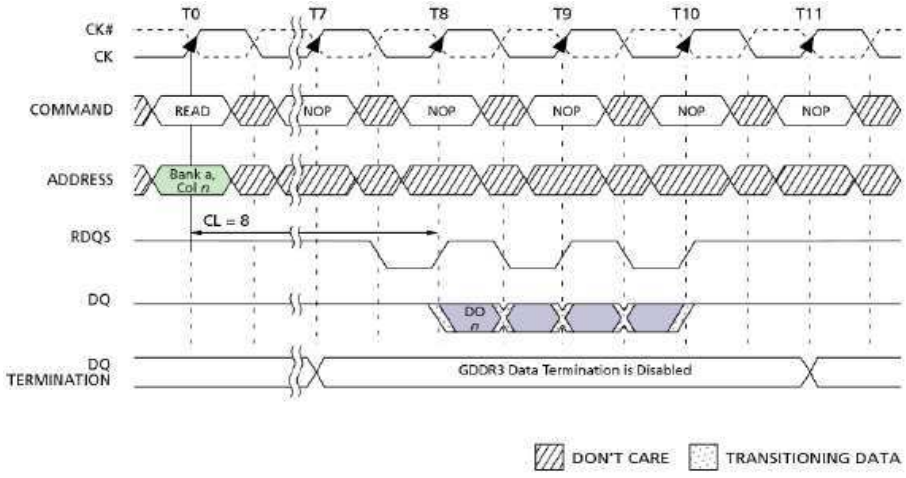
The GDDR3 SDRAM uses a programmable impedance output buffers. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and VSSQ. The value of the resistor must be six times the desired driver impedance. For example, a 240Ω resistor is required for an output impedance of 40Ω. To ensure that output impedance is one-sixth the value of RQ (within 10 percent), RQ should be in the range of 210Ω to 270Ω. (30Ω - 50Ω output impedance).
CK and /CK are not internally terminated. CK and /CK will be terminated on the system module using external 1% resisters.

The output impedance and on die termination is updated during every AUTO REFRRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all datasheet timings and current specifications are met during an update.

A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8 x 3.9us (31.2us). This maximum absolute interval guarantees that the output drivers and the on die terminations of GDDR3 SDRAMs are recalibrated often enough to keep the impedance characteristics of those within the specified boundaries.

ODT Control

Bus snooping for READ commands other than CS# is used to control the on die termination in the dual load configuration. The GDDR3 SGRAM will disable the DQ and RDQS on die termination when a READ command is detected regardless of the state of CS#. The on die termination is disabled x clocks after the READ command where x equals CL-1 and stay off for a duration of BL/2+2CK. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on die termination, for the DQ and DQS pins if a READ command is detected. The on die termination for all other pins on the device is always

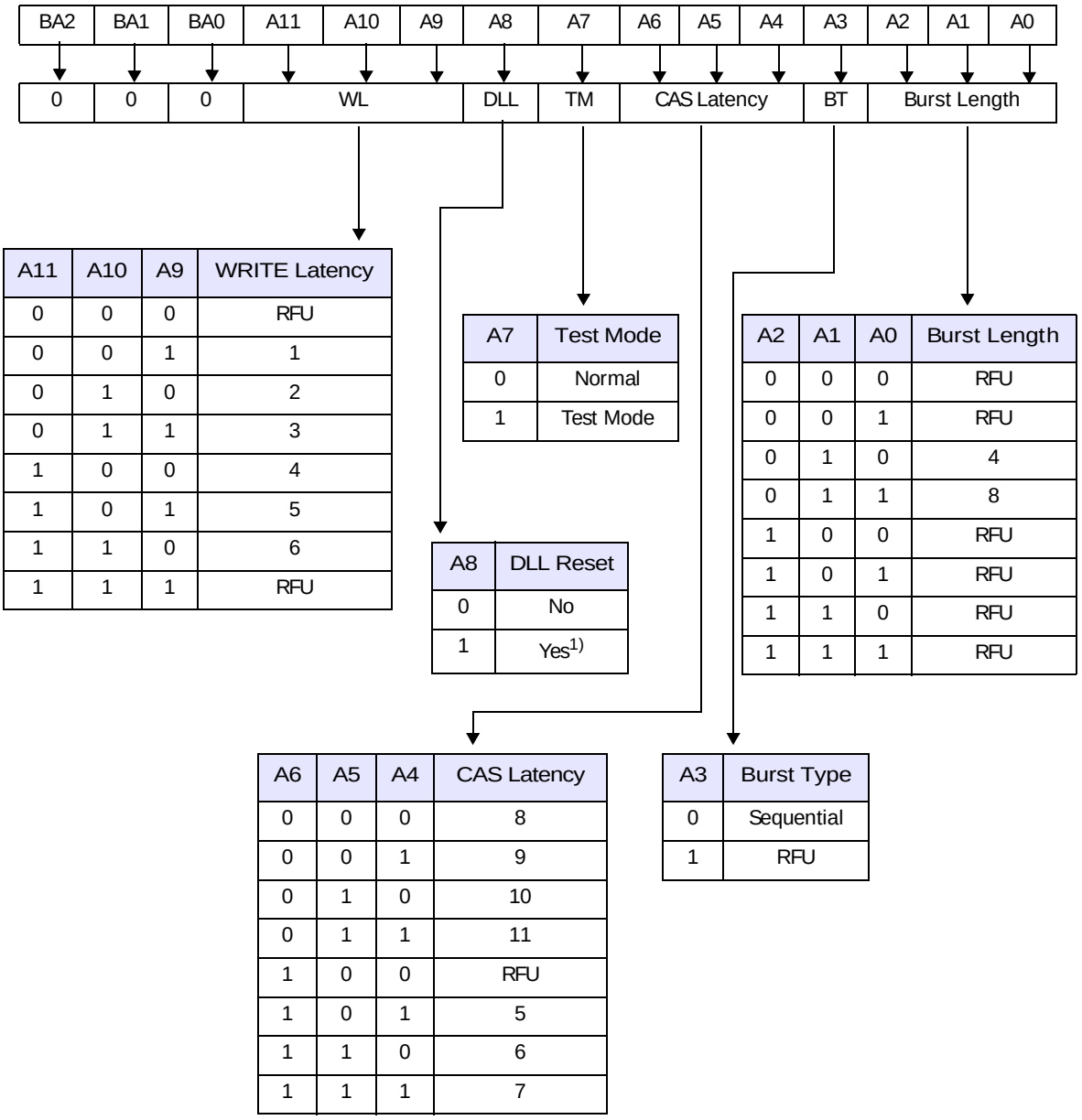


Mode Register Definition

The mode register is used to define the specific mode of operation of the GDDR3 SDRAM. This definition includes the selection of a burst length, CAS latency, WRITE latency, and operating mode, as shown in Figure 3, Mode Register Definition, on page 11. The mode register is porgrammed via the MODE REGISTER SET command (with BA0=0, BA1=0 and BA2=0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing). Re-programming the mode register will not alter the contents of the memory. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A2-A0 specify the burst length; A3 specifies the type of burst (sequential); A4-A6 specify the CAS latency; A7 is a test mode; A8 specifies the operating mode; and A9-A11 specifiy the WRITE latency.

Figure 3: Mode Register Definition



A11	A10	A9	WRITE Latency
0	0	0	RFU
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	RFU

A7	Test Mode
0	Normal
1	Test Mode

A8	DLL Reset
0	No
1	Yes[1)]

A2	A1	A0	Burst Length
0	0	0	RFU
0	0	1	RFU
0	1	0	4
0	1	1	8
1	0	0	RFU
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

A6	A5	A4	CAS Latency
0	0	0	8
0	0	1	9
0	1	0	10
0	1	1	11
1	0	0	RFU
1	0	1	5
1	1	0	6
1	1	1	7

A3	Burst Type
0	Sequential
1	RFU

Note:

1) The DLL reset command is self-clearing.

2) For the each of RFU code means Reserved for Future Use, however with this version, RFU of Burst Length is programmed BL= 4, Burst type is Sequential, Cas Latency is CL=5 and Write Latency is 1.

Burst Length

Read and write accesses to the GDDR3 SDRAM are burst-oriented, with the burst length being programmable, as shown in Figure3, Mode Register Definition. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 4 or 8 locations are available for the sequential burst type. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A2. Ai when the burst length is set to four and by A3. Ai when the burst length is set to eight(where Ai is the most significant column address bit for a given configuration). The remaining(least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

Burst Type

Accesses within a given burst must be programmed to be sequential; this is referred to as the burst type and is selected via bit A3. This device does not support the interleaved burst mode found in DDR SDRAM devices. The ordering of accesses within a burst is determined by the burst length, the burst type, and the starting column address, as shown in Table3.

Table 3: Burst Definition

Burst[1, 2] Length	Starting Column Address			Order of Accesses Within a Burst
				Type=Sequential
4		A1	A0	
		0	0	0-1-2-3
8	A2	A1	A0	
	0	0	0	0-1-2-3-4-5-6-7
	1	0	0	4-5-6-7-0-1-2-3

NOTE:

1. For a burst length of four, A2-A7 select the block of four burst; A0-A1 select the starting column within the block and must be set to zero.
2. For a burst length of eight, A3-A7 select the of eight burst; A0-A2 select the starting column within the block.

CAS Latency

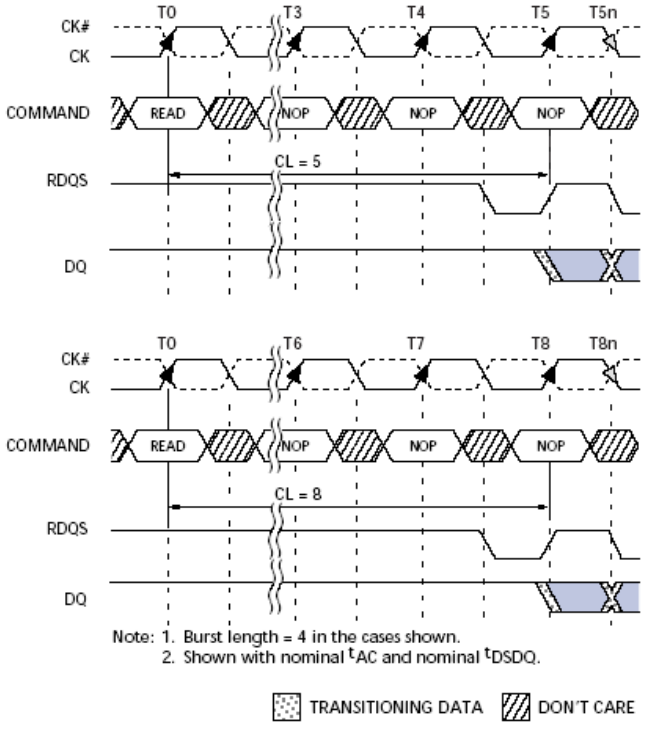
The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 5-11 clocks, as shown in Figure 4, CAS Latency, on page 13. If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m. Table4 indicates the operating frequencies at which each CAS latency setting can be used. For the proper operation, do not change the CL without DLL reset. Or proper CL should be set with DLL reset code

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Table 4: CAS Latency

	ALLOWABLE OPERATING FREQUENCY (MHz)				
SPEED	CL=11	CL=10	CL=9	CL=8	CL=7
-11	900	<=800	<=700	<=600	<=500
-12		800	<=700	<=600	<=500
-14			700	<=600	<=500
-16			-	600	<=500
-2					500

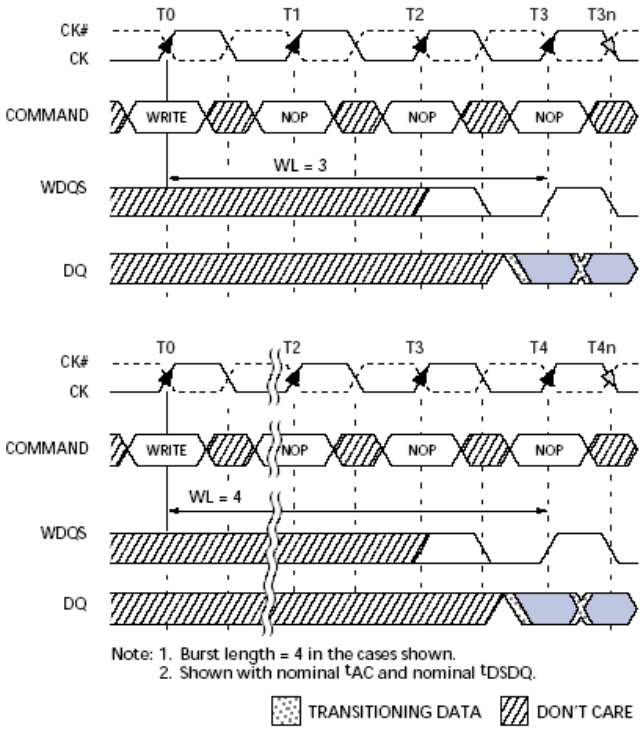
Figure 4: CAS Latency



Write Latency

The WRITE latency (WL) is the delay, in clock cycles,between the registration of a WRITE command and the availability of the first bit of input data as shown in Figure5. The latency can be set from 1 to 6 clocks depending on the operating frequency and desired current draw. When the write latencies are set to 1 or 4 clocks, the input receivers never turn off, in turn, raising the operating power. When the WRITE latency is set to 5 or 6 clocks the input receivers turn on when the WRITE command is registered. If a WRITE command is registered at clock edge n, and the latency is m clocks, the data will be available nominally coincident with clock edge n + m. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 5: WRITE Latency



Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to zero, and bits A0~A6 and A8~ A11 set to the desired values. Test Mode is initiated by issuing a MODE REGISTER SET command with bit A7 set to one, and bits A0~A6 and A8~A11 set to the desired values. Test mode funtions are specific to each DRAM vendor and their exact function are hidden from the user.

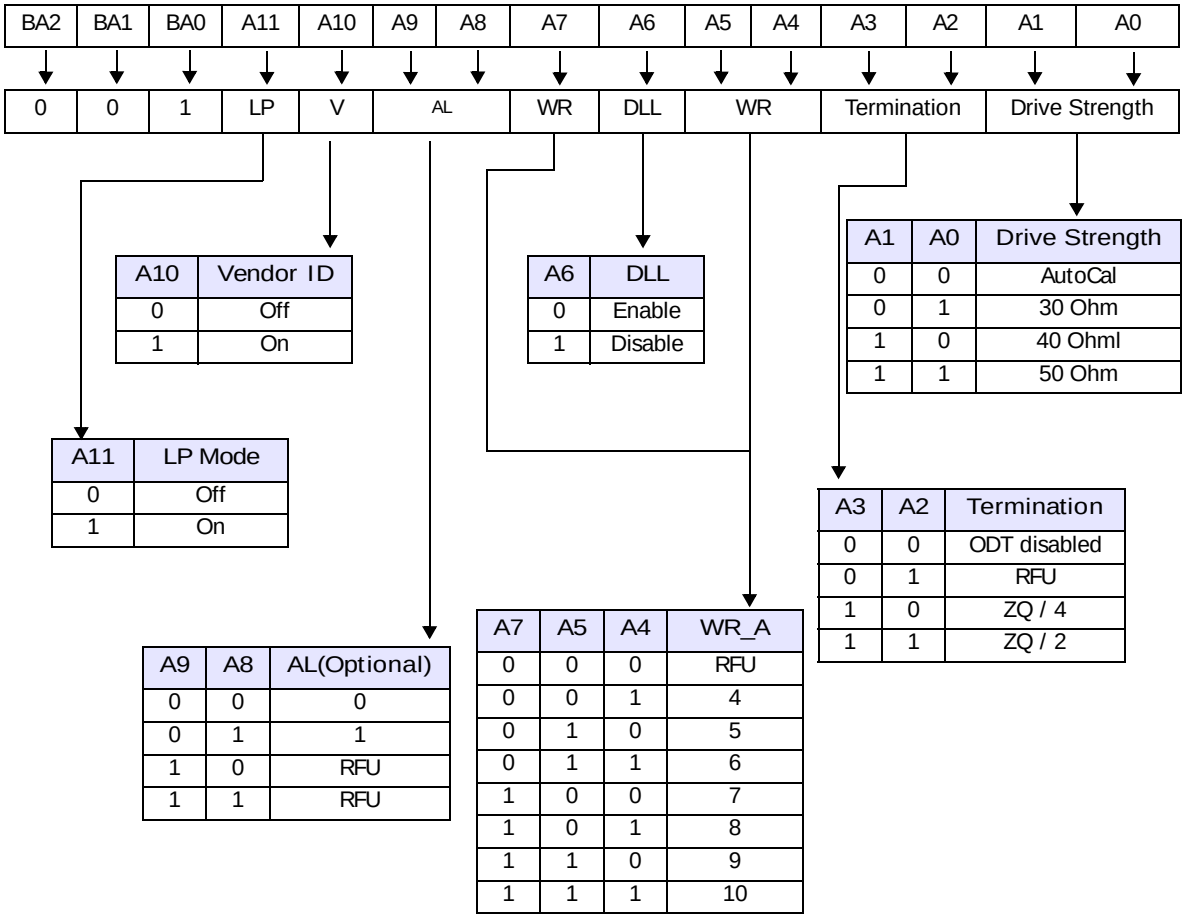
DLL Reset

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits A0~ A7 and A9~A11 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0~A7 and A9~A11 set to the desired values. When a DLL Reset is complete the GDDR3 SDRAM Reset bit, A8 of the mode register is self clearing (i.e.automatically set to a zero by the DRAM). Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, drive strength, data temination, vendor ID, and low-power mode. These functions are controlled via the bits shown in Figure 6, Extended Mode Register Definition. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1, BA1 = 0 and BA2= 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both low) to reset the DLL.The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Figure 6: Extended Mode Register Definition



A10	Vendor ID
0	Off
1	On

A6	DLL
0	Enable
1	Disable

A1	A0	Drive Strength
0	0	AutoCal
0	1	30 Ohm
1	0	40 Ohml
1	1	50 Ohm

A11	LP Mode
0	Off
1	On

A3	A2	Termination
0	0	ODT disabled
0	1	RFU
1	0	ZQ / 4
1	1	ZQ / 2

A9	A8	AL(Optional)
0	0	0
0	1	1
1	0	RFU
1	1	RFU

A7	A5	A4	WR_A
0	0	0	RFU
0	0	1	4
0	1	0	5
0	1	1	6
1	0	0	7
1	0	1	8
1	1	0	9
1	1	1	10

NOTE:

1. The ODT disable function disables DQ,RDQS,WDQS and DM pins.
2. The default setting at Power Up for A3,A2 is 10 or 11
3. A9,A8 are used for Additive Latency setting.
4. If the user activates bits in the extended mode register in an optional field, device will work improperly. Please do not set RFU.
5. The optional values of the drive strength (A1,A0) are only targets and can be determined by the DRAM vendor.
6. WR_A (write recovery time for autoprecharge) in clock cycles is calculated by dividing tWR (in nS) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 20K clock cycles must occur before a READ command can be issued.

tWR(WR_A)

The value of tWR in the AC parametrics table on page 49 of this specification is loaded into register bits 5 and 4. The WR_A (write recovery time for autoprecharge) in clock cycles is calculated by dividing tWR (in ns) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value.

Additive Latency

The Additive Latency function , AL, is used to optimize the command bus efficiency. The AL value is used to determine the number of clock cycles that is to be added to CL after CAS is captured by the rising edge of CK. Thus the total CAS latency is determined by adding CL and AL.

Data Termination

The data termination value is used to define the value for the on die termination for the DQ, DM, and WDQS pins. The GDDR3 device supports one-quarter ZQ and one-half ZQ termination for a nominal 60Ω or 120Ω set with bit E3 and E2 during an EMRS command for a single- or dual-loaded system.

Data Driver Impedence

The Data Driver Impedence, DZ, is used to determine the value of the data drivers impedence. When auto calibration is used the data driver impedence is set to 1/6 ZQ and it's tolerance is determined by the calibration accuracy of the device. When any other value is selected the target impedence is set nominally to the selected impedence. However, the accuracy is now determined by the device's specific process corner, applied voltage and operating temperature.

Low Power Mode

In the Low power mode, Precharge Power Down command activates LP mode. If a Precharge Power Down command issued under the condition of Low Power mode enabled, a device enters the LP mode and it can reduce Precharge Power Down current significantly by disabling DLL during the Precharge Power Down, however it requires more time to exit Power Down. Exit power down timing in Low power mode is defined as tPDIXL(=20K tCK)

Manufacturers Vendor Code Identification

The Manufacturers Vendor Code, V, is selected by issuing an EXTENDED MODE REGISTER SET command with bits A10 set to 1, and bits A0-A9 and A11 set to the desired values. When the V function is enabled the GDDR3 SGRAM will provide its manufacturers vendor code on DQ[3:0] and revision identification on DQ[7:4]. The code will be driven onto the DQ bus after tIDON with respect to the EMRS that set A10 to 1. The DQ bus will be continuously driven until an EMRS write sets A10 back to 0. The DQ bus will be in a Hi-Z state after tIDOFF. The code can be sampled by the controller after waiting tIDON max and before tIDOFF min.

Table 5: Vendor IDs

VENDOR	DQ(3:0)
Reserved	0
Samsung	1
Infineon	2
Elpida	3
Etron	4
Nanya	5
Hynix	*6*
Mosel	7
Winbond	8
ESMT	9
Reserved	A
Reserved	B
Reserved	C
Reserved	D
Reserved	E
Micron	F

Commands

Table6 provides a quick reference of available commands, followed by a description of each command. Two additional truth tables appear following the Operation section; these tables provide current state/next state information.

Table 6: Truth Table - Commands

Note: 1

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	8
NO OPERATION (NOP)	L	H	H	H	X	8
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2
DATA TERMINATOR DISABLE	X	H	L	H	X	10

Table 7: Truth Table 2 - DM Operation

NAME (FUNCTION)	DM	DQS	NOTES
Write Enable	L	Valid	9
Write Inhibit	H	X	8

NOTE:

1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0.BA1 are reserved). A0-A11 provide the opcode to be written to the selected mode register.
3. BA0-BA2 provide bank address and A0-A11 provide row address.
4. BA0-BA2 provide bank address; A0-A7 and A9 provide column address; A8 HIGH enables the auto precharge feature (non-persistent), and A8 LOW disables the auto precharge feature.
5. A8 LOW: BA0-BA2 determine which bank is precharged. A8 HIGH: all banks are precharged and BA0-BA2 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are Don’t Care except for CKE.
8. DESELECT and NOP are functionally interchangeable.
9. Used to mask write data; provided coincident with the corresponding data.
10. Used for bus snooping when the DQ termination is set to 120 ohms in the EMR and cannot be used during power-down or self refresh.

Deselect

The DESELECT function (CS# HIGH) prevents new commands from being executed by the GDDR3 SDRAM. The GDDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

NO Operation (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR3 SDRAM to perform a NOP(CS# LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0~A11. See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0~ BA2 inputs selects the bank, and the address provided on inputs A0~A11 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0~ BA2 inputs selects the bank, and the address provided on inputs A0~A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0~BA2 inputs selects the bank, and the address provided on inputs A0~A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored and a write will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0.BA2 select the bank. Otherwise, BA0. BA2 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state) or if the previouslyopen row is already in the process of precharging.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank precharge function described above but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS min, as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH

The addressing is generated by the internal refresh controller. This makes the address bits a Don't Care during an AUTO REFRESH command. The 512Mb x32 GDDR3 SDRAM requires AUTO REFRESH cycles at an average interval of 3.9us (maximum). A maximum of eight AUTO REFRESH commands can be posted to any given GDDR3 SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 3.9us (35.1us). This maximum absolute interval allows GDDR3 SDRAM output drivers to automatically recalibrate to compensate for voltage and temperature changes. AUTO REFRESH is used during normal operation ofthe GDDR3 SDRAM and is analogous to CAS# -BEFORE-RAS# (CBR) refresh in FPM/EDO DRAMs.This command is nonpersistent, so it must be issued each time a refresh is required.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR3 SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the GDDR3 SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled(LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The on-die termination is also disabled upon entering Self Refresh except for CKE and enabled upon exiting Self Refresh. (20K clock cycles must then occur before a READ command can be issued). Input signals except CKE are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the GDDR3 SDRAM must have NOP commands issued for tXSNR because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements and output calibration is to apply NOPs for 1000 clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate. If the GDDR3 device enters SELF REFRESH with the DLL disabled the GDDR3 device will exit SELF REFRESH with the DLL disabled.

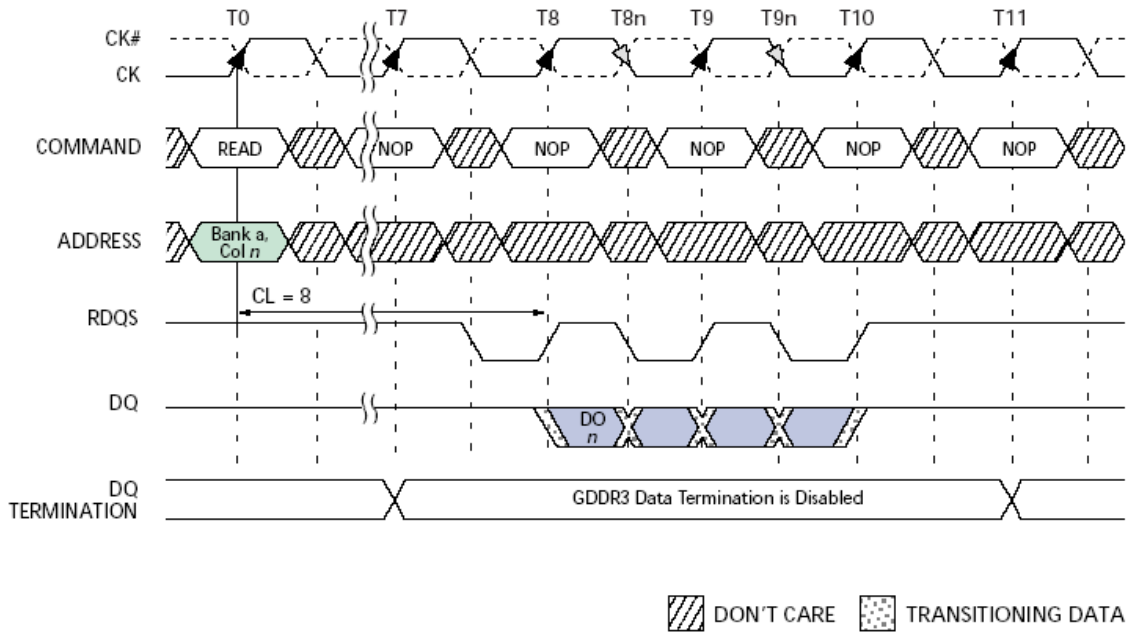
DATA TERMINATOR DISABLE (BUS SNOOPING FOR READ COMMANDS)

Bus snooping for READ commands other than CS# isused to control the on-die termination in the dual load configuration. The GDDR3 SDRAM will disable the on-die termination when a READ command is detected, regardless of the state of CS#, when the ODT for the DQ pins are set for dual loads (120Ω).The on-die termina-tion is disabled x clocks after the READ command where x equals CL-1 and stay off for a duration of BL/2 +2CK, as shown in Figure8, Data Termination Disable Timing on page15. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on-die termination if a READ command is detected. The on-die termination for all other pins on the device are always turned-on for both a single-rank system and a dual-rank system.

Boundary Scan Test Mode

The 512Mb GDDR3 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.11990. To save the current GDDR3 ballout, this mode will scan the parallel data input and output the scanned data through WDQS0 pin controlled by an addon pin, SEN which is located at V4 of 136 ball package. You can find the detailed descriptions of this feature on Appendix C (page 58).

Figure 8: Data Termination Disable Timing



NOTE:

1. DO n = data-out from column n.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO n.
4. Shown with nominal tAC and tDQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge.
6. The Data Terminators are disabled starting at CL - 1 and the duration is BL/2 + 2CK.
7. READS to either rank disable both ranks' termination regardless of the logic level of CS#.

Operations

Bank/Row Activation

Before any READ or WRITE commands can be issued to a bank within the GDDR3 device, a row in that bank must be “opened.”

This is accomplished via the ACTIVE comand, which selects both the bank and the row to be activated, as shown in Figure 9, Activating a Specific Row in a Specific Bank. After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD min should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a tRCD specification of 15ns with a 500 MHz clock(2.0ns period) results in 7.5 clocks rounded to 8.

This is reflected in Figure 10, Example: Meeting tRCD, which overs any cases where 7 < tRCDMIN/tCK <= 8. The same procedure is used to convert other specification limits from time units to clock cycles. A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed,which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.

Figure 9: Activating a Specific Row in a Specific Bank

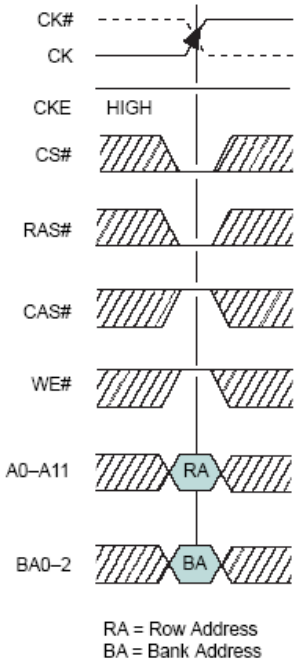
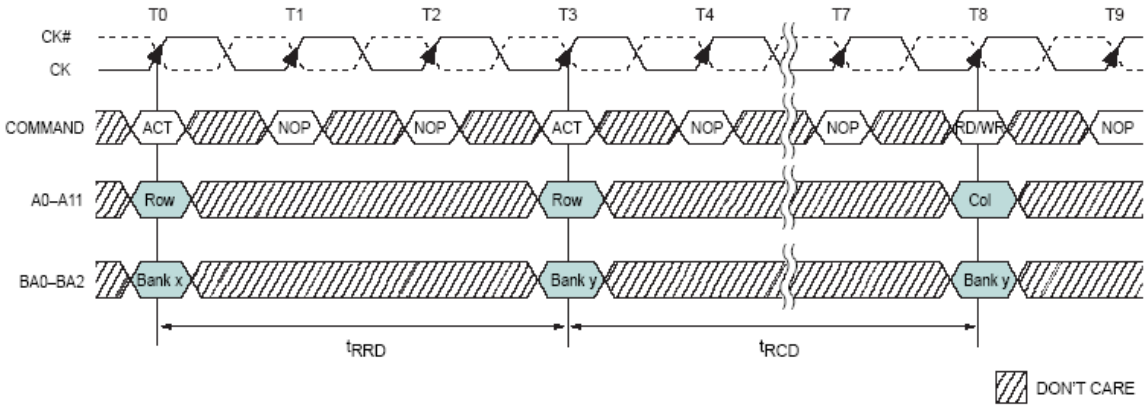


Figure 10: Example: Meeting tRCD



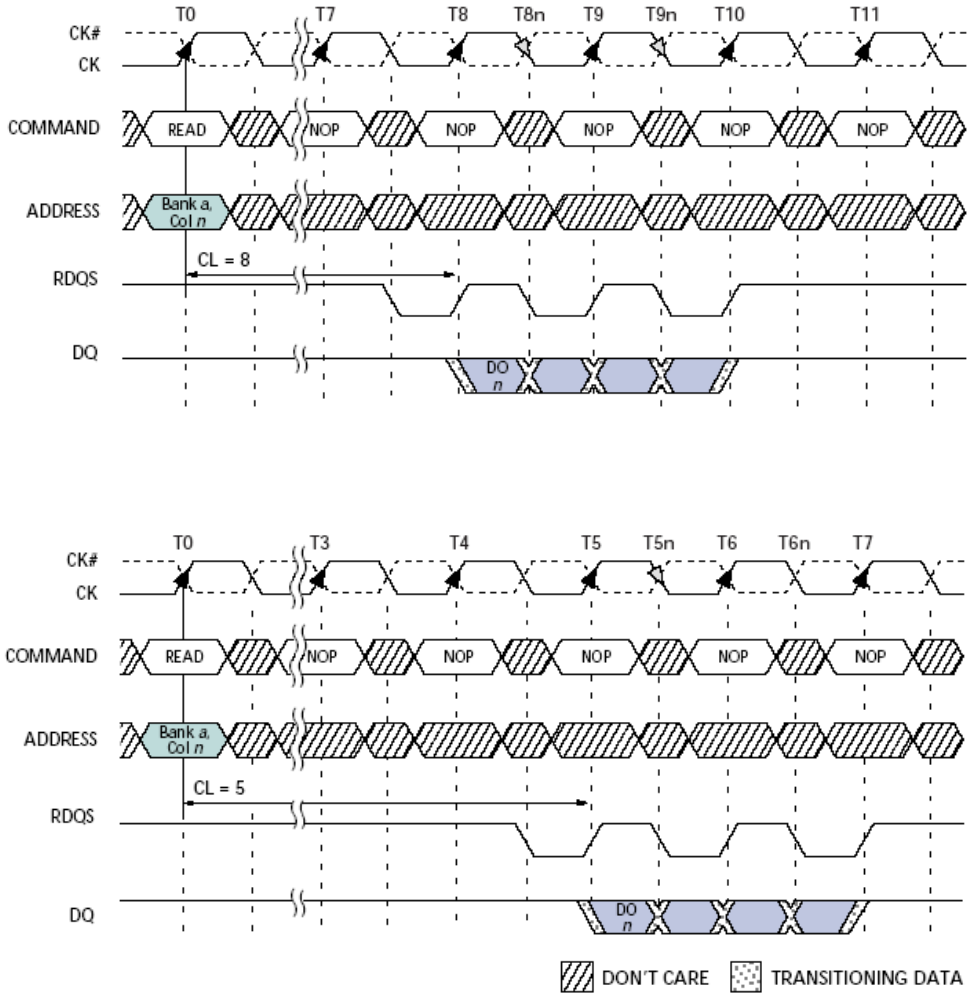
READ Timing

READ burst is initiated with a READ command.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS min has been met.

During READ bursts, the first valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative RDQS edges. The GDDR3 SGRAM drives the output data edge aligned to RDQS. And all outputs, i.e. DQs and RDQS, are also edge aligned to the clock. Prior to the first valid RDQS rising edge, a cycle is driven and specified as the READ preamble. The preamble consists of a half cycle High followed by a half cycle Low driven by the GDDR3 SGRAM. The cycle on RDQS consisting of a half cycle Low coincident with the last data-out element followed by a half cycle High is known as the read postamble, and it will be driven by the SGRAM. The SGRAM toggles RDQS only when it is driving valid data out onto on the bus.
Upon completion of a burst, assuming no other command has been initiated; the DQs and RDQS will go to be in Hi-Z state. VDDQ due to the on die termination. long as the bus turn around time is met. READ data cannot be terminated or truncated.
A PRECHARGE can also be issued to the SGRAM with the same timing restriction as the new READ command if tRAS is met as shown in Figure 17, READ to Precharge, on page 29. A WRITE can be issued any time after a READ command as long as the bus turn around time is met as shown in Figure 16, READ to WRITE, on page 28. READ data cannot be terminated or truncated

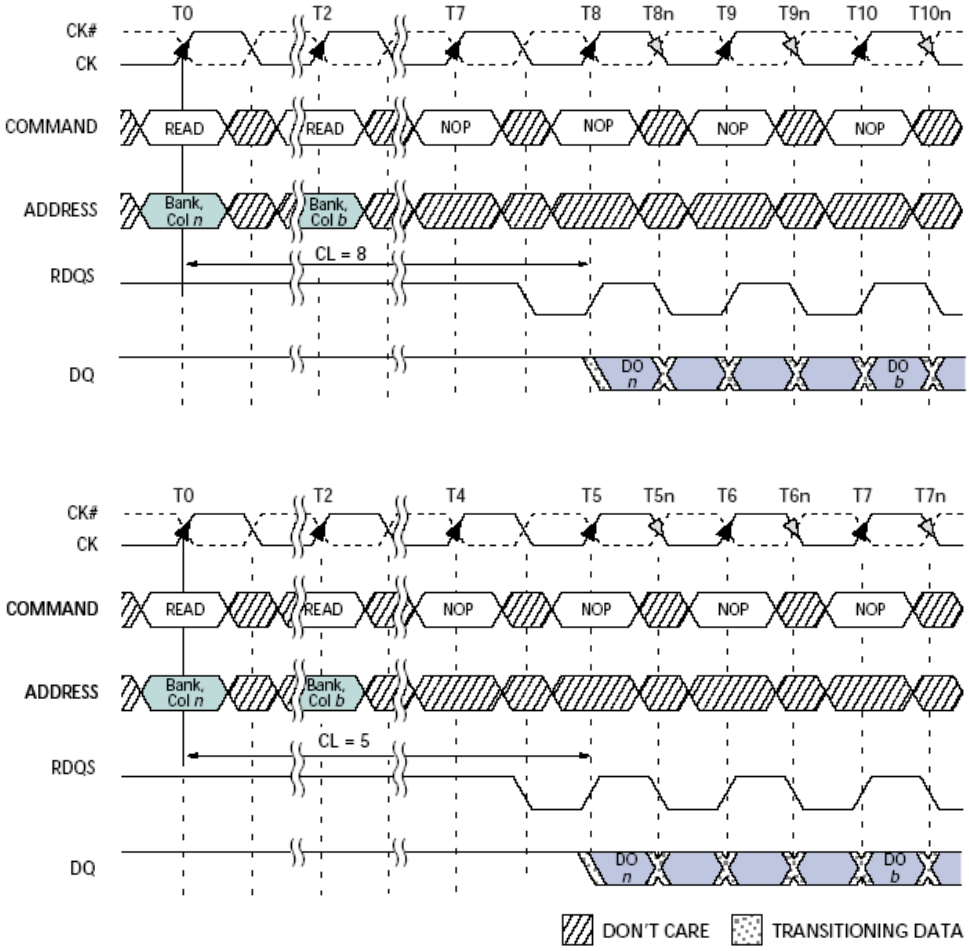
Figure 12: READ Burst



NOTE:

1. DO n = data-out from column n.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the specified order following DO n.
4. Shown with nominal tAC and tDQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge.

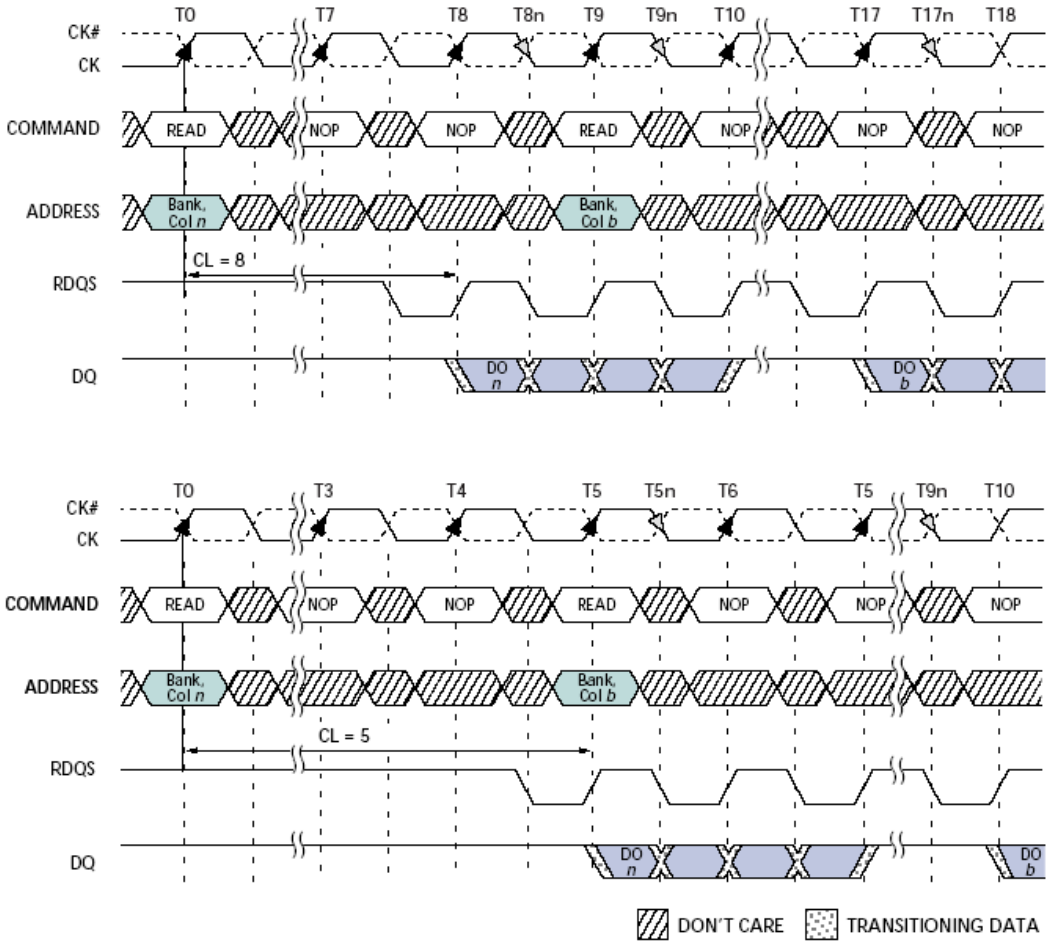
Figure 13: Consecutive READ Bursts



NOTE:

1. DO n (or b) = data-out from column n (or column b).
2. Burst length = 4
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal tAC, and tDQSQ.
6. Example applies only when READ commands are issued to same device.
7. RDQS will start driving high one half clock cycle prior to the first falling edge of RDQS.

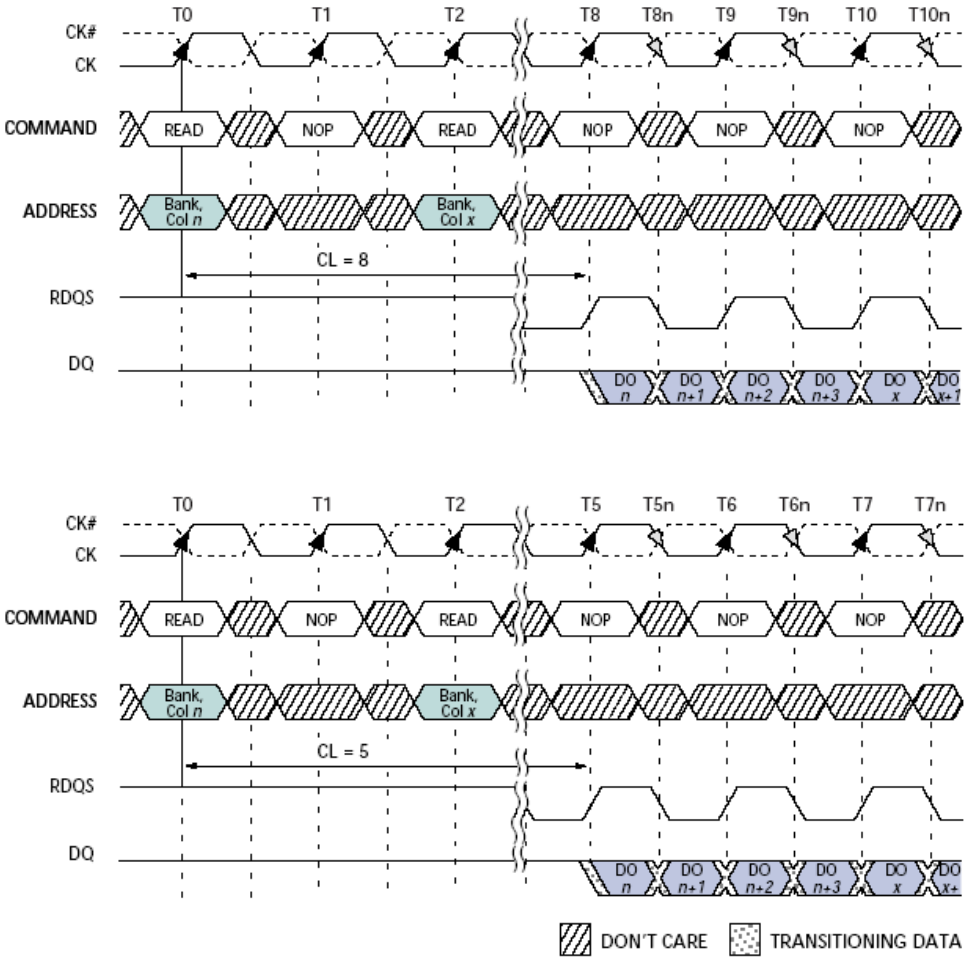
Figure 14: Non-Consecutive READ Bursts



NOTE:

1. DO n (or b) = data-out from column n (or column b).
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Three subsequent elements of data-out appear in the programmed order following DO b.
5. Shown with nominal tAC and tDQSQ.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one-half clock cycle prior to the first falling edge of RDQS.

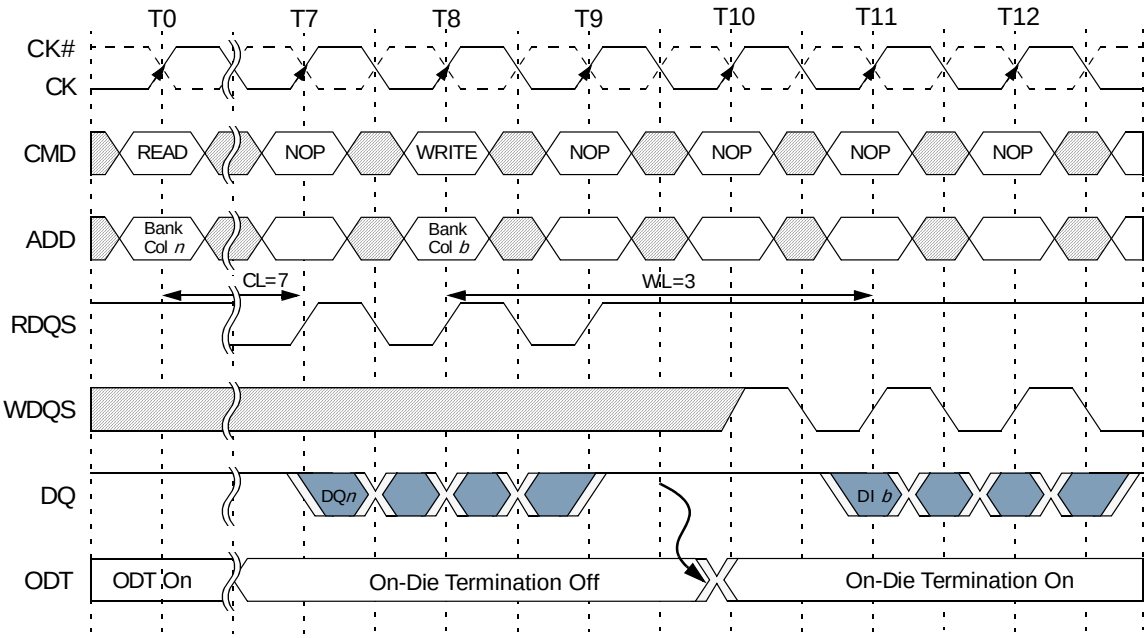
Figure 15: Random Read Accesses



NOTE:

1. DO n (or x or b or g) = data-out from column n (or column x or column b or column g).
2. Burst length = 4.
3. READs are to an active row in any banks.
4. Shown with nominal tAC and tDQSQ.
5. RDQS will start driving high one-half clock cycle prior to the first falling edge of RDQS.

Figure 16: Read to Write

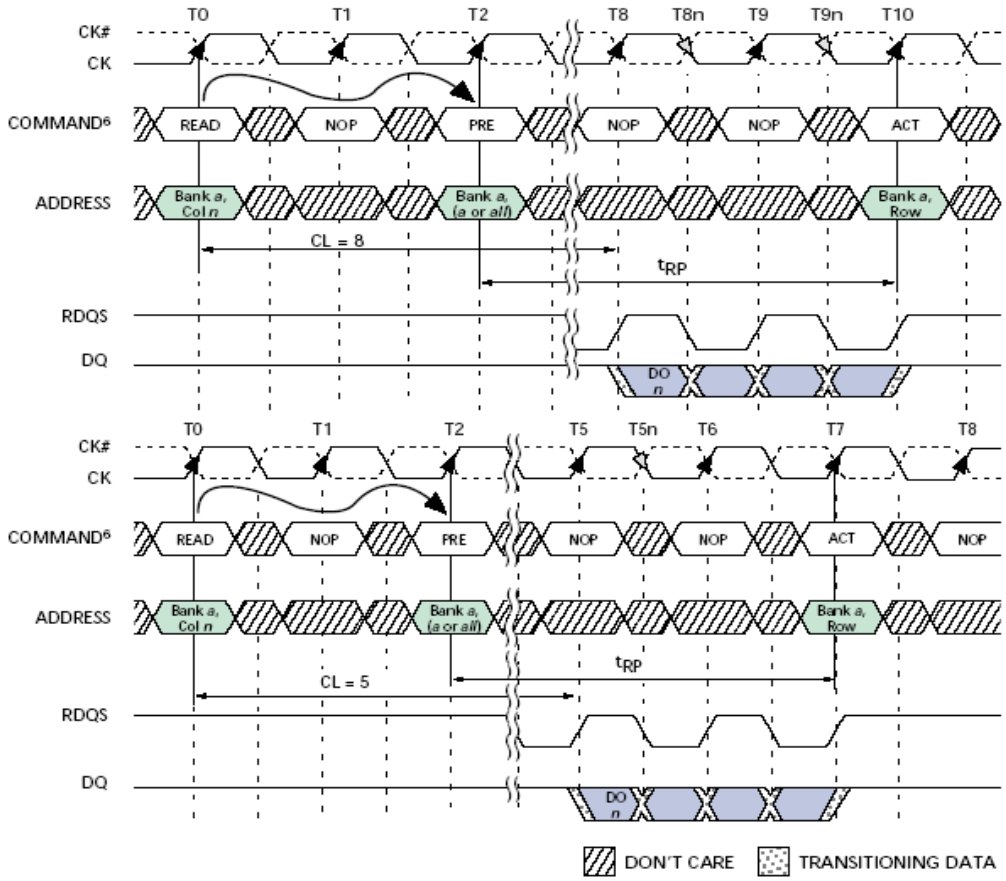


CL=7, BL=4, WL=3

NOTE:

1. DQ *n* = Data-out from column n.
2. DI *b* = Data-in from column b.
3. Shown with nominal tAC, tDQSQ and tDQSS.
4. Read Preamble consists of a half cycle High followed by a half cycle Low driven by device
5. Write Data connot be driven onto the DQ bus for 2 clocks after the READ data is off the bus.
6. The timing diagram covers a READ to a WRITE command from different device, different bank or the same row in the same bank.

Figure 17: READ to Precharge



NOTE:

1. DO n = data-out from column n.
2. Burst length = 4.
3. Three subsequent elements of data-out appear in the programmed order following DO n.
4. Shown with nominal tAC and tDQSQ.
5. READ to PRECHARGE equals two clocks, which enables two data pairs of data-out.
6. PRE = PRECHARGE command; ACT = ACTIVE command.
7. RDQS will start driving high one-half clock cycle prior to the first falling edge of RDQS.

WRITE Timing

WRITE burst is initiated with a WRITE command.

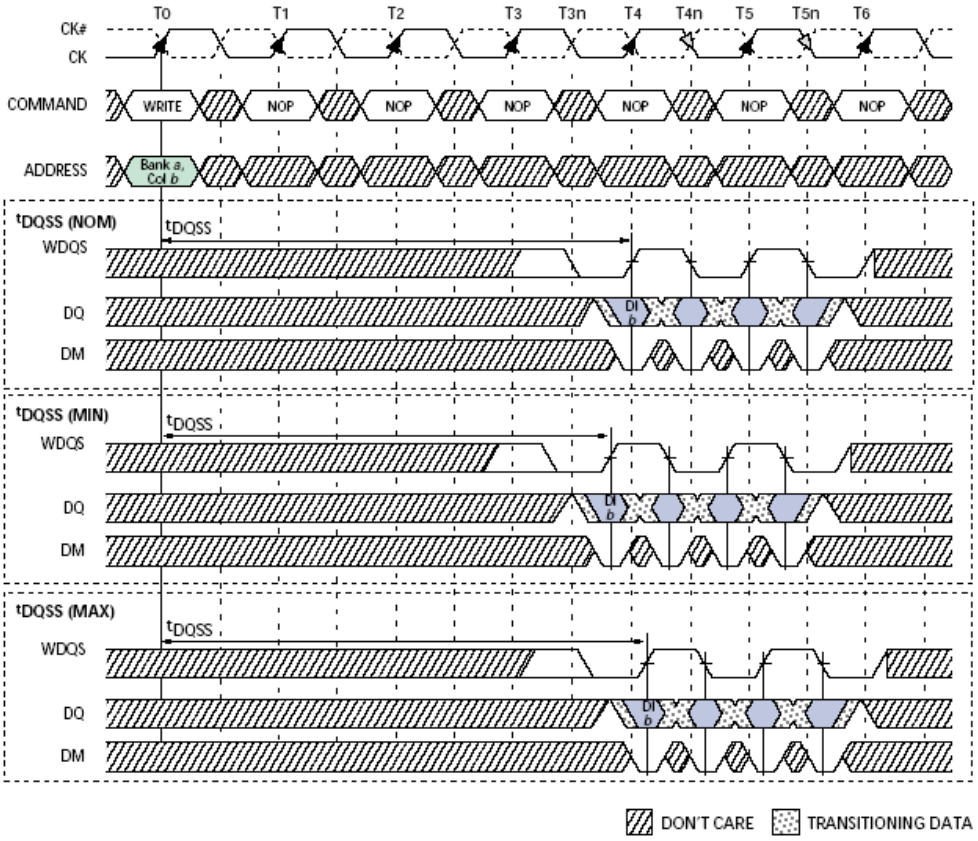
The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

During WRITE bursts, the first valid data-in element will be registered on the rising edge of WDQS following the write latency set in the mode register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS rising edge, a cycle is needed and specified as the WRITE Preamble. The preamble consists of a half cycle High followed by a half cycle Low driven by the controller. The cycle on WDQS following the last data-in element is known as the write postamble and must be driven High by the controller, it can not be left to float High using the on die termination. The WDQS should only toggle on data transfers.

The time between the WRITE command and the first valid rising edge of WDQS (tDQSS) is specified relative to the write latency (WL - 0.2CK and WL + 0.2CK). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS [MIN] and tDQSS [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other command has been initiated, the DQs should remain Hi-Z and any additional input data will be ignored.

Data for any WRITE burst may not be truncated with any subsequent command. A subsequent WRITE command can be issued on any positive edge of clock following the previous WRITE command assuming the previous burst has completed. The subsequent WRITE command can be issued x cycles after the previous WRITE command, where x equals the number of desired nibbles x2 (nibbles are required by 4n-prefetch architecture) i.e. BL/2. A subsequent READ command can be issued once tWTR is met or a subsequent PRECHARGE command can be issued once tWR is met. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

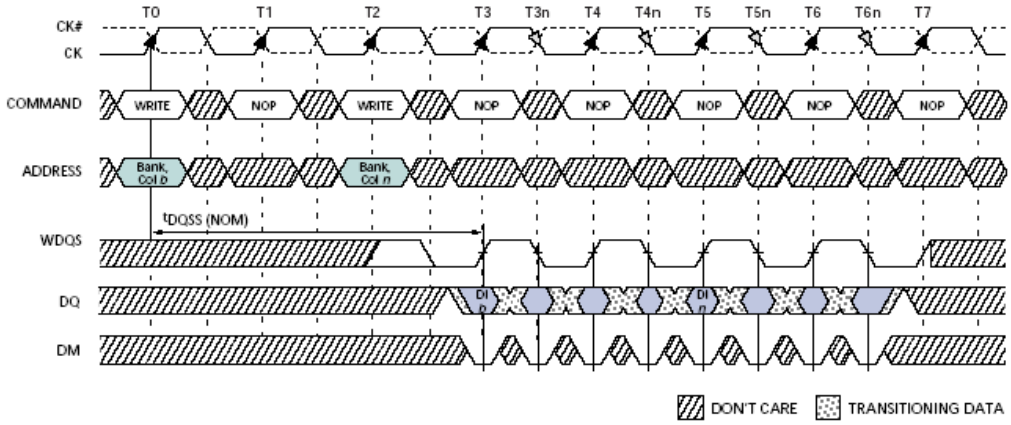
Figure 19: WRITE Burst



NOTE:

1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the specified order following DI b.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. Write latency is set to 4.

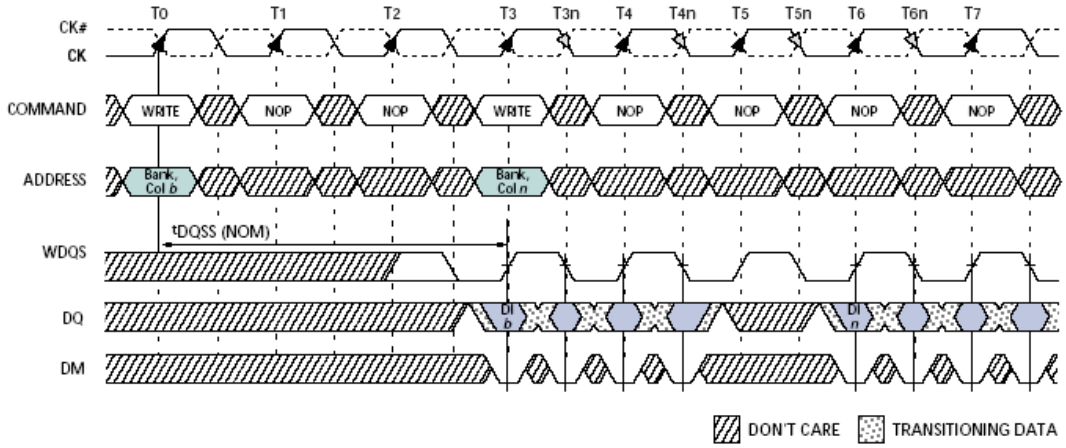
Figure 20: Consecutive WRITE to WRITE



NOTE:

1. DI b, etc. = data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the specified order following DI b.
3. Three subsequent elements of data-in are applied in the specified order following DI n.
4. Burst of 4 is shown.
5. Each WRITE command may be to any bank of the same device.
6. WRITE latency is set to 3.

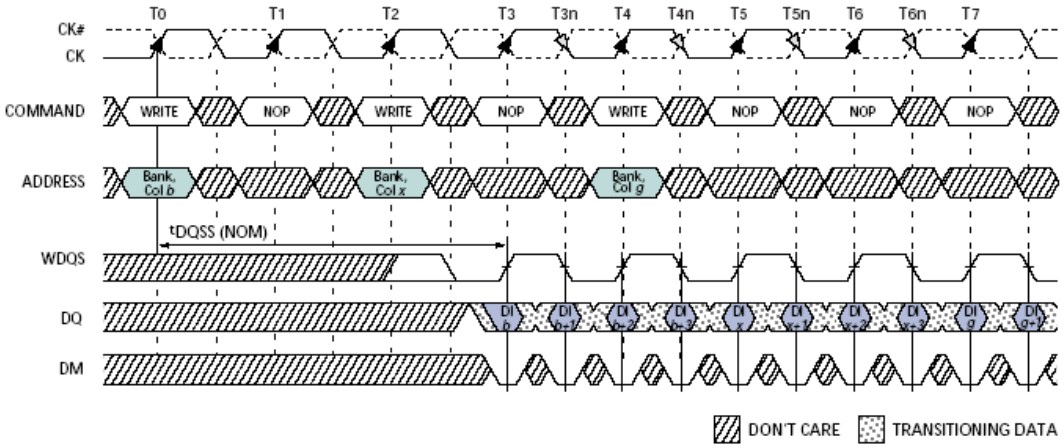
Figure 21: NonConsecutive WRITE to WRITE



NOTE:

1. DI b, etc. = data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the specified order following DI b.
3. Three subsequent elements of data-in are applied in the specified order following DI n.
4. A burst of 4 is shown.
5. Each WRITE command may be to any banks.
6. WRITE latency set to 3.

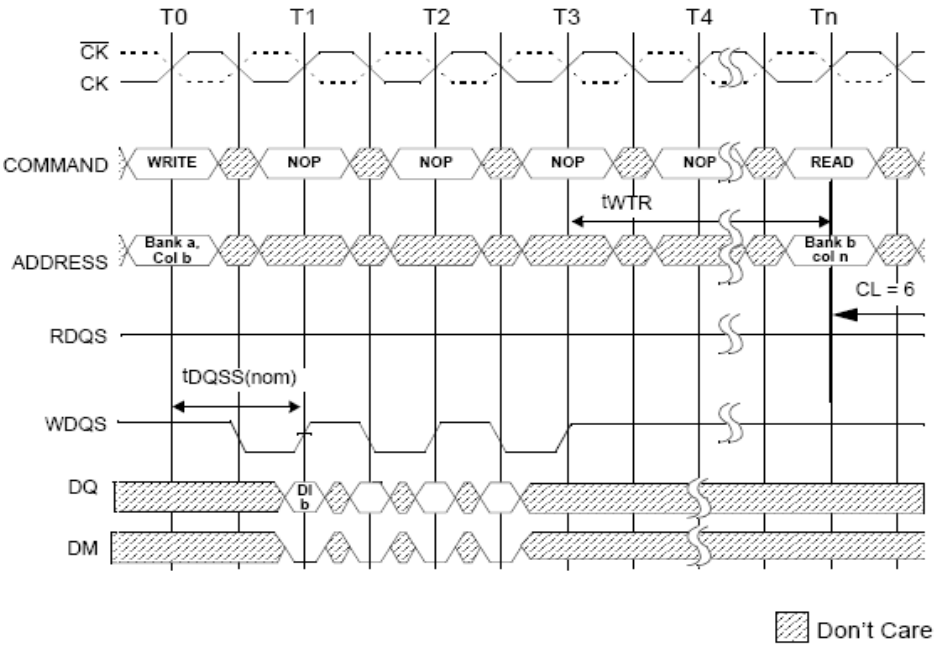
Figure 22: Random WRITE Cycles



NOTE:

1. DI b, etc. = data-in for column b, etc.
2. b', etc. = the next data-in following DI b, etc., according to the specified burst order.
3. Programmed burst length = 4 case is shown.
4. Each WRITE command may be to any banks.
5. Last write command will have the rest of the nibble on T8 and T8n.
6. WRITE latency is set to 3.

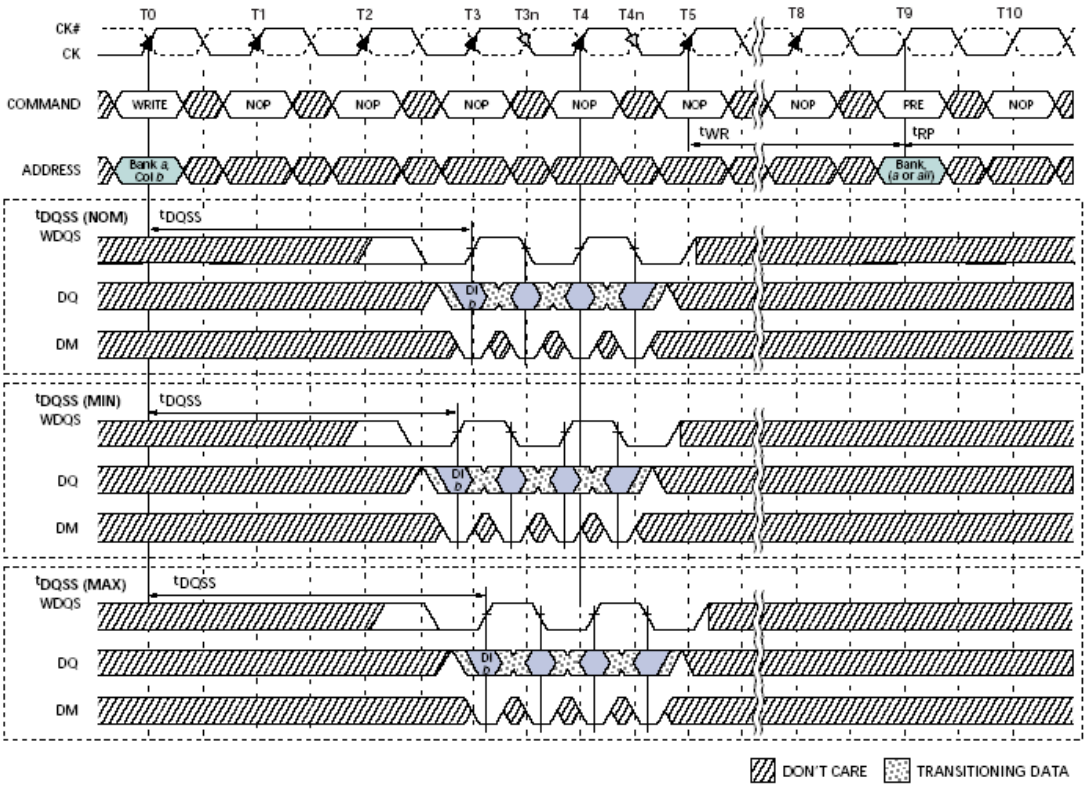
Figure 23: WRITE to READ Timing



NOTE:

1. DI b = Data In for column b
2. Three subsequent elements of Data In are applied following D1 b
3. tWTR is referenced from the first positive CK edge after the last Data In
4. The READ and WRITE commands may be to any bank.
5. WRITE Latency is set to 1

Figure 24: WRITE to PRECHARGE



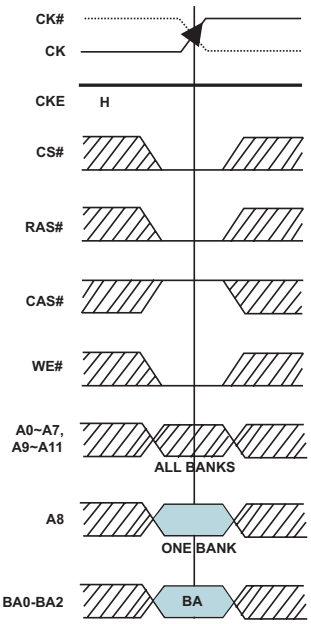
NOTE:

1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the specified order following DI b.
3. A burst of 4 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. WRITE latency is set to 3.
6. The 4n prefetch architecture requires a 2-clock WRITE-to-READ turnaround time (tWTR).

PRECHARGE

The PRECHARGE command (shown in Figure25) issused to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the precharge command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0-BA2 select the bank. When all banks are to be precharged, inputs BA0-BA2 are treated as "Don't Care." Once a bank has been pre-charged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Figure 25: PRECHARGE Command



BA=Bank Address(if A8 is LOW; otherwise "Don't Care")

POWER-DOWN (CKE Not Active)

Unlike SDR SDRAMs, GDDR3 SDRAMs require CKE to be active at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied. Power-down (shown in Figure26, Power-Down, on page38) is entered when CKE is registered low. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any banks, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK# and CKE. For maximum power savings, the user also has the option of disabling the DLL prior to entering power-down. In that case, the DLL must be enabled and reset after exiting power-down, and 20K clock cycles must occur before a READ command can be issued. However, power-down duration is limited by the refresh requirements of the device, so in most applications, the self refresh mode is preferred over the DLL-disabled power-down mode. While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the GDDR3 SDRAM, while all other input signals are "Don't Care." The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied four clock cycles later.

Figure 26: Power-Down

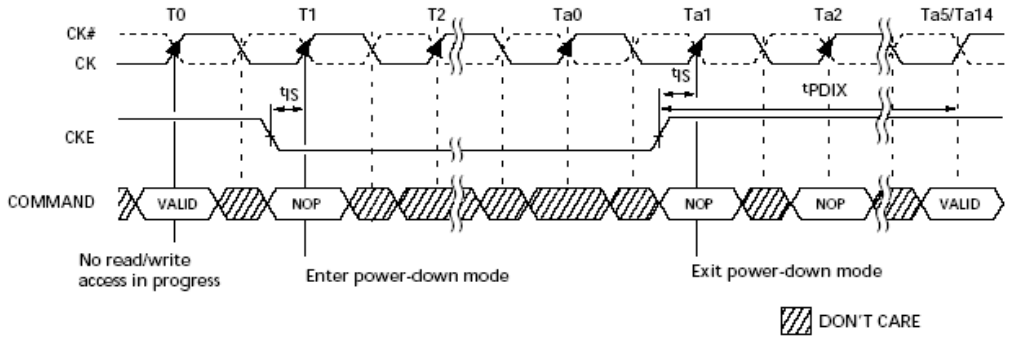


Table 8: Truth Table - CKE

Notes: 1~4; notes appear below table

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power-Down	X	Maintain Power-Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
L	H	Self Refresh	DESELECT or NOP	Exit Self Refresh	5
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Dwon Entry	
H	L	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Truth Table 3		

NOTE:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the GDDR3 SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the tXSR period. A minimum of 20K clock cycles is needed for the DLL to lock before applying a READ command if the DLL was disabled.

Table 9: Truth Table - Current State Bank n - Command to Bank n

Notes: 1~3; notes appear below table

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	L	L	H	H	ACTIVE (select and activate row)	
Idle	L	L	L	H	AUTO REFRESH	4
	L	L	L	L	LOAD MODE REGISTER	4
Row Active	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	5
Read (Auto Pre-charge Disabled)	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6, 8
	L	L	H	L	PRECHARGE (truncate READ burst , start Precharge)	5
Write (Auto Pre-charge Disabled)	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE (truncate WRITE burst, start Precharge)	5, 7

NOTE:

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH (see Truth Table 2) and after tXSNR has been met (if the previ-ous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled.
   Write: A WRITE burst has been initiated, with auto precharge disabled.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table9, and according to Table10. Precharging: Starts with registration of a PRECHARGE command and ends when tRP is met. Once tRP ismet, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the “row active” state.
   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
   Write w/ Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRC is met. Once tRC is met, the GDDR3 x32 will be in the all banks idle state.
   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when tMRD has been met. Once tMRD is met, the GDDR3 x32 will be in the all banks idle state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, all banks will be in the idle state. READ or WRITE: Starts with the registation of the ACTIVE command and ends the last valid data nibble.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.
10. Requires appropriate DM masking.
11. A WRITE command may be applied after the completion of the READ burst

Table 10: Truth Table - Current State Bank n - Command to Bank m

Notes: 1~5; notes appear below table

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read(With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write(With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	

NOTE:

1. This table applies when CKEn-1 was HIGH and CKEn is HIGH (see Table9) and after tXSNR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank n and the commands shown are those allowed to be issued to bank m, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

   Idle: The bank has been precharged, and tRP has been met.

   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

   Read: A READ burst has been initiated, with auto precharge disabled.

   Write: A WRITE burst has been initiated, with auto precharge disabled.

   Read with Auto Precharge Enabled: See following text

   Write with Auto Precharge Enabled: See following text

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a commandto a different bank is summarized below.

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. All states and sequences not shown are illegal or reserved.

6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.

7. Requires appropriate DM masking.

Table 11: Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	[WL + (BL/2)] tCK + tWTR
	WRITE or WRITE with AUTO PRECHARGE	(BL/2) tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK
READ with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	(BL/2) * tCK
	WRITE or WRITE with AUTO PRECHARGE	[CL + (BL/2) + 2 - WL] * tCK *1)*
	PRECHARGE	1 tCK
	ACTIVE	1 tCK

NOTE:

CL = CAS latency (CL) rounded up to the next integer.

BL = Burst length.

WL = WRITE latency.

1) Write Data connot be driven onto the DQ bus for 2 clocks after the READ data is off the bus.(refer to Fig16. on the page28)

Absolute Maximum Ratings*

Voltage on Vdd Supply
Relative to Vss .....-0.5V to +2.5V
Voltage on VddQ Supply
Relative to Vss .....-0.5V to +2.5V
Voltage on Vref and Inputs
Relative to Vss .....-0.5V to +2.5V
Voltage on I/O Pins
Relative to Vss .....-0.5V to VddQ +0.5V
MAX Junction Temperature, TJ .....+125℃
Storage Temperature (plastic).....-55℃ to +150℃
Power Dissipation.....TBD
Short Circuit Output Current.....50mA

* Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 12: DC Electrical Characteristics and Operating Conditions

(Recommended operating conditions; 0℃ <= TC <= 85℃)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS	Remark
Supply Voltage	VDD	1.74	1.8	2.15	V	1
I/O Supply Voltage	VDDQ	1.74	1.8	2.15	V	1
Supply Voltage	VDD	1.94	2.0	2.15	V	2
I/O Supply Voltage	VDDQ	1.94	2.0	2.15	V	2
Supply Voltage	VDD	2.1	2.2	2.3	V	3
I/O Supply Voltage	VDDQ	2.1	2.2	2.3	V	3
I/O Reference Voltage	VREF	0.69xVDDQ	0.70xVDDQ	0.71xVDDQ	V	
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	-	-	V	
Input Low (Logic 0) Voltage	VIL(DC)	-	-	VREF-0.15	V	
INPUT LEAKAGE CURRENT Any Input 0V <= Vin <= Vdd (All other pins not under test = 0V)	II	-5	-	5	uA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V <= Vout <= VddQ)	IOZ	-5	-	5	uA	
OUTPUT Logic Low	VOL(DC)	-	-	0.76	V	

Note:

1. Supports 500/600MHz
2. Supports 700MHz
3. Supports 800/900MHz

Table 13: AC Input Operating

(Recommended operating conditions; 0℃ <= TC <= 85℃)

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Input High (Logic 1) Voltage; DQ	VIH(AC)	VREF+0.250	-	-	V
Input Low (Logic 0) Voltage; DQ	VIL(AC)	-	-	VREF-0.250	V
Clock Input Differential Voltage; CK and CK#	Vid(AC)	0.5	-	VDDQ+0.5	V
Clock Input Crossing Point Voltage; CK and CK#	Vix(AC)	VREF-0.15	VREF-0.15	VREF+0.15	V

OUTPUT IMPEDANCE AND TERMINATION DC ELECTRICAL CHARACTERISTICS

The Driver and Termination impedances are determined by applying VDDQ/2 nominal (0.9v) at the corresponding input or output and by measuring the current flowing into or out of the device. VDDQ is set to the nominal 1.8v.

- IOH is the current flowing out of DQ when the Pull-up transistor is activated and the DQ termination is disabled
- IOL is the current flowing out of DQ when the Pull-down transistor is activated and the DQ termination is disabled
- ITCAH(ZQ/2) is the current flowing out of the Termination of Commands and Addresses for a ZQ/2 termination value
- ITCAH(ZQ) is the current flowing out of the Termination of Commands and Addresses for a ZQ termination value.
- ITDQH(ZQ/4) is the current flowing out of the Termination of the DQs for a ZQ/4 termination value.
- ITDQH(ZQ/2) is the current flowing out of the Termination of the DQs for a ZQ/2 termination value

Note:
Measurement performed with VDDQ = 1.8v (nominal) and by applying VDDQ/2 (0.9v) at the corresponding Input or Output. (0℃ <= Tc <= +85℃)

Table 14: Driver and Termination DC Characteristics

PARAMETER	ZQ VALUE	200		240		280		OHM	
		MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
IOH	ZQ/6	24.5	30.0	20.5	25.0	17.5	21.4	mA	
IOL	ZQ/6	24.5	30.0	20.5	25.0	17.5	21.4	mA	
ITCAH (ZQ/2)	ZQ/2	8.2	10.0	6.8	8.3	5.8	7.1	mA	
ITCAH (ZQ)	ZQ	4.1	5.0	3.4	4.2	11.7	14.3	mA	
ITDQH (ZQ/4)	ZQ/4	16.4	18.0	13.6	16.7	11.7	14.3	mA	
ITDQH (ZQ/2)	ZQ/2	8.2	10.0	6.8	8.3	5.8	7.1	mA	

Figure 27: Input and Output Voltage Waveform

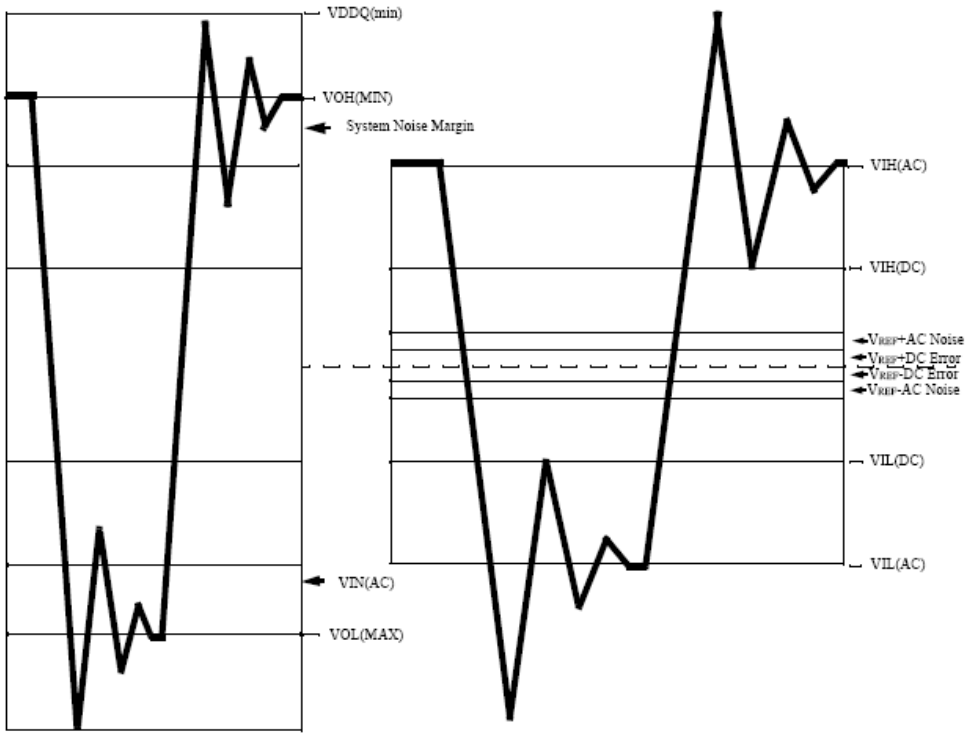
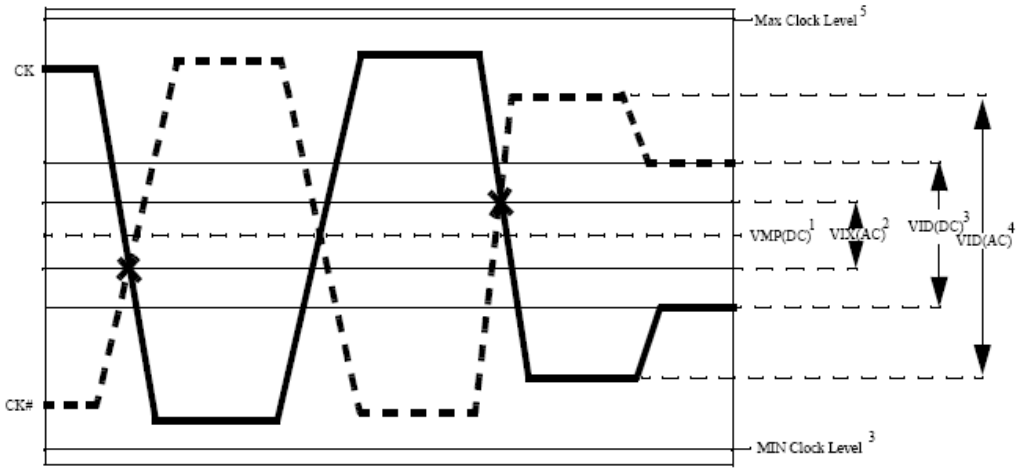


Table 16: Clock Input Operating Conditions

PARAMETER/CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Clock Input Midpoint Voltage; CK and CK#	V_{MP}(DC)	1.16	1.26	1.36	V
Clock Input Voltage Level; CK and CK#	V_{IN}(DC)	0.42	-	V_{DDQ}+0.3	V
Clock Input Differential Voltage; CK and CK#	V_{ID}(DC)	0.22		V_{DDQ}	V
Clock Input Differential Voltage; CK and CK#	V_{ID}(AC)	0.5		V_{DDQ}+0.5	V
Clock Input Crossing Point Voltage; CK and CK#	V_{IX}(AC)	V_{REF}-0.15	0.70xV_{DDQ}	V_{REF}+0.15	V

Figure 28: Clock Input



NOTE:

1. This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of VDDQ.
2. CK and CK# must cross in this region.
3. CK and CK# must meet at least VIN(DC) MIN when static and is centered around VMP(DC).
4. CK and CK# must have a minimum 600mV peak-to-peak swing.
5. CK or CK# may not be more positive than VDDQ + 0.5V or lower than 0.22V.
6. For AC operation, all DC clock requirements must also be satisfied.
7. Numbers in diagram reflect nominal values.

Table 17: Capacitance

Note: 13; notes appear on pages 49,50

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DQS, DM	DCIO	-	0.20	pF	24
Delta Input Capacitance: Command and Address	DCI1	-	0.40	pF	29
Delta Input Capacitance: CK, CK#	DCI2	-	0.10	pF	29
Input/Output Capacitance: DQs, DQS, DM	CIO	2.5	4.5	pF	
Input Capacitance: Command and Address	CI1	2.0	4.0	pF	
Input Capacitance: CK, CK#	CI2	2.0	4.0	pF	
Input Capacitance: CKE	CI3	2.0	4.0	pF	

Table 18: IDD Specifications and Conditions

Note:1-5, 10, 12, 14, 40; notes on page 49,50; 0℃ <= TC <= 85℃

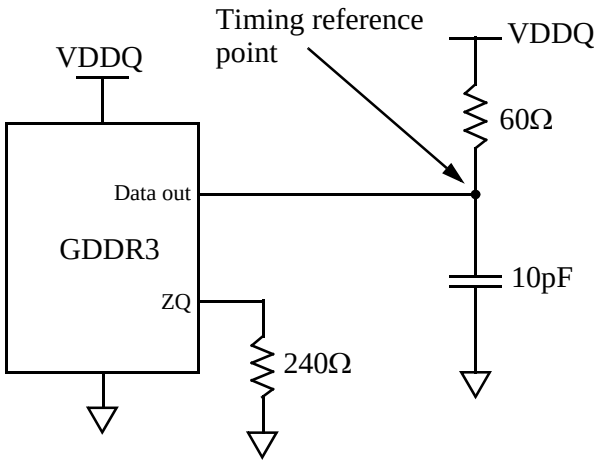
PARAMETER/CONDITION		SYMBOL	MAX					UNITS	NOTES
			-2	-16	-14	-12	-11		
OPERATING CURRENT: One bank; Active-Precharge; tRC (MIN); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle; WL=6		IDD0	350	400	450	500	550	mA	22, 46
OPERATING CURRENT: One bank; Active Read Pre-charge; Burst = 4; tRC (MIN); tCK = tCK (MIN); Address and control inputs changing once per clock cycle; I(OUT) =0mA; WL=6		IDD1	350	400	450	500	550	mA	22, 46
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; tCK = tCK (MIN); CKE= LOW		IDD2P	100	110	120	140	150	mA	32
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; tCK = tCK (MIN); CKE = HIGH; inputs changing once per clock cycle		IDD2N	180	200	230	270	290	mA	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; tCK = tCK (MIN); CKE= LOW; WL=6		IDD3P	100	110	140	160	170	mA	32
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank; Active Precharge; tRC = tRAS (MAX); tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle;WL=6		IDD3N	280	300	350	400	450	mA	22
OPERATING CURRENT: Burst = 4; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); I(OUT)=0mA; WL=6		IDD4R	700	850	950	1200	1300	mA	
OPERATING CURRENT: Burst = 4; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK = tCK (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; WL=6		IDD4W	700	850	950	1200	1300	mA	
AUTO REFRESH CURRENT	tRFC (MIN)	IDD5A	400	450	480	500	550	mA	22
	tRFC = 3.9us	IDD5B	270	280	290	310	320	mA	27
SELF REFRESH CURRENT: CKE <= 0.2V		IDD6	70	70	70	70	70	mA	11

Table 19: Electrical Characteristics and AC Operating Conditions

Notes: 1-5,14-16,33,40; notes on pages 49.50; 0℃ <= TC <=85℃

AC Characteristics Parameter			-2		-16		-14		-12		-11		Unit	Note
Parameter		Sym-bol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Access window of RDQS from CK/CK#		tAC	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	-0.25	+0.25	tCK	
CK High-level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30
CK Low-level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30
Clock Cycle Time	CL=11	tCK	-	-	-	-	-	-	-	-	1.1	3.3	ns	33, 40
	CL=10	tCK	-	-	-	-	-	-	1.25	3.3	-	-	ns	33, 40
	CL=9	tCK	-	-	-	-	1.4	3.3	-	-	-	-	ns	33, 40
	CL=8	tCK	-	-	1.6	3.3	-	-	-	-	-	-	ns	33, 40
	CL=7	tCK	2	3.3	-	-	-	-	-	-	-	-	ns	33, 40
Write Latency		tWL	1	4	1	4	1	5	1	5	1	5	tCK	43
DQ & DM input hold time relative to DQS		tDH	0.25		0.2		0.18		0.16		0.14		ns	26, 31
DQ & DM input setup time relative to DQS		tDS	0.25		0.2		0.18		0.16		0.14		ns	26, 31
Active termination setup time		tATS	10		10		10		10		10		ns	
Active termination hold time		tATH	10		10		10		10		10		ns	
Vendor ID & Revision code out timing from command		tWRID-ON	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC		
Vendor ID & Revision code out off timing from command		tWRID-OFF	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC	0ns	CL+ tAC		
DQS input high pulse width		tDQSH	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse width		tDQSL	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
DQS-DQ skew		tDQSQ	-0.20	0.20	-0.160	0.160	-0.125	0.125	-0.11	0.11	-0.09	0.09	ns	25, 26
Write command to first DQS latching transition		tDQSS	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	tCK	
DQS falling edge to CK rising . setup time		tDSS	0.25		0.25		0.25		0.25		0.25		tCK	
DQS falling edge from CK rising . hold time		tDSH	0.25		0.25		0.25		0.25		0.25		tCK	
Half strobe period		tHP	0.45		0.45		0.45		0.45		0.45		tCK	34
Data-out high-impedance window from CK/CK#		tHZ	-0.3		-0.3		-0.25		-0.25		-0.25		ns	18
Data-out low-impedance window fromCK/CK#		tLZ	-0.3		-0.3		-0.25		-0.25		-0.25		ns	18
Address and control input hold time		tIH	0.5		0.45		0.35		0.3		0.25		ns	14
Address and control input setup time		tIS	0.5		0.45		0.35		0.3		0.25		ns	14
Address and control input pulse width		tIPW	1.4		1.2		1.0		0.75		0.6		ns	
LOAD MODE REGISTER command cycle time		tMRD	4		4		4		4		4		tCK	44
Data valid output window		tDV	tHP - 0.5ns		tHP - 0.45ns		tHP - 0.38ns		tHP-0.32ns		tHP-0.28ns		ns	25, 26, 34
ACTIVE to PRECHARGE command		tRAS	38	120,000	38	120,000	30	120,000	30	120,000	30	120,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period		tRC	52.5		52.5		43.5		43.5		43.5		ns	
AUTO REFRESH command period		tRFC	83		83		56		56		56		ns	

AC Characteristics Parameter		-2		-16		-14		-12		-11		Unit	Note
Parameter	Sym-bol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
REFRESH to REFRESH command interval`	tREFC		35		35		35		35		35	us	23
Average periodic refresh interval	tREFI		3.9		3.9		3.9		3.9		3.9	us	23
ACTIVE to READ delay	tRCDR	15	-	15	-	15	-	15	-	15	-	ns	
ACTIVE to WRITE delay	tRCDW	12	-	12	-	10	-	10	-	10	-	ns	
PRECHARGE command period	tRP	16	-	16	-	13	-	13	-	13	-	ns	
DQS read preamble	tRPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	46
DQS read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to ACTIVE bank b command	tRRD	10	-	10	-	10	-	10	-	10	-	ns	
Exit Power-down	tPDIX	6 + tIS		6 + tIS		6 + tIS		6 + tIS		6 + tIS		tCK	
Exit Power-down on LP mode	tPDIXL	20K	-	20K	-	20K	-	20K	-	20K	-	tCK	
DQS write preamble	tWPRE	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS write preamble setup time	tWPRES	0	-	0	-	0	-	0	0.6	0	0.6	ns	20, 21
DQS write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	19, 37
Write recovery time	tWR	7	-	9	-	10	-	10	-	10	-	tCK	47
Internal WRITE to READ com-mand delay	tWTR	4	-	5	-	5	-	5	-	6	-	tCK	
Bank active restriction rolling window	tFAW	50	-	50	-	50	-	50	-	50	-	nS	45
Exit SELF REFRESH to non-READ command	tXSNR	66	-	66	-	66	-	66	-	66	-	tCK	
Exit SELF REFRESH to READ command	tXSRD	20K	-	20K	-	20K	-	20K	-	20K	-	tCK	
Cyclic jitter of Clock	tCJC	0.05		0.05		0.05		0.05		0.05		tCK	30



AC timing reference load (Refer to note3 on page49)

Notes:

1. All voltages referenced to Vss.
2. Tests for AC timing, Idd, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs measured with equivalent load of 10pf teminated with 60Ω to VddQ. The output timing reference voltage level for single ended signals is the cross point with VREF (=0.7*VDDQ nominal).
4. AC timing and Idd tests may use a Vil-to-Vih swing of up to 1.0V in the test environment, but input timing is still referenced to Vref (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 3V/ns in the range between Vil(AC) and Vih(AC).
5. The AC and DC input level specifications are a pseudo open drain design for improved high-speed signaling.
6. Vref is expected to equal 70 percent of VddQ for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on Vref may not exceed ± 2 percent of the DC value. Thus, from 70% of VddQ, Vref is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.
7. Needed to further definitions.
8. Vid is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of Vix is expected to equal 70 percent of VddQ for the transmitting device and must track variations in the DC level of the same.
10. Idd is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at minium CAS latency and does not include the on-die termination current. Outputs are open during Idd measurements.
11. Enables on-chip refresh and address counters.
12. Idd specifications are tested after the device is properly initialized.
13. This parameter is sampled. Vdd = 1.8V, VddQ = 1.8V, Vref = Vss, f = 1 MHz, TA =25℃, Vout(DC) = 0.75V, VddQ, Vout (peak to peak)= 0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
14. Command/Address input slew rate = 3 V/ns. If the slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the Vil(AC) maximum and Vih(AC) minimum points.
15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is Vref.
16. Inputs are not recognized as valid until Vref stabilizes. Exception: during the period before Vref stabilizes, MF, CKE <= 0.3 x VddQ is recognized as LOW.
17. Not used in this Specification.
18. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving(LZ).
19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance(bus turn-around) will degrade accordingly.
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that WDQS be valid (HIGH orLOW) on or before the WRITE command.
22. MIN (tRC or tRFC) for Idd measurements is the smallest multiple of tCK that meets the minimum absolute value for the respective parameter. tRASMAX for Idd measurements is the largest multiple of tCK that meets the maximum absolute value for tRAS.
23. The refresh period is 8K every 32ms. This equates to an average refresh rate of 3.9us.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. The valid data window is derived by achieving other specifications . tDQHP and tDQSQ. The data valid window derates in direct pro-portion to the strobe duty cycle and a practical data valid window can be derived. The strobe is allowed a maximum duty cycle variation of 48:52. Functionality is uncertain when operating beyond a 48:52 ratio.
26. Referenced to each output group: RDQS0 with DQ0.DQ7, RDQS1 with DQ8.DQ15, RDQS2 with DQ16.DQ23, and RDQS with DQ24.DQ31.

27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period (tRFC [MIN]) else CKE is LOW (e.g., during standby).
28. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge, and the driver should achieve the same slew rate through the AC values.
29. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
30. CK and CK# input slew rate must be >= 6 V/ns.
31. DQ and DM input slew rates must not deviate from WDQS by more than 10 percent. If the DQ/DM/WDQS slew rate is less than 3 V/ns, timing is no longer referenced to the midpoint but to the Vil(AC) maximum and Vih(AC) minimum points.
32. Vdd must not vary more than 4 percent if CKE is not active while any bank is active.
33. The clock is allowed up to ± 90ps of jitter. Each timing parameter is allowed to vary by the same amount.
34. tHP (MIN) is the lesser of tDQSL minimum and tDQSH minimum actually applied to the device CK and CK# inputs, collectively during bank active.
35. For READs and WRITEs with auto precharge the GDDR3 device will hold off the internal PRECHARGE command until tRAS (MIN) has been satisfied.
36. The last rising edge of WDQS after the write postamble must be driven high by the controller.WDQS cannot be pulled high by the on-die termination alone. For the read postamble the GDDR3 will drive the last rising edge of the read postamble.
37. The voltage levels used are derived from the referenced test load. In practice, the voltage levels obtained from a properly termi nated bus will provide significantly different voltage values.
38. Vih overshoot: Vih (MAX) = VddQ + 0.5V for apulse width <= 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. Vil under-shoot: Vil (MIN) = 0.0V for a pulse width <= 500ps and the pulse width cannot be greater than 1/3 ofthe cycle rate.
39. The DLL must be reset when changing the frequency, followed by 20K clock cycles.
40. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
41. The thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number. These parameters are not tested in production or jusr guarateed by the simulation methods.
42. The WRITE latency can be set from 1 to 6 clocks butcan never be less than 2ns for latencies of 1 and 3clocks. When the WRITE latency is set to 1 or 3 clocks,the input buffers are always on, reducing the latency but adding power. When the WRITE latency is set to 4 or 6 clocks the input buffers are turned on during the WRITE commands for lower power operation and can never be less than 7.5ns.
43. We'll try to cut these values for positive timing budget of 800MHz operations
44. Minimum of +9 cycles are needed to Read commands.
45. 8 Banks device sequential bank activation restriction: No more than 4 banks may be activated in a rolling tFAW window. tFAW= 4th Banks Act + 2*tRRD=(5*tRRD). Converting to clocks is done by dividing tFAW by tCK and rounding up to next integer.
46. In here, tRPRE means, Low drive period of RDQS prior to the valid high rising edge. It doesn't include the High drive period prior to Low drive.
47. WR_A (write recovery time for autoprecharge) in clock cycles is calculated by dividing tWR (in nS) and rounding up to the next integer (WR[cycles] = tWR(ns)/tCK(ns)). The mode register must be programmed to this value.

Table 20: Electrical Characteristics Usages as Clock phase

AC Characteristics Parameter		-2		-16		-14		-12		-11		Unit	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVE to PRECHARGE command	tRAS	20	100K	24	100K	22	100K	25	100K	28	100K	tCK	-
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	27	-	33	-	31	-	37	-	40	-	tCK	-
AUTO REFRESH command period	tRFC	42	-	52	-	40	-	47	-	51	-	tCK	-
ACTIVE to READ delay	tRCDR	8	-	10	-	11	-	13	-	14	-	tCK	-
ACTIVE to WRITE delay	tRCDW	6	-	8	-	8	-	9	-	10	-	tCK	-
PRECHARGE command period	tRP	8	-	10	-	10	-	11	-	12	-	tCK	-
ACTIVE bank a to ACTIVE bank b command	tRRD	6	-	7	-	8	-	9	-	10	-	tCK	-
Bank active restriction rolling window	tFAW	26	-	32	-	36	-	42	-	46	-	tCK	-
Write recovery time	tWR	7	-	9	-	10	-	10	-	10	-	tCK	-
Internal WRITE to READ command delay	tWTR	4	-	4	-	5	-	5	-	6	-	tCK	-
WRITE recovery time + PRECHARGE command period	tDAL	14	-	18	-	20	-	21	-	22	-	tCK	-
Exit SELF REFRESH to READ command	tXSRD	20K	-	20K	-	20K	-	20K	-	20K	-	tCK	-
Exit Power-down	tPDIX	6	-	6	-	6	-	6	-	6	-	tCK	-
REFRESH Interval	tREF	-	3.9	-	3.9	-	3.9	-	3.9	-	3.9	uS	-

I/O and ODT Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.8V (VDD/VDDQ)
2. Power the GDDR3 device and calibrate the output drivers and termination to eliminate process variation at 25℃.
3. Reduce temperature to 10℃ recalibrate.
4. Reduce temperature to 0℃ and take the fast corner measurement.
5. Raise temperature to 75℃ and recalibrate
6. Raise temperature to 85℃ and take the slow corner measurement

I/O Impedances

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN	MAX
0.1	2.144	3.366
0.2	4.268	6.516
0.3	6.373	9.454
0.4	8.449	12.185
0.5	10.505	14.715
0.6	12.542	17.051
0.7	14.540	19.400
0.8	16.509	21.828
0.9	18.449	24.219
1.0	20.341	26.580
1.1	22.203	28.913
1.2	24.017	31.222
1.3	25.783	33.508
1.4	27.480	35.813
1.5	29.119	38.213
1.6	30.671	40.551
1.7	31.387	42.900
1.8	31.648	45.176

Pull-Up Characteristic at 40ohms		
Voltage (V)	MIN	MAX
0.1	-2.377	-2.946
0.2	-4.705	-5.829
0.3	-6.984	-8.644
0.4	-9.283	-11.383
0.5	-11.524	-14.038
0.6	-13.803	-16.599
0.7	-16.015	-19.051
0.8	-18.285	-21.630
0.9	-20.302	-24.143
1.0	-22.223	-26.605
1.1	-24.066	-29.005
1.2	-25.773	-31.353
1.3	-27.344	-33.619
1.4	-28.683	-35.803
1.5	-29.731	-37.883
1.6	-30.691	-39.882
1.7	-31.544	-42.003
1.8	-32.311	-44.063

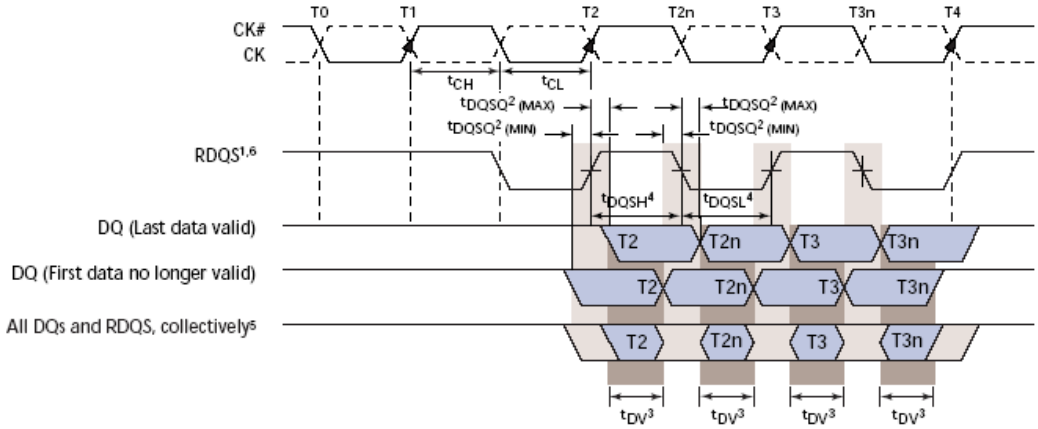
On Die Termination Values

Pull-Up Characteristic at 60ohms		
Voltage (V)	MIN	MAX
0.1	-1.58	-1.96
0.2	-3.14	-3.89
0.3	-4.66	-5.76
0.4	-6.19	-7.59
0.5	-7.68	-9.36
0.6	-9.20	-11.07
0.7	-10.68	-12.70
0.8	-12.19	-14.42
0.9	-13.53	-16.10
1.0	-14.82	-17.74
1.1	-16.04	-19.34
1.2	-17.18	-20.90
1.3	-18.23	-22.41
1.4	-19.12	-23.87
1.5	-19.82	-25.26
1.6	-20.46	-26.59
1.7	-21.03	-28.00
1.8	-21.54	-29.38

Pull-Up Characteristic at 120ohms		
Voltage (V)	MIN	MAX
0.1	-0.79	-0.98
0.2	-1.57	-1.94
0.3	-2.33	-2.88
0.4	-3.09	-3.79
0.5	-3.84	-4.68
0.6	-4.60	-5.53
0.7	-5.34	-6.35
0.8	-6.09	-7.21
0.9	-6.77	-8.05
1.0	-7.41	-8.87
1.1	-8.02	-9.67
1.2	-8.59	-10.45
1.3	-9.11	-11.21
1.4	-9.56	-11.93
1.5	-9.91	-12.63
1.6	-10.23	-13.29
1.7	-10.51	-14.00
1.8	-10.77	-14.69

Pull-Up Characteristic at 240ohms		
Voltage (V)	MIN	MAX
0.1	-0.40	-0.49
0.2	-0.78	-0.97
0.3	-1.16	-1.44
0.4	-1.55	-1.90
0.5	-1.92	-2.34
0.6	-2.30	-2.77
0.7	-2.67	-3.18
0.8	-3.05	-3.60
0.9	-3.38	-4.02
1.0	-3.70	-4.43
1.1	-4.01	-4.83
1.2	-4.30	-5.23
1.3	-4.56	-5.60
1.4	-4.78	-5.97
1.5	-4.96	-6.31
1.6	-5.12	-6.65
1.7	-5.26	-7.00
1.8	-5.39	-7.34

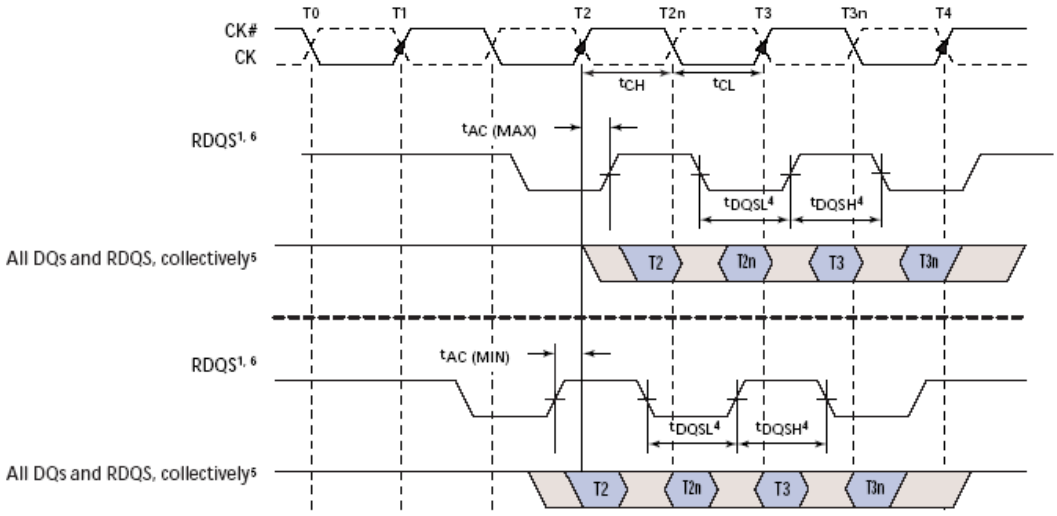
Figure 29: Data Output Timing - tDQSQ, tQH and Data Valid Window



NOTE:

1. tDQSQ represents the skew between the eight DQ lines and the respective RDQS pin.
2. tDQSQ is derived at each RDQS edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQ.
3. tAC is shown in the nominal case.
4. tDQHP is the lesser of tDQSL or tDQSH strobe transition collectively when a bank is active.
5. The data valid window is derived for each RDQS transitions and is defined by tDV.
6. There are four RDQS pins for this device with RDQS0 in relation to DQ(0.7), RDQS1 in relation DQ(8.15), RDQS2 in relation to DQ(16.24), and RDQS3 in relation to DQ(25.31).
7. This diagram only represents one of the four byte lanes.

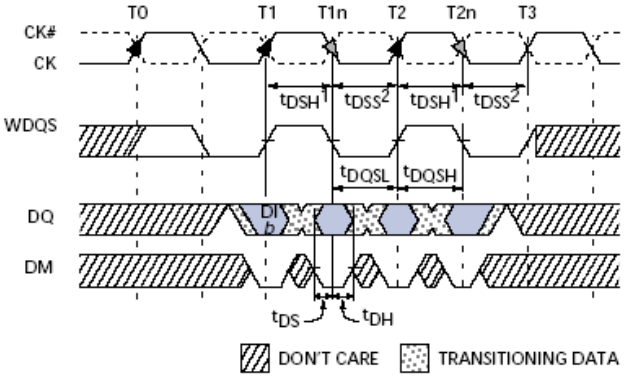
Figure 30: Data Output Timing - AC



NOTE:

1. tAC represents the relationship between DQ, RDQS to the crossing of CK and CK#.

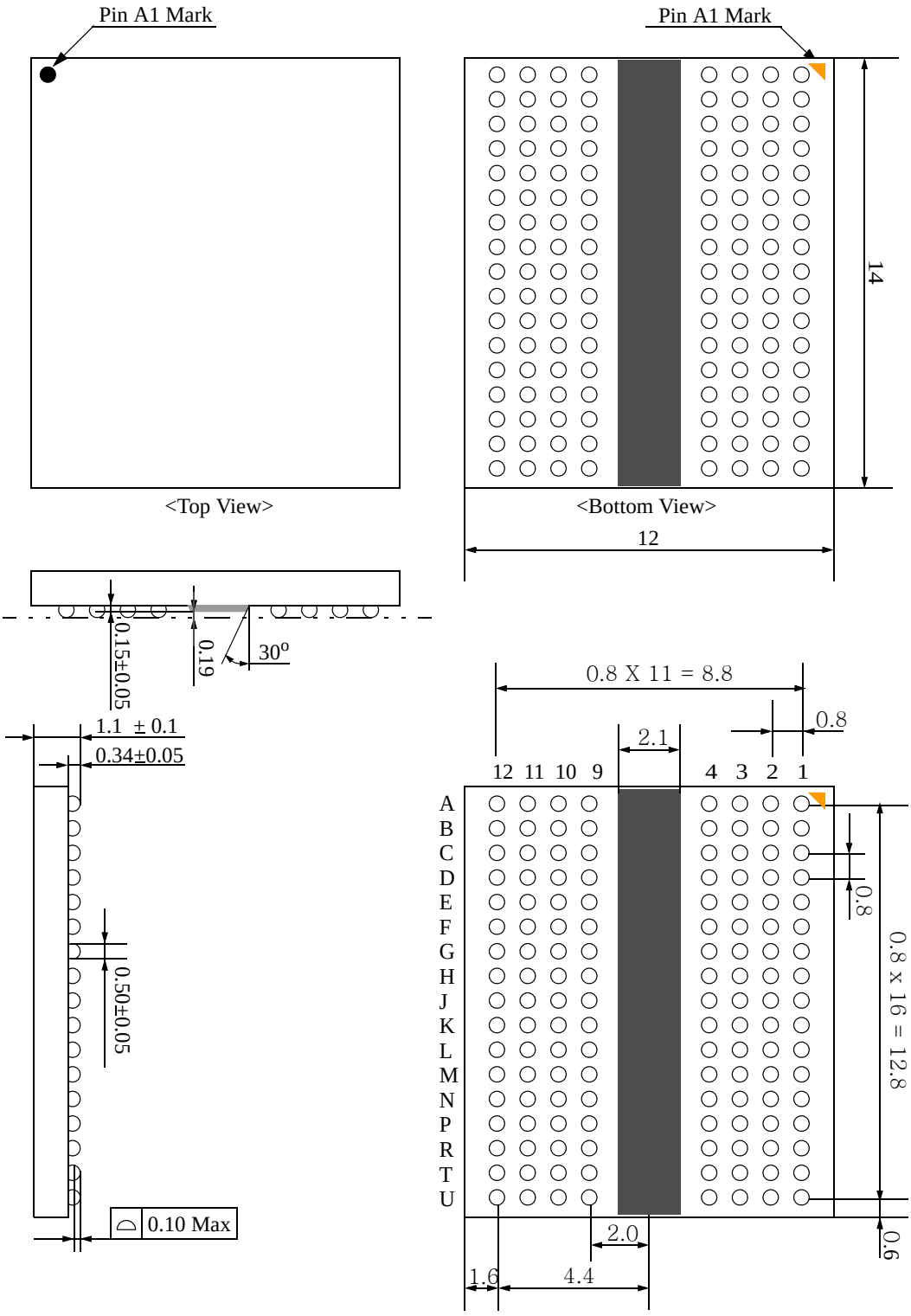
Figure 31: Data Input Timing



NOTE:

1. tDSH (MIN) generally occurs during tDQSS (MIN).
2. tDSS (MIN) generally occurs during tDQSS (MAX).

Package Information



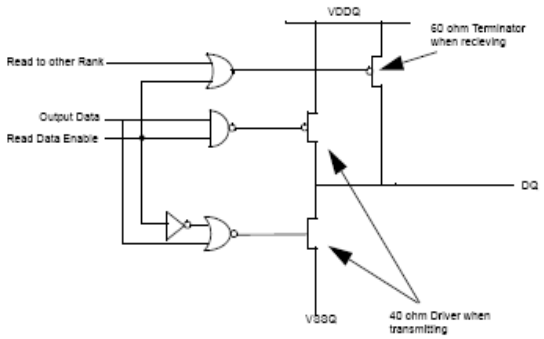
Note) HY5RS123235FP-xx is the Lead Free Package part number

Unit:mm

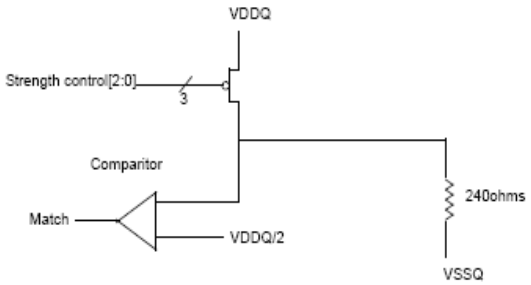
Appendix A

The following diagram shows the general GDDR3 driver and terminator

Output Driver



Self Calibration of Pmos Leg

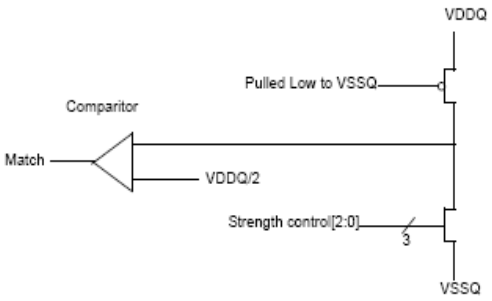


When Match Pmos leg is calibrated to 240 ohms

Self Calibration flow for Driver and Terminator

- First calibrate Pmos device against 240ohm resister to VSS via ZQ pin
  - This calibrates one Pmos leg to 240 ohms
    - Use 1 Pmos leg for 240 ohm terminator
    - Use 2 Pmos legs for 120 ohm teminator
    - Use 4 Pmos legs for 60 ohm terminator
    - Use 6 Pmos legs for 40 ohm pullup driver
- Next calibrate one Nmos leg against the already calibrated 240 ohm Pmos leg
  - This calibrates one Nmos leg to 240 ohms
  - Use 6 Nmos legs for 40 ohm driver

Self Calibration of Nmos Leg



When Match Nmos leg is calibrated to 240 ohms

Apendix B Definition of Terminology

Hereafter are defined terminologies used in the GDDR3 SGRAM specification.

Although GDDR3 might be operated in ODT Disable Mode, it is not recommended and the specification describes the ODT Enable Mode only. Should a system be designed to operate the GDDR3 in ODT Disable Mode, the system should comprehend the effect of the discrepancies between this specification and its own design.

If it is stated that a bus is in one of the following state, it should be interpreted as described.

Following are three terminologies defined for ODT Enable Mode.

- High{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.
- Hi-z{terminated}: No driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VDDQ.
- Low{terminated}: A driver on the bus is driving the bus. One or more termination (ODT) on the bus is turned-on. The voltage level of the bus would be nominally VOL(DC).

Corresponding terminologies for ODT Disable Mode are defined below.

As mentioned before, ODT Disable Mode is not an intended mode of operation. However, there exist situations where ODT Enable Mode can not be guaranteed for a short period of time, like during power up, yet is indeed an intended mode of operation.

- High{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VDDQ.
- Hi-z{unterminated}: No driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be undefined, because the bus would be floating.
- Low{unterminated}: A driver on the bus is driving the bus. No termination on the bus is active. The voltage level of the bus would be nominally VSSQ.

APPENDIX C Boundary Scan Test Mode

General Information

The 512Mb GDDR3 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.11990. To save the current GDDR3 ballout, this mode will scan the parallel data input and output the scanned data through WDQS0 pin controlled by an addon pin, SEN which is located at V4 of 136 ball package.

Disabling the Scan feature

It is possible to operate the 512Mb GDDR3 without using the boundary scan feature. SEN(at V4 of 136ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RES, MF, WDQS0 and CS# will be operating at normal GDDR3 functionalities when SEN is deasserted.

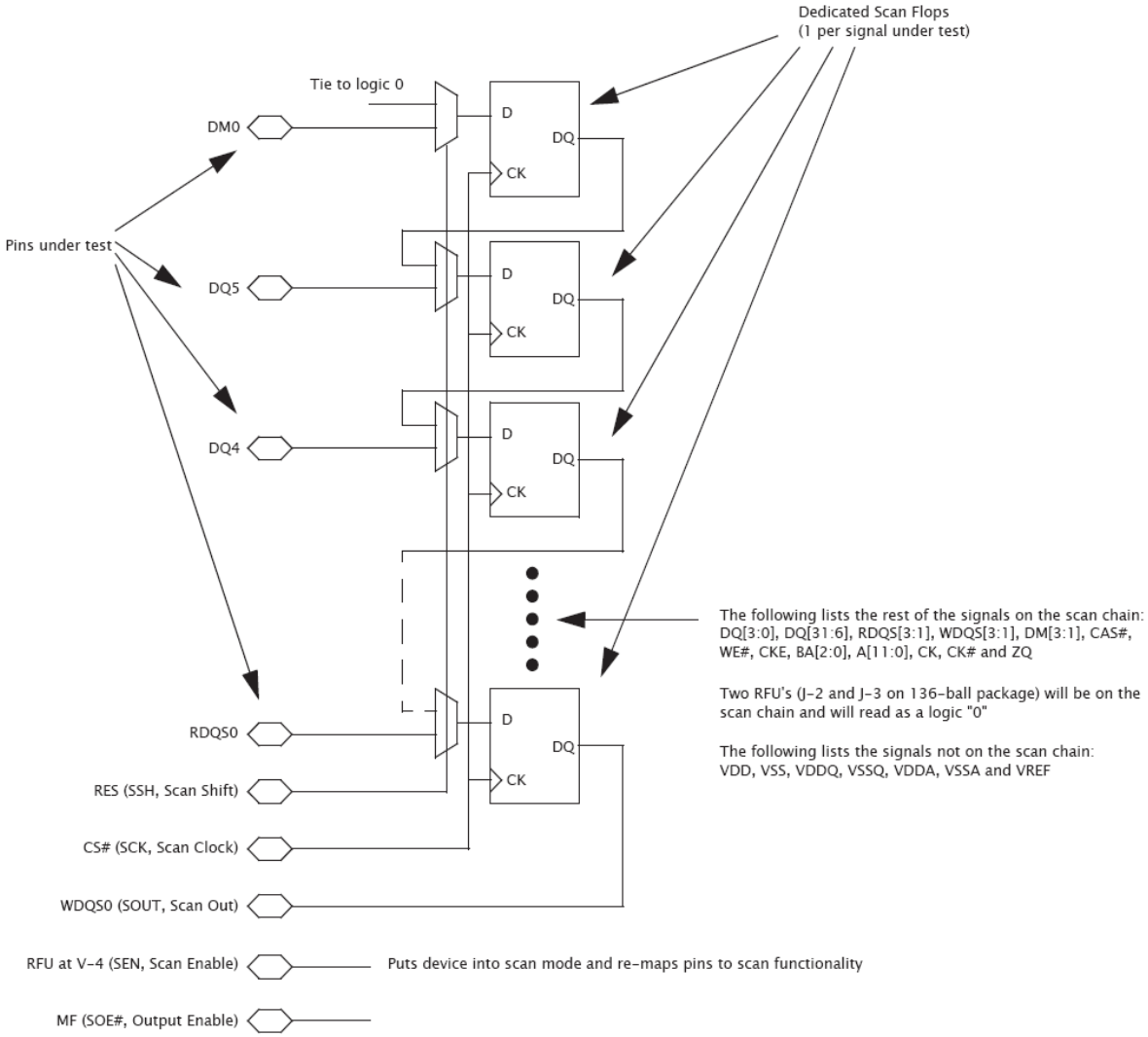


Figure C-1: Internal Block Diagram(Reference Only)

Table C-1: Boundary Scan (Exit) Order

BIT#	BALL	PIN	BIT#	BALL	PIN	BIT#	BALL	PIN	BIT#	BALL	PIN
1	D-3	RDQ0	18	G-9	BA1	35	P-10	RDQS2	52	K4	A0
2	C-2	DQ2	19	H-9	WE#	36	R-11	DQ20	53	K-3	A2
3	C-3	DQ3	20	H-10	BA2	37	R-10	DQ21	54	K-2	A10
4	B-2	DQ0	21	H-11	A5	38	T-11	DQ22	55	L-4	A11
5	B-3	DQ1	22	J-11	CK	39	T-10	DQ23	56	J-3	RFU2
6	A-4	ZQ	23	J-10	CK#	40	T-3	DQ31	57	J-2	RFU1
7	B-10	DQ9	24	L-9	A7	41	T-2	DQ30	58	H-2	A1
8	B-11	DQ8	25	K-11	A8	42	R-3	DQ29	59	H-3	RAS#
9	C-10	DQ11	26	K-10	A6	43	R-2	DQ28	60	H-4	CKE
10	C-11	DQ10	27	K-9	A4	44	P-3	RDQS3	61	G-4	BA0
11	D-10	RDQ1	28	M-9	A9	45	P-2	WDQS3	62	F-4	CAS#
12	D-11	WDQS1	29	M-11	DQ16	46	N-3	DM3	63	F-2	DQ6
13	E-10	DM1	30	L-10	DQ17	47	M-3	DQ27	64	G-3	DQ7
14	F-10	DQ13	31	N-11	DQ18	48	N-2	DQ26	65	E-2	DQ4
15	E-11	DQ12	32	M-10	DQ19	49	L-3	DQ25	66	F-3	DQ5
16	G-10	DQ15	33	N-10	DM2	50	M-2	DQ24	67	E-3	DM0
17	F-11	DQ14	34	P-11	WDQS2	51	M-4	A3			

Note:

1. When the device is in scan mode, the mirror function will be disabled and none of the pins are remapped.
2. Since the other input of the MUX for DM0 tied to GND, the device will output the continuous zeros after scanning a bit #67, if the chip stays in scan shift mode.
3. Two RFU balls (#56 and #57) in the scan order, will read as a logic“0”.

Table C-2: Scan Pin Descriptions

BALL	SYMBOL	Normal Funtion	Type	Descriptions
U-9	SSH	RES	Input	Scan Shift. Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	CS#	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock.
D-2	SOUT	WDQS0	Output	Scan Output.
U-4	SEN	RFU	Input	Scan Enable. Logic HIGH would enable the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	SOE#	MF	Input	Scan Output Enable. Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1K) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

Note:

1. When SEN is asserted, no commands are to be executed by the GDDR3. This applies both to user commands and manufacturing commands which may exist while RES is deasserted.
2. All scan functionalities are valid only after the appropriate power-up and initialization sequence. (RES and CKE, to set the ODT of the C/A)
3. In scan mode, the ODT for the address and control lines set to a nominal termination value of ZQ. The ODT for DQ's will be disabled. It is not necessary for the termination to be calibrated. It means, user should program the EMRS for ODT disable mode (EMRS termination code, A<3:2>=0)
4. During the power-up and initialization sequence, ZQ pin should be maintained the connection to VSSQ through proper RQ.
5. In a double-load clam-shell configuration, SEN will be asserted to both devices. Separate two SOE#'s should be provided to top and bottom devices to access the scanned output. When either of the devices is in scan mode, SOE# for the other device which is not in a scan will be disabled.

Table C-3: Scna DC Electrical Characteristics and Operating Conditions

Parameter/Conditionss	Symbol	MIN	MAX	Units
Input High(Logic 1) Voltage	VIH(DC)	VREF+0.15	-	V
Input Low(Logic 0) Voltage	VIL(DC)	-	VREF-0.15	V

Note:

1. The parameter applies only when SEN is asserted.

2. All voltages referenced to GND.

Figure C-2: Scan Capture Timing

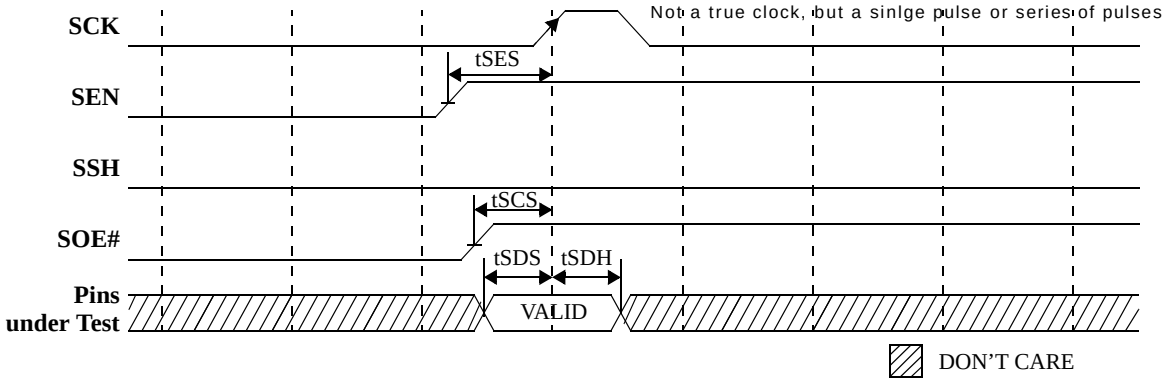


Figure C-3: Scan Shift Timing

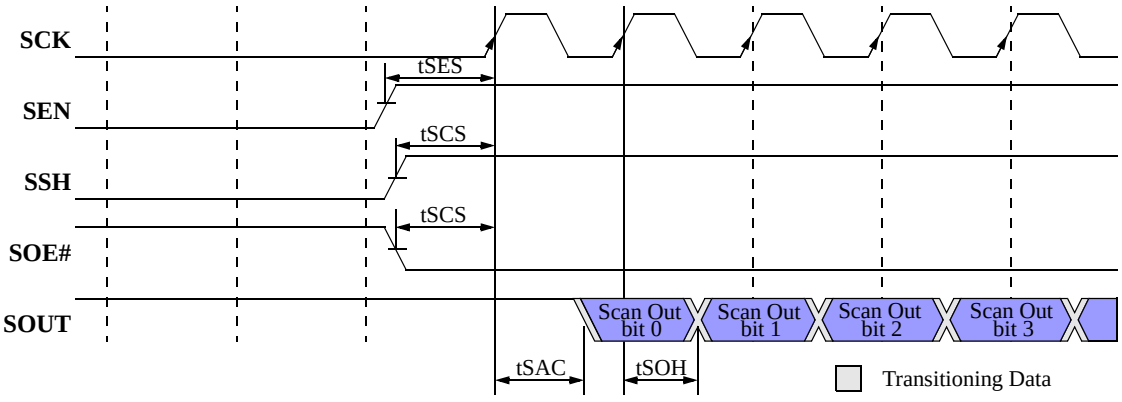
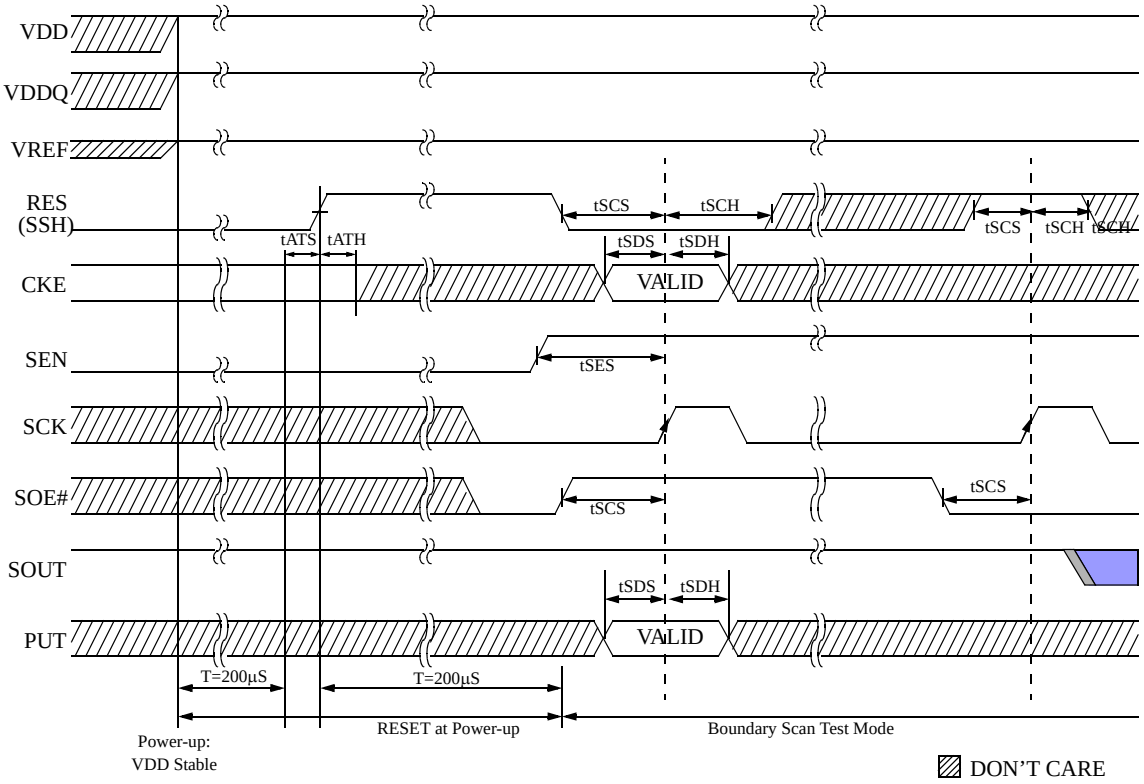


Table C-1: Scan AC Electrical Charateristics

Parameters/Conditions	SYMBOL	MIN	MAX	UNITS	NOTE
Clock					
Clock Cycle time	tSCK	40	-	nS	
Scan Command Time					
Scan enable setup time	tSES	20	-	nS	1,2
Scan enable hold time	tSEH	20	-	nS	
Scan command setup time for SSH, SOE# and SOUT	tSCS	14	-	nS	
Scan command hold time for SSH, SOE# and SOUT	tSCH	14	-	nS	
Scan Capture Time					
Scan capture setup time	tSDS	10	-	nS	
Scan capture hold time	tSDH	10	-	nS	
Scan Shift Time					
Scan clock to valid scan output	tSAC	-	6	nS	
Scan clock to scan output hold	tSOH	1.5	-	nS	

Note:
1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other Scan Commands by 10nS.

Figure C-4: Scan Initialization Sequence



Note:

To set the pre-defined ODT for C/A, a boundary scan mode should be issued after an appropriate ODT initialization sequence with RES and CKE signals