TLE6280GP -
A bridge driver IC for high current 3 phase motor drives in 12 and 24V power nets

by Benno Köppl

Automotive Power

Infineon
technologies

N e v e r   s t o p   t h i n k i n g .

1. Abstract

This Application Note is intended to provide additional information to the datasheet. It contains information to frequently asked topics such as start up sequence, function of the charge pump, dI/dt control etc.
It is not intended to replace the datasheet by this application note. Main target is to simplify the first putting into service of the 3 Phase bridge and optimize the operation of the bridge in an early stage of the design.

2. Introduction

Some years ago it was nearly impossible to find 3-phase electro-motors in automotive applications. In the meantime new powerful applications such as electric power steering have entered the cars. In addition applications originally driven by a big DC brush motor show the tendency to be replaced by 3 phase motors which their higher durability due to their brushless design. An example is here the cooling fan of the engine.
Another trend supporting the tendency to 3 phase motors is the wish of the car manufacturers to remove belt driven designs such as water pumps. The supply in automotive applications is an DC power net requiring a converter to drive 3 phase motors.

The TLE6280GP is an IC designed to drive the 3 highside and 3 lowside switches of such a converter. The main features of the TLE6280GP are:

1) The powerful output stages, able to drive 4mOhm 40V Mosfets with a switching time of about 300µs, allow the usage in applications up to 200A. (usage of 12 Mosfets)
2) The integrated short circuit protection for the external Mosfets by Drain-Source voltage monitoring with adjustable short circuit detection level, fulfils the requirements for protection in safety critical applications. Especially together with the adjustable current limitation in case of short circuit detection by Gate voltage limitation of the Mosfet
3) The adjustable on chip dead time generation avoids on one hand crosscurrent within a half-bridges and reduces on the other hand the power dissipation caused by the body diodes in passive freewheeling to a minimum. Together with the shoot through

protection. A safe operation of a B6 bridge is guarantied.
4) The flexible input structure combined with a minimum dead time of about 100ns makes a absolute free control of the 6 switches possible.
5) Its bootstrap design allows to switch even the high-side Mosfets with 30kHz and makes it attractive for various motor control strategies such as field orientated, sinusoidal control or even block commutation.
6) The integrated charge pump allows to reach even 10V Gate voltage when the supply voltage is below 9V and assures that the RDSon of the external Mosfets is not increased causing extra power dissipation.
7) Diagnosis output for reporting:
   a) short-circuiting of external bridge
   b) driver overheating
   c) driver output undervoltage in the event of defective external bootstrap capacitors or supply power shortfall
8) The highly innovative dI/dt control allows to reduce electro-magnetic emission by slowing down the switching process of the external Mosfets in the EME critical area without a significant increasing of switching losses.
9) Special driver design, such as separate source terminals for each lowside MOSFET, to ensure immunity to external interference.
10) The P-DSO-36-10 (Power-SO36) package with its Rth junction-heatsink of less then 5K/W together with the Tj max of 150°C allows the usage of the TLE6280GP up to ambient temperatures of 135°C and ensures that even 12 Mosfets can be driven by this device.

All together this driver IC is a highly integrated solution of high current 3 phase AC drives. It provides high output power, various protection functions, diagnosis and automotive specific functions to fulfil all requirements of a safety critical automotive application .

3. Application

Out of the applications mentioned before, electric power steering will be selected here to describe the specific requirements of a high current 3 phase drive. This was the target application the TLE6280GP was designed to.

Over the past few years the automobile sector has established power steering as part of the standard equipment in vehicles down to the subcompact car class. Classical power steering is based on a hydraulic system whose mechanical components need to be adapted to each vehicle type. The hydraulic oil it contains is harmful to the environment and has to be filled in during vehicle assembly. Electrical solutions for power steering were only offered for small vehicles, primarily as an aid to gap parking, but failed to attain the convenience and performance of hydraulic systems. There was a discernible trend in the market as early as 1998 for full-blown EPS (**E**lectric **P**ower **S**teering) systems to be extended to midrange vehicles in the car's 12V electrical distribution system. This type of system basically consists of a 3-phase AC motor with a rating of around 1 to 1.5 kW to drive the power steering, torque sensors on the steering column to register steering forces, a microprocessor to control the power circuitry, and an inverter supplying the engine with power from the 12V DC electrical distribution system. A major challenge to implementing a system of this type is the precise regulation of the engine torque in order, on the one hand, to ensure smooth steering support and, on the other, to preclude any perceptible jolting on the steering wheel. This entails controlling the motor current of up to 130A rms with the aid of the inverter, consisting of 6 MOS switches and a bridge driver. This application offers a power range previously unheard-of in the automobile industry, which has mostly made use of DC electric motors up to 80A in the past.
The major advantages of this type of system lie in reducing fuel consumption by up to 0.3 ltr/100 km, the modest package space requirements compared to hydraulic systems, and simple adaptation to different vehicle types through software modification.
Nor must we forget the saving in environmentally harmful hydraulic oil and the approximately 80% reduction in installation time during final vehicle assembly.
These advantages make electric power

steering a very attractive solution.
Essential parts of this application have to be newly developed. In the area of semiconductor components these are the power Mosfets, which must be able to accept up to 130A per package, and in particular the bridge driver ICs. This application places the following requirements on the bridge:

1. Switching of up to 180A peak in 300ns at 25kHz
2. Full driver output voltage even when battery voltage is low
3. Bridge short-circuit protection
4. Possibility of diagnosis
5. Compliance with EMC regulations
6. Immunity to electromagnetic radiation.
7. Immunity to over- and under voltages due to the fast switching of high currents.

The number of drivers ICs on the market able to drive such a bridge and fulfilling all these requirements is very limited. The Automotive Power Division of Infineon therefore decided to start developing the TLE6280GP so it could offer all power semiconductor products for this important application.
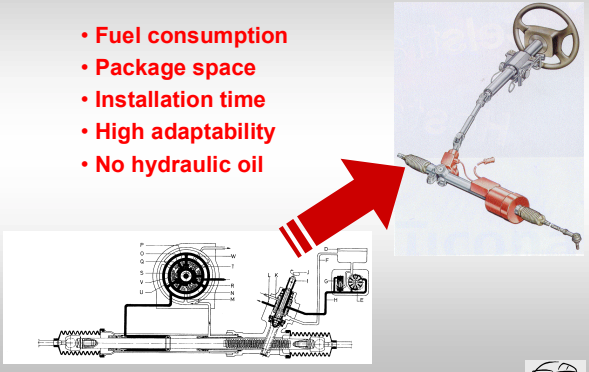With its features decribed in chapter 2 the TLE6280GP is covering all requirements of such an application.
Its unique combination of features make it the perfect solution for a high current B6 bridge in the 12 and 24V sector not only for electric power steering but for electro-hydraulic power steering, engine cooling fans, water pumps, elctric break systems as well.

System Advantages
Electric Power Steering vs. Hydraulic Systems

• **Fuel consumption**
• **Package space**
• **Installation time**
• **High adaptability**
• **No hydraulic oil**

Innovation
Award 99
AI AP SB

Fig. 1: System advantages

4. Product description

This chapter describes the individual functions of the driver and provides information about dimensioning of the external components and design of the power unit.
Figure 1 shows the block diagram of the driver.

4.1. Feature list

The feature list of the TLE6280GP is:
- Compatible to very low ohmic normal level N-Channel Mosfets
- Separate input for each Mosfets
- PWM frequency up to 30kHz
- Fulfils specification down to 9V supply voltage
- Low EMC sensitivity and emission
- Separate Source connection for each MOSFET
- Adjustable dead time
- Adjustable dI/dt limitation
- Short circuit protection with adjustable current limitation
- Driver undervoltage warning
- Reverse polarity protection
- Disable function
- Input with TTL characteristics

- Error flag
- Thermal overload warning for driver IC
- Shoot through protection

- Shoot through option
- Integrated bootstrap diodes

As this application not is not a replacement of the datasheet, not all of the features will be described here. The focus here will be to cover the most frequently asked questions about the functionality and the usage of the TLE6280GP.
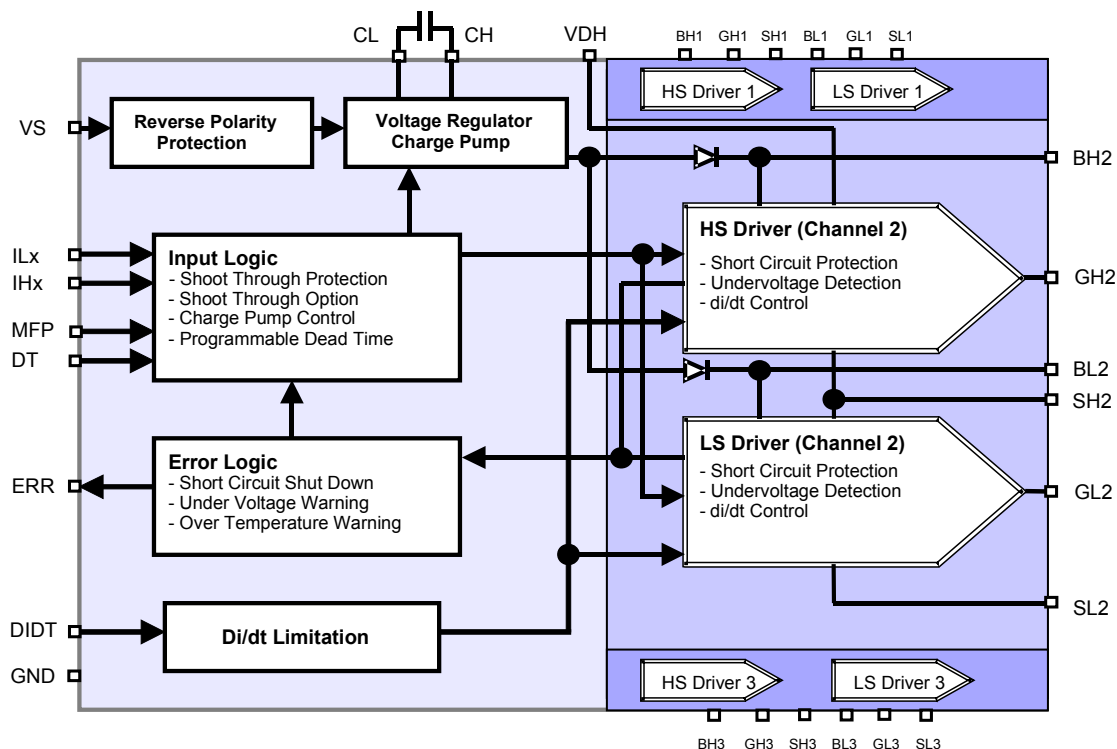

Fig. 1: Block diagram

4.2. The Output Stages

Figure 1 shows the block diagram of the driver IC with the 6 output stages.

In general all 6 output stages are designed in the same way. This means that not only the highside output stage is allowed to float, but the lowside output stages as well (max ratings SLx Pin is –7…7V – see datasheet). Together with the separated Source connections for each lowside Mosfet this assures a stable control of the external Mosfets by reducing the common path of the load current and the gate control to a minimum, minimizing the influence of stray inductivities and ohmic resistors to the Gate-Source voltage. This guaranties a stable bridge control even in high current applications like electric power steering. See fig. 2.

The output stages are strong enough to drive 12 4mOhm 40V Mosfets with rise and fall times far below 500ns. See fig. 3.
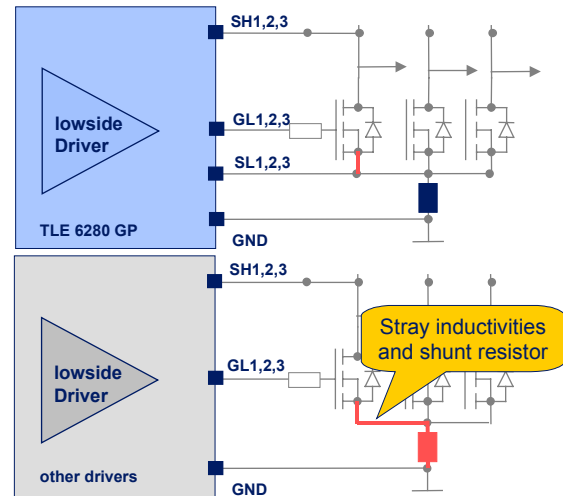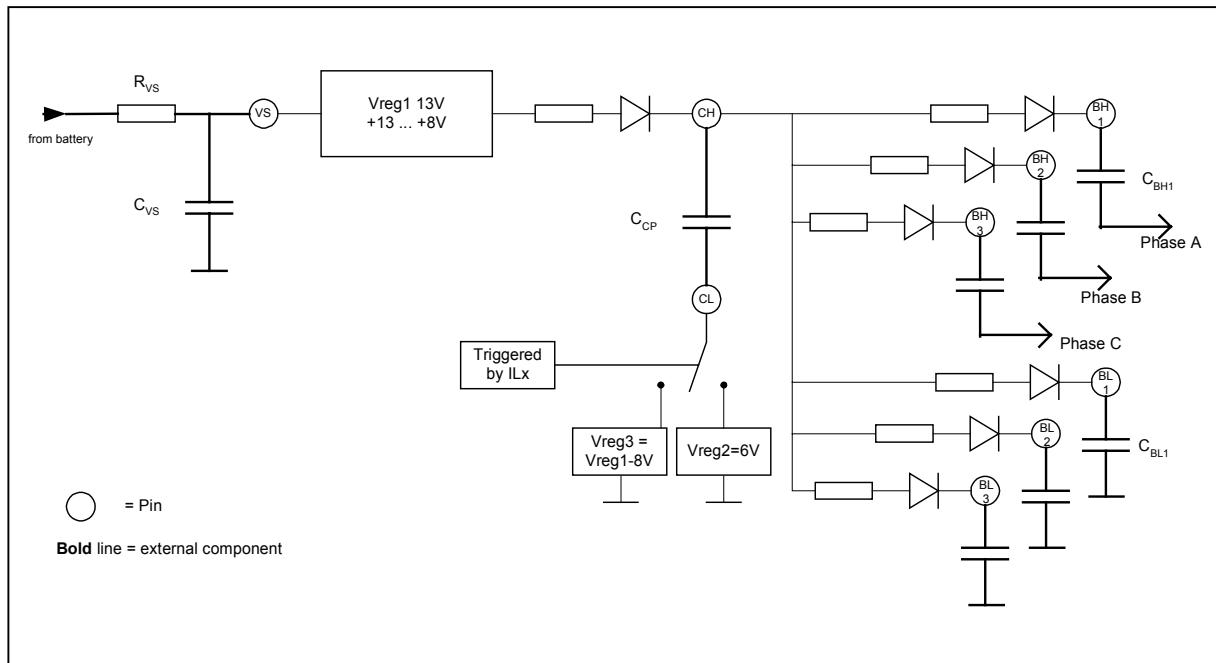

Fig. 2 : Dramatic reduction of common path of gate control and load circuit

Conditions:
VS=12V
MFP=3,75V
RG=1ohm
Switches: 12xSPB 80N04S2-04
I Load = 10A
25°C
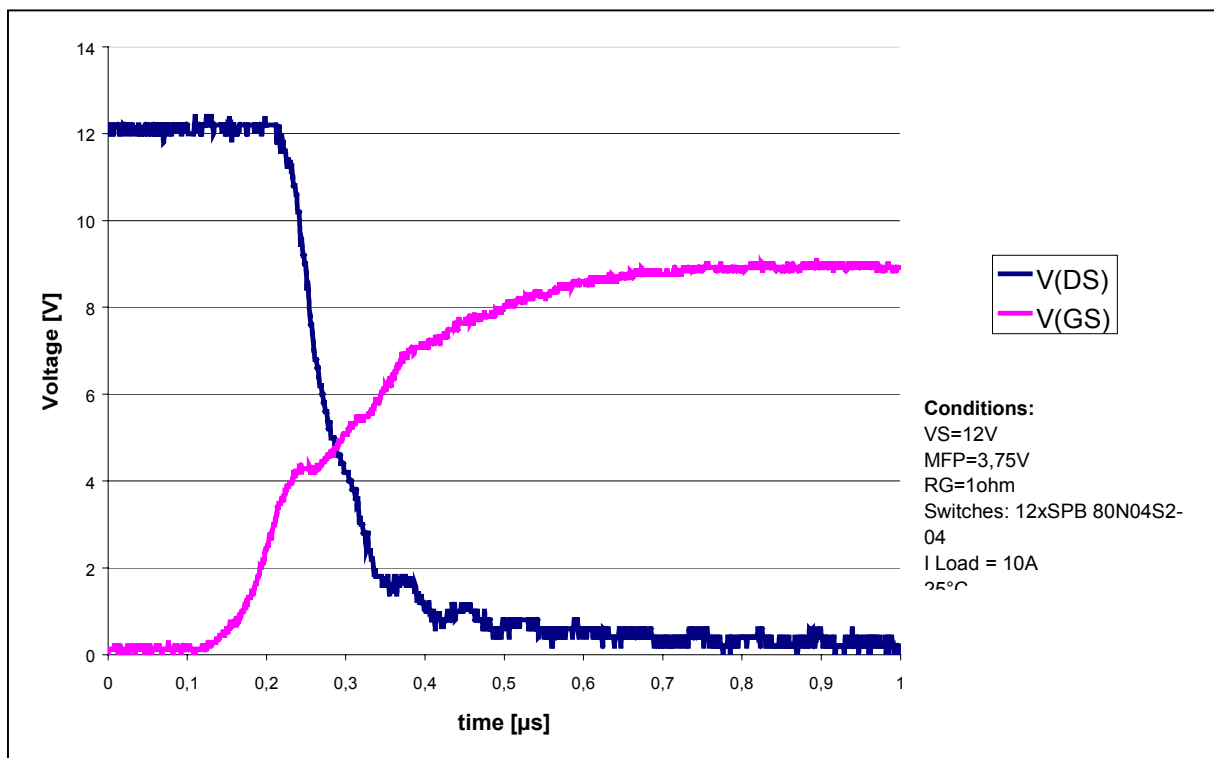
Fig. 3: Rise time of about 250 ns with 10A Load and 2 x 4mOhm Mosfets per switch. Rise time measured at V(DS)

Fig. 4: Supply structure of TLE 6280 GP

4.3. The Supply Concept of TLE6280GP and the Bootstrap Capacitors

Figure 4 shows the components involved in the driver's power supply system.
The supply chain can be separated in 3 parts.
1) The RC-element between battery and supply pin VS of the IC works as filter and guaranties a stable supply voltage.
2) The next link in the chain is formed by the internal voltage regulator Vreg1 and a charge pump formed by an integrated diode, the external pump capacitor C_{CP} and 2 integrated voltage regulators Vreg2 and 3.
The voltage regulator Vreg1 guaranties that the internal supply voltage is not higher than 13V. Of course the output voltage of this voltage regulator is reduced if the voltage at Vs is lower than 13V. To reach the full output voltage of 10V at the Gxx pins even at low supply voltages, the above mentioned charge pump pumps the voltage at the CH pin back to 13V . This is achieved by the 2 voltage regulators Vreg2 and 3. C_{CP} serves as a pump capacitor.
3) The third part of the supply chain starts at the CH pin and is formed by a diode and the external bootstrap and backup capacitor C_{Bxx}. C_{Bxx} is directly charged via this diode from CH pin.
The C_{BLx} capacitors work as supply for the lowside output stages and can be considered as output capacitor of the charge pump. Normally each driver stage for a low-side switch has its own capacitor C_{BLx}. This assures a stable supply of the output even if transient voltages at the SLx pin cause this output stage to float to voltages different to GND.
In general it is allowed to tie all BLx pins together and to use only one capacitor as CBLx, connected to GND. In this case the ability of the lowside output stage to float is limited. The maximum rating of the SLx pins I reduced in this case from −7…+7V to −1…+7V.

The C_{BHx} capacitors are the bootstrap capacitors of the driver IC, forming the supply for the highside output stages.
The bootstrap principle for controlling n-channel Mosfets as high-side switches is a low-cost standard solution for fast switching applications in comparison with an otherwise necessary, permanently operating charge pump or use of p-channel Mosfets.
The bootstrap principle allows a large duty cycle range to be implemented when the capacitors are correctly dimensioned. In this way an active free-wheeling can also be realized in the high-side switches which considerably reduces the resultant power loss in the case of free-wheeling.
The bootstrap capacitors are supplied directly from the CH pin via a integrated bootstrap diode.

The bootstrap principle works like follows:
The C_{BHx} capacitors are connected to the output of the power bridge (=SHx Pin). To charge the capacitor C_{BHx} from CH pin the lowside Mosfets in the bridge has to be switched on forcing SHx to GND or the motor current is flowing in forward direction over the body diode of the lowside Mosfet forcing SHx even below GND. The characteristic time to charge this capacitor is the RC time formed by the internal diode and the C_{BHx}, given in the datasheet.
As soon as the lowside Mosfet is switched of and the highside Mosfet is switched on, the SHx pin is forced to the supply voltage of the bridge, pushing the BHx pin to the supply voltage plus the voltage of the C_{BHx}, guaranteeing the supply of the output stage and the gate of the highside Mosfet. In this position it is impossible to recharge the C_{BHx} from CH.
By switching on the highside Mosfet, the total gate charge is taken out of C_{BHx}, reducing the voltage of this capacitor.
Therefore the size of the C_{Bxx} used, depends on the gate charge $Q_{G(10V)}$ of the external Mosfet at 10V V_{GS}. Too small a dimensioning leads to high voltage interruptions on the capacitors when the Mosfet is switched on and thus to lower gate voltages. Too large capacitors need a long pumping time during commissioning of the driver.
The following equation can be used as a guide:

$$(1) \qquad \Delta U_{Bxx} = \frac{n * Q_{G(10V)}}{C_{Bxx}} \le 0.5V$$

with

ΔU_{Bxx} change in the voltage at the C_{Bxx} capacitor during switching on

n equals the number of parallel connected Mosfets (usually 1 or 2)

$Q_{G(10V)}$ equals gate charge of the used Mosfet at V_{GS}=10V

The dimensioning of the C_{Bxx} capacitors according to equation 1 guarantees a uniformly high output voltage on the driver and therefore the R_{DSon} of the connected Mosfet.

Keeping on the highside Mosfet for a long time, means that the quiescent current of the output stage has to be considered. This current is taken out of the C_{BHx} as well, reducing again the voltage at C_{BHx}.
This means that the voltage of C_{BHx} is reduced over the time, when the highside Mosfet is on. As soon as the voltage of that capacitor reaches about 9V, a undervoltage warning is given by the status pin of the driver.
If the voltage reaches the undervoltage lock out level - given in the datasheet - the output stage will actively switch of the external Mosfet. This condition has to be avoided, as it would disturb the intended PWM pattern.
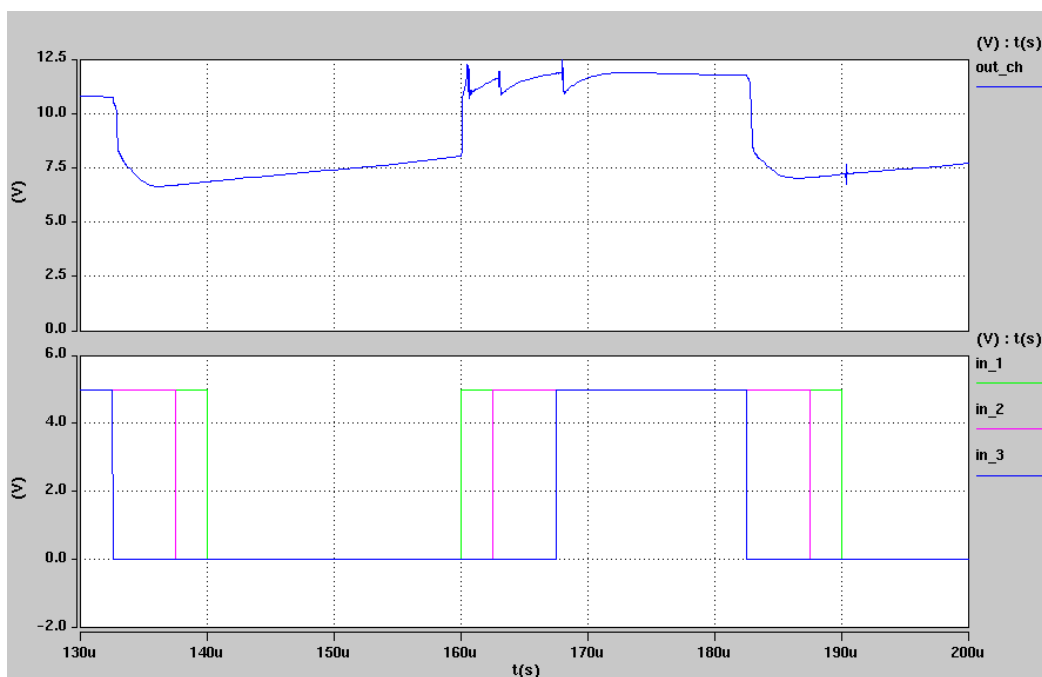The quiescent current is given in the datasheet.

Fig. 5: Pump behavior of the charge pump

The charge pump pumps every time any low-side switch is switched on for the first time per PWM cycle. Figure 3 illustrates this using the usual PWM pattern as an example. Another example is shown in the datasheet
The pump capacitor C_{CP} of the charge pump should be about 6 times larger than a C_{Bxx} capacitor.
The supply voltage at the V_s pin should be smoothed through a low pass. About 10Ω are recommended for R_s and about 1µF for C_s. When using 10Ω for R_s reverse polarity protection is guaranteed up to –4V.

Advantages and limits
This supply concept provides 10V gate voltage at the Mosfet over a wide duty cycle range even with Vs<8V. The EM emission, generated by the charge pump has the same spectrum as the bower bridge and needs no extra filters.

This concept has two limitations:
1) As the driver is based on the bootstrap principle , the C_{BHx} capacitors have to me refreshed from time to time and the refresh pulse has to be long enough to recharge C_{BHx}. If the TLE6280GP is used in a motor drive based on block commutation, when the highside switch is usually on for some 10ms, the µC has to send refresh pulses of about 2µs every 500µs. This corresponds to a duty cycle of 99.6%. Demo-software and demo-board based on TLE6280GP and µC C164 are available.
2) As the charge pump is triggered by the ILx pins, the performance of the charge pump is dependent on the input pattern. As shown in the datasheet (fig. 3 datasheet), the output performance of the charge pump is reduced when all switched half-bridges are running with a duty cycle of less then 10% at 20kHz. The reason is that the time where the charge pump is in low position is now to short to recharge C_{CP}.

The complete timing of the supply chain can be described by the three parts mentioned at the beginning. 2 parts of that chain can be described in first order by a RC time.
The RC time of the first part is obvious.
The second part is charge pump. This part can be described partly as resistor of about 10Ω, a diode with forward drop of 0.7V and the C_{CP} capacitor. In addition to that description, there are some reaction times to be considered for this part of the supply chain.

The third part is the C_{Bxx} capacitor with a diode described by an ideal 0.7V forward voltage and an R given in the datasheet.
At higher gate charges, note that the times to charge the C_{Bxx} get longer and the implementable duty cycle range is limited.
At higher PWM frequencies same charging times mean a reduction in the duty cycle range. A precise description of the behavior is given by the Infineon Saber model of the TLE6280GP, available on the internet.

In addition to the considerations about the duty-cycle range, the user will make sure that the integrated voltage controller is not overloaded, caused by high supply voltages, high PWM frquences or very large external Mosftes.
The maximum permissible power loss P_{tot} is 1.2W. The actual power loss can be estimated using the following formula:

$$P_D = (Q_{gate} * n * const + I_{VS(open)}/20kHz) * f_{PWM} * V_{Vs} - P_{RGate}$$

With:

P_D	= Power dissipation in the driver IC
f_{PWM}	= Switching frequency
Q_{gate}	= Total gate charge of used MOSFET at 10V V_{GS}
n	= number of switched Mosfets
const	= constant considering some leakage current in the driver and the power dissipation caused by the charge pump (about 2)
$I_{VS(open)}$	= Current consumption of driver without connected Mosfets during switching
V_{VS}	= Voltage at Vs
P_{RGate}	= Power dissipation in the external gate resistors

This value can be reduced dramatically by usage of external gate resistors.
PWM frequencies above 30 kHz can also be implemented when these conditions are observed.

4.4.   Recommended start up procedure

The fact that the input pins ILx are triggering the charge pump lead to some considerations about a possible start up sequence.
1) In a fist step the aim is to keep the external Mosfets off during start up. This means that the user has to assure that the voltage at the MFP pin keeps below 1V. This is assured by internal pull down as long as the µC output port, connected to this pin, is in

tri-state or pull down mode. In dependent to the supply voltage, this guarantees that all Mosfets will be permanently actively switched off.

2) At supply voltages below 9.5V it is now recommended to trigger all ILx pins with the PWM frequency and 50% duty cycle. All 3 half-bridges should be triggered simultaneously. This assures that the charge pump is running and that the CCP and CBLx capacitors are charged fully and the there will be no current in the motor when the device will be enabled and the PWM patterns stay the same.

3) The next step is to enable the device by setting VMFP to values between 2.5 and 4V. The best timing to do this is some µs before the next transition of the ILx from low to high. This assures that the device will be awake when the next switch on signal for the low-side Mosfets occurs. This means that the low-side Mosfets will switch on and make sure that the bootstrap capacitors will be charged.

    The 50% duty cycle, still applied to the input pins guarantees a running charge pump and filled bootstrap capacitors even at low supply voltages of less then 8V.

    The user can keep this situation as long as the motor is not used. This is a good starting point to start the motor.

Remarks:
In the procedure described above, only the ILx pins are mentioned. They are decisive for the function of the charge pump. Of course the IHx pins can be triggered with the same PWM pattern. The result for the application should be the same.
Not triggering the ILx inputs means that the charge pump is not working. An example is a so called 0-vector, permanently switching on the low-side Mosfets. In this situation, there is the possibility with supply voltages below 9.5V that there is a undervoltage shut down of the output stages at –40°C. See datasheet.

4.5. The Integrated Undervoltage Monitor

Every driver stage has its own voltage monitor. If the voltage V_{Bxx} - V_{Sxx} drops below a typ. 10V the ERR pin is set and an undervoltage warning is emitted.
This architecture offers the advantage that the function of the external capacitor of the charge pump C_{CP} and the bootstrap or support

capacitors C_{Bxx} are monitored as well and a failure is detected reliably.
However, since the driver has also been designed for applications concerning safety in which independent switching off of the driver is only acceptable in an absolute emergency, operation is maintained and a reduced gate voltage at the power transistors taken into account. The functioning of the driver is still guaranteed in this undervoltage range. Individual data of the specification, such as "High level output voltage min = 8V" are no longer guaranteed however.
If the voltage of a bootstrap capacitor C_{Bxx} reaches the undervoltage shut-down level, the Gate-Source voltage of the affected external Mosfet will be actively pulled to low. In this situation the short circuit detection of this output stage is deactivated to avoid a complete shut down of the driver. This allows continued operation of the motor in case of undervoltage shut-down for a short period of time.
As soon as the bootstrap voltage recovers, the output stage condition will be aligned to the input patterns by the next changing input signal at the corresponding input pin.

4.6. The Input Architecture and the Shoot Through Protection

The TLE6280GP has its own input for every output. This gives the user the greatest possible freedom in designing the PWM pattern.
The input signal of the high-side inputs is inverted additionally. This allows the low-side and high-side inputs to be combined in one signal. This means that the bridge can be controlled from the µC with only 3 input lines. In this case the driver takes care of dead time generation to avoid cross currents due to simultaneously open high and low side switches. The dead time is set by connecting a resistor in relation to Logic-Gnd at the DT pin.
The correlation between dead time and external resistance can be read on the data sheet.
Several diagrams explain how the shoot through protection and the dead time work.
Figure 6 illustrates the case of connected ILx and IHx pins. First it should be noted that there are always propagation times between the input signal and reaction at the output. These propagation times are specified in the data sheet..
As the propagation times for switching on or off for the high or lowside Mosfets are not identical, these propagation time differences have some influence in the resulting dead time.
One example is given here:
The lowside Mosfets will be switched off and the highside Mosfet will be switched on.
R_{DT}=0kΩ corresponding to a typical dead time of 80ns. According the datasheet there is:
$t_{P(IHF)}$= 200ns
$t_{P(ILN)}$= 280ns

The difference is 80ns which is increasing the dead time aot the output to 80+80ns = 160ns
The following times are given in the datasheet:
1) All propagation times for all channels for switching on – the maximum time difference of all these times is $t_{PD(an)}$.
2) All propagation times for all channels for switching off – the maximum time difference of all these times is $t_{PD(af)}$.
3) The propagation time difference between switching one lowside on and the corresponding highside off $t_{PD(1lnhf)}$.
4) The propagation time difference between switching one lowside off and the corresponding highside on $t_{PD(1lnhn)}$.
5) All propagation times for all channels for switching a highside off together with all propagation times for all channels for switching a lowside on – the maximum time difference of all these times is $t_{PD(ahfln)}$.
6) All propagation times for all channels for switching a lowside off together with all propagation times for all channels for switching a highside on – the maximum time difference of all these times is $t_{PD(alfhn)}$.

The dead time for GHx and GLx is always the same here and is independent of the duty cycle. It should also be noted here that the set dead time can result in a change in the duty cycle between input and output. An extreme example shown in fig.7 illustrates this. If a dead time of 2µs is preset and a switch is only to be switched on for 1 µs, the transistor to be switched off is switched off briefly because the input pulse is longer than the propagation time but the power transistor to be switched on in this half bridge remains off because the dead time is longer
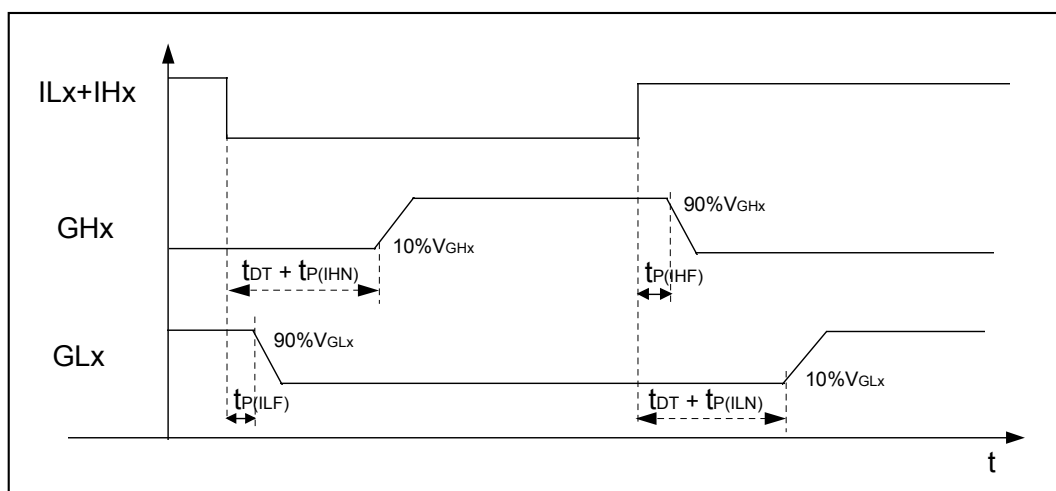

Fig. 6: Dead time behaviour with connected input pins

than the on-time.

selected dead time prevents switching on.
If you want to change the dead time during
operation or you want to have the greatest
possible freedom in switching the power
transistors, it is of advantage to control the low
and high side inputs separately – see datasheet.
If the time difference between the change at the
low and high side input is shorter than the dead
time, you get the same picture at the output
which you would have had with a simultaneous
input signal change. See fig.8.
Output signals are only modified at time
differences that are greater than the set dead
time.
Here you can see clearly that the internally
generated dead time can be used to guarantee
a minimum dead time and the actual dead time

is checked by the µC.

The behavior of the driver in reaction to faults in
the input signals and to incorrect instructions
which would lead to simultaneous switching on
of the high and low side switch and thus to
short-circuiting of the bridge is particularly
important.
Examples are shown in fig. 8.

Here you can see that the driver does not react
to the input signal for switching on the second
switch and the outputs remain stuck in the
previous status. This guarantees that the PWM
pattern of the outputs is not falsified in the case
of voltage peaks (EM susceptibility) and other
faults.
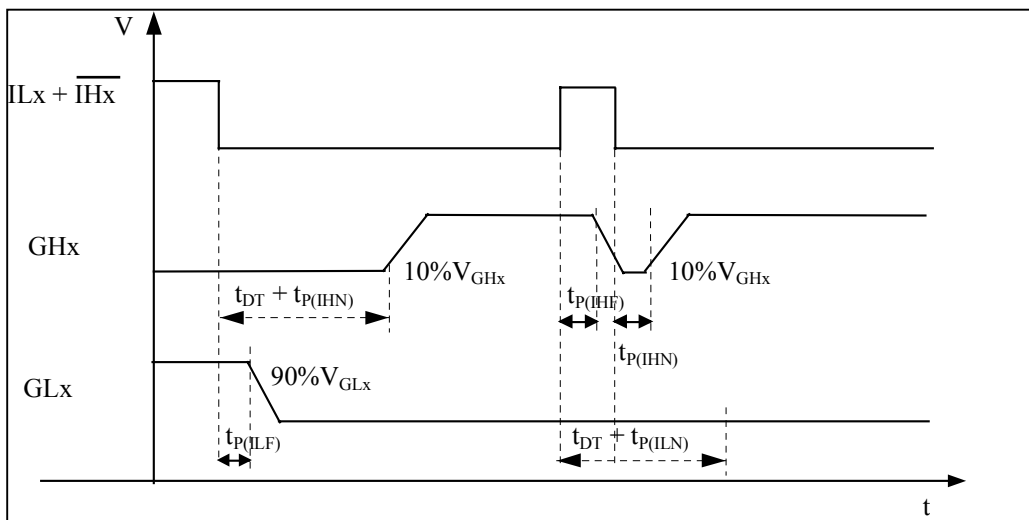
Fig. 7: Influence of the dead time in the case of very short changes at the input
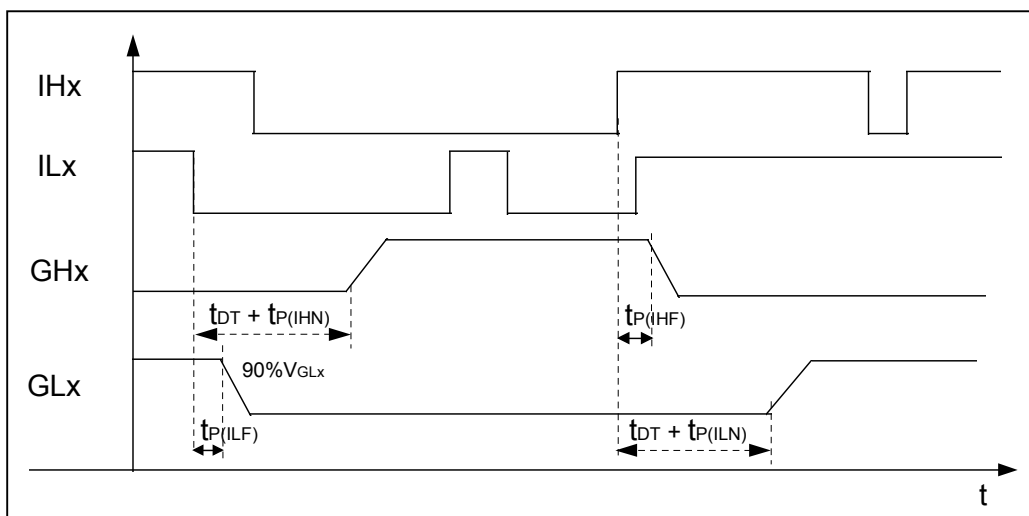
Fig. 8: Influence of misleading input commands to the output

4.7. Short-circuit Protection and Current Limiting

To protect the connected Mosfets the driver constantly monitors the Drain-Source voltages V_{DS} of the external transistors switched on. If this voltage is higher than $V_{DS(SCP)}$, the gate source voltage V_{GS} of this Mosfet is first limited to a voltage value $V_{GS(lim)}$ which can be adjusted externally. This gives a maximum drain current corresponding to the output characteristic of the connected power Mosfet and thus current limiting in the event of a short-circuit.
$V_{GS(lim)}$ and $V_{DS(SCP)}$ are programmed by the user by applying a voltage between 2.5 and 4V at the MFP pin. $V_{GS(lim)}$ at $V_{DS} > V_{DS(SCP)}$ is given by double the applied MFP voltage and can therefore be selected between 5 and 8V.
$V_{DS(SCP)}$ varies, dependent on the MFP voltage, between 1 and 3V.
Fig. 9 shows the behavior in the event of a sudden short-circuit. V_{MFP}=3V was chosen as an example. Which corresponds to a $V_{GS(lim)}$=6V and $V_{DS(SCP)}$ = 1.75V .

The Mosfet is initially fully modulated (V_{GS}=10V) and the I_D in the normal working range. Then a short-circuit occurs and both I_D and V_{DS} increase suddenly. After a delay of typical 100ns the gate voltage is reduced and I_D reduced. After approx. 11µs the driver switches off all Mosfets and sets the error flag.
To reset the driver, the MFP pin must be pulled to under 1.1V and a 'disable' set.
It should be noted in particular that this current limiting becomes active initially every time a
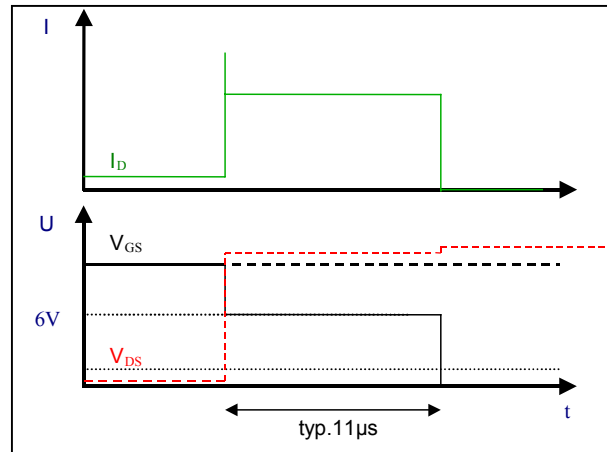
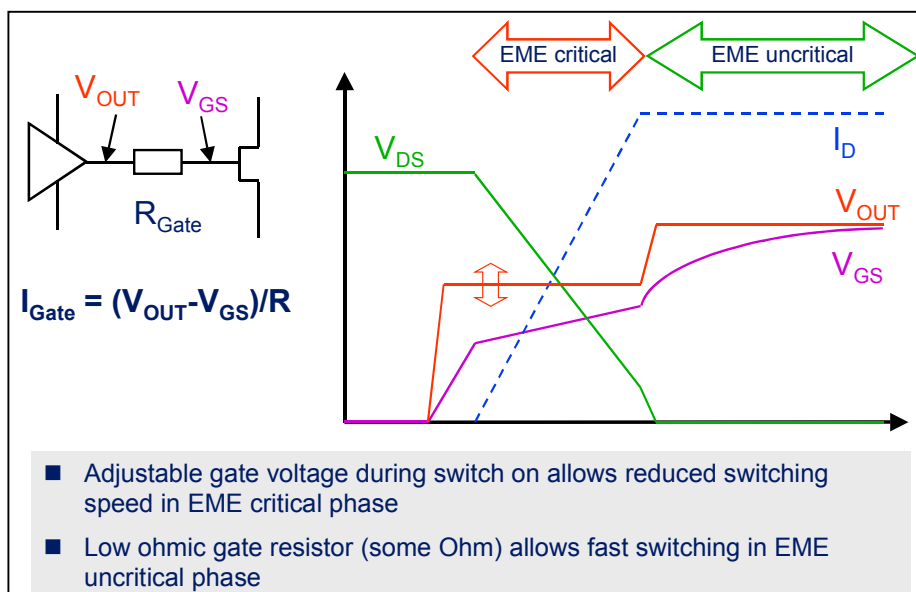**Fig.9: Behavior in the event of a sudden short-circuit**

power Mosfet is switched on because the V_{DS} is always above 1.75 V at the start of the switching process. This leads to a very "gentle" 2-stage switching on of the Mosfet if the user selects a $V_{GS(lim)}$ only just above the Miller plateau of the power transistor at preset zero. After V_{DS} has dropped below 1.75V (V(MFP)=3V), the full driver power is available again to pull V_{GS} to 10V as quickly as possible.
This ensures there is no unnecessary power loss in the Mosfet. See fig.10.
Here, $V_{GS(lim)}$ must be high enough to ensure that the transistor can also take over the motor current to be controlled and V_{DS} drops below 1.75V.
Determination of this value is shown by example of a BUZ111S and its output characteristic in fig. 11.
A maximum current of 60A is assumed. This

$$I_{Gate} = (V_{OUT} - V_{GS})/R$$

- Adjustable gate voltage during switch on allows reduced switching speed in EME critical phase
- Low ohmic gate resistor (some Ohm) allows fast switching in EME uncritical phase

Fig.10: Two-stage switch-on behaviour of the TLE6280GP

gives a minimum V_{GS} of about 5.0V. If you take into account the tolerance of the threshold voltage of +/- 1V at room temperature and a temperature response of the threshold voltage between –40°C and +25°C of 0.4V this gives a lower limit for $V_{GS(lim)}$ of 5.0 + 1 + 0.4 = 6.4V. If a voltage below 3.2V is applied to the MFP pin and if 100A are to be switched, it is possible that the driver recognizes this as a short-circuit and switches off. Taking in account that the factor between V(MFP) and $V_{GS(lim)}$ has some tolerance as well, we have to calculate with

V(MFP) = 6.4V / 1.67 = 3.85V

In this context it should be pointed out that the voltage at the MFP pin must reach the desired value between 2.5 and 4V at the MFP pin within 50µs after a disable otherwise there is a danger

that the short-circuit detection will switch off the driver due to the $V_{GS(lim)}$ being too low.

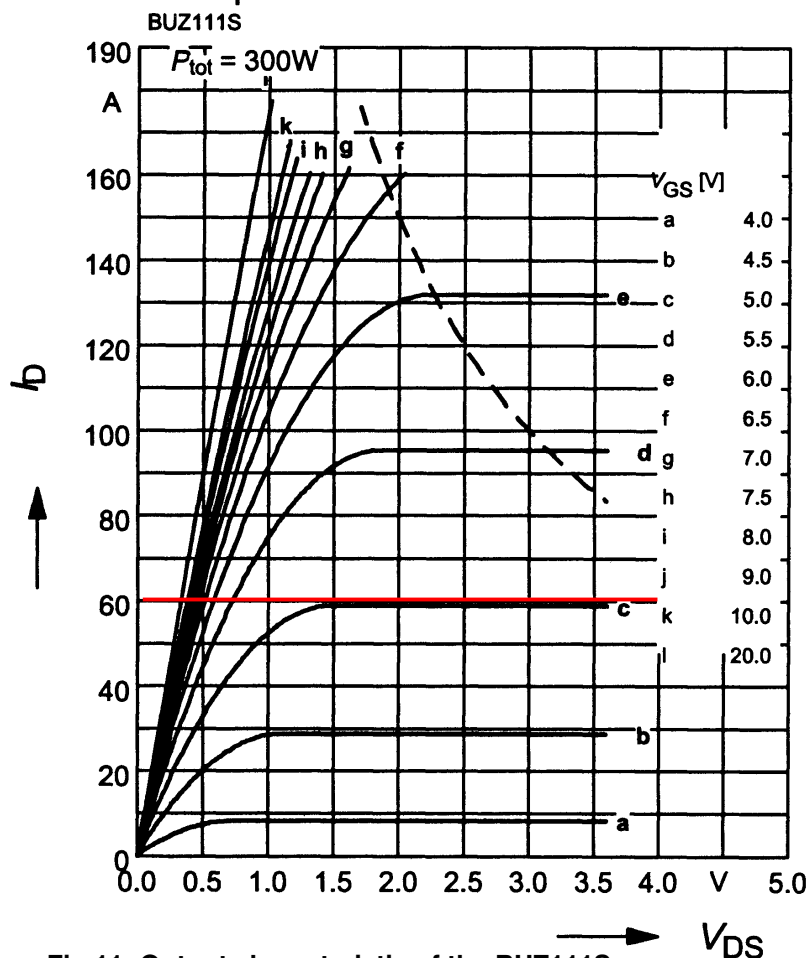# Typ. output characteristics

$$I_D = f(V_{DS})$$

parameter: $t_p = 80$ µs

Fig.11: Output characteristic of the BUZ111S

4.8. The dI/dt Control

Why a dI/dt control? To answer this question let us first have a look at a typical structure of a high current motor bridge. Particular attention should be paid in these clocked high current applications to switching losses and EMC radiation.
Basically the switching speed of the Mosfet should on the one hand be as high as possible to minimize switching losses, on the other hand the effort for suppressing EMC interference increases at high switching speeds.

Figure 12 again shows only one branch of a 3-phase bridge. With this example the current and voltage relationships when switching off the low-side switch are to be looked at briefly and the function of the dI/dt control explained.
The following examination has been greatly simplified. This is allowed for a rough observation.
The following initial situation is assumed: The low side switch is switched on and the high side switch is switched off. The motor current flows out of the motor through the low side switch to ground. Switching off the low side switch will lead to free-wheeling of the motor current in the high side switch. The current is "deflected" from the low side switch to the high side switch. The

stray inductance has a special significance in this path.
The dI/dt is the same in all stray inductances in the outer circuit shown. The voltage generated at the individual stray inductances is:

$$(2) \qquad U_L = \frac{dI}{dt} * L$$

The induced voltages at the stray inductance is therefore directly proportional to the stray inductance. The resulting voltages are already shown in figure 7. Applying the 2nd law of Kirchhoff this gives:

$$(3) \qquad \begin{aligned} & 20*U + 14V + U_R + 20*U + \\ & 10*U - U_{DSH} + 5*U + 5*U - \\ & U_{DSL} + 10*U = 0V \end{aligned}$$

Ignoring U_R and assuming U_{DSH}=-1V (body-diode in conducting direction) it applies that:

$$(4) \qquad 70*U + 15V = U_{DSL}$$

The maximum voltage that a Mosfet can take is its breakthrough voltage V_{BRDSS}. On the assumption that V_{BRDSS} is 40V in our case, a U of 0.36V is given with U_{DSL}=40V for the event that the Mosfet is in breakthrough.

Fig.12: Stray inductance in a half bridge

To determine the dI/dt, the stray inductance is observed with 10nH:

$$(5) \qquad \frac{dI}{dt} = -\frac{10*0,36V}{10nH} = -360\frac{A}{\mu s}$$

On the assumption that I is 120A at time t_0 and that the low side switch is in avalanche breakthrough, the decaying of the current in the low side switch takes about:

$$(6) \qquad t = \frac{dt}{dI} * I(t_0) = 333ns$$

This value cannot be underbid even by switching off the power transistor faster because the minimum decay time for the current is given by the value of the current to be switched, the stray inductance in the circuit and the maximum V_{DS} of the power transistor.
This results for the situation described above in which the Mosfet goes into breakthrough at 40V in the voltages shown in figure 13.

The aim will be to avoid breakthrough at the power transistor and still to switch as quickly as possible to minimize switching losses in the Mosfets. To achieve this, V_{DS} of the power switch must be just below its breakthrough voltage for as long as possible. This can be achieved with the aid of the dI/dt control with careful design.
Usually the switching speed is set without dI/dt control when using conventional drivers by adapting the gate bias resistors. Since here, V_{DS} of the power switch is not constant over time and the bias resistor needs to be dimensioned so that the max. V_{DS} is still below the breakthrough, the switching time is lengthened unnecessarily with this procedure.

The following hints should simplify application and tuning of the dI/dt control in the application.
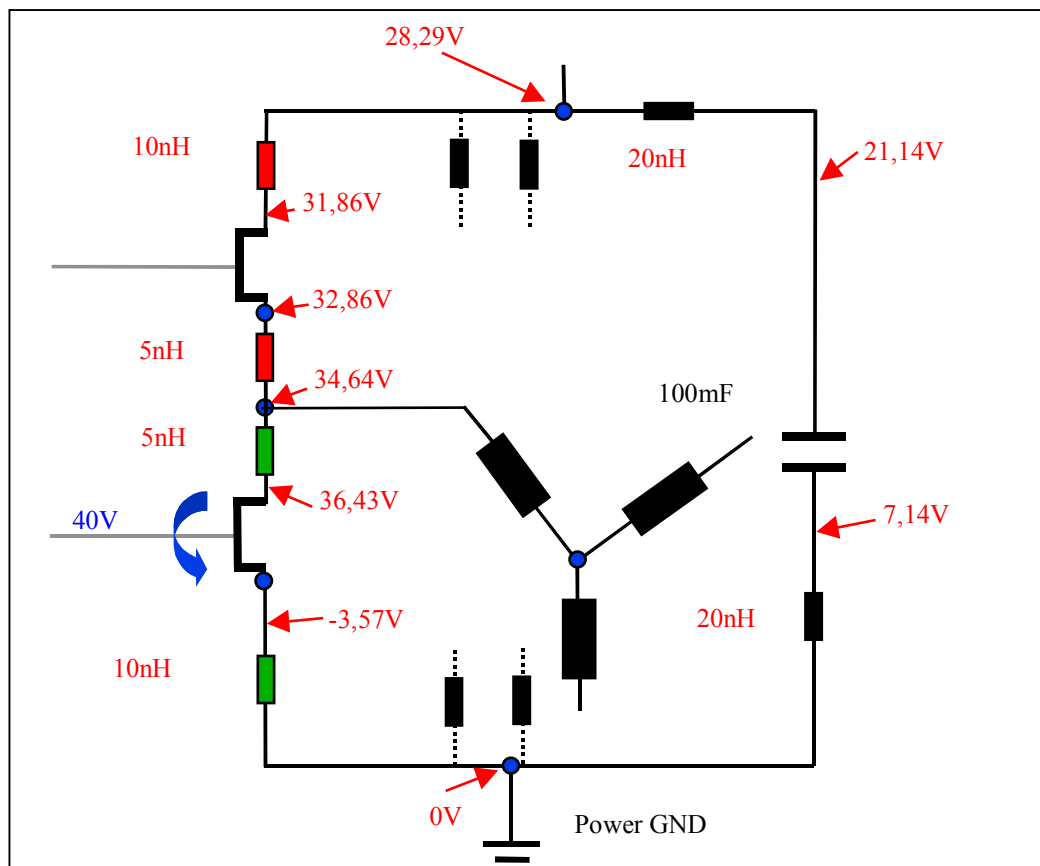
Fig.13: Voltages in the circuit when switching off the low side switch

First let us explain the principle function in simple terms.

Figure 14 shows the basic components. The dI/dt control monitors the overvoltages at the tapping point by a voltage tap and slows down switching of the Mosfet on exceeding and dropping below a defined voltage level. In figure 14 the common node of all three half bridges at the V_{bb} side is chosen as a potential tap. With the aid of an high pass filter formed by a RC element at the dI/dt pin the AC voltage part of the signal is fed to the dI/dt pin.

The DIDT pin has an internal impedance of 60Ω towards GND in the frequency range between some kHz and 10MHz. This 60Ω form together with the external RDIDT a voltage divider. The impedance of the dIDT pin has to be considered in the design of the high pass filter.

If the voltage drops or rises at the dI/dt pin related to Logic-GND to over $|V_{dl/dt}| > 2V$, the output current of the driver stages is reduced to reduce the switching speed of the connected Mosfet. The dI/dt control achieves its full effect at $|V_{Dl/dt}| = 7V$. With the help of the voltage divider at the dI/dt pin it can therefore be determined at which overvoltages and under voltages the dI/dt control comes into effect at the tapping point.

Figure 15 shows the effect of the dI/dt control

with an example. The initial situation is as described above: The low side switch is switched on and the high side switch is switched off. The motor current of 120A flows out of the motor through the low side switch to ground. Switching off of the low side switch leads to free wheeling of the motor current through the high side switch and thus to a situation similar to that in figure 12.

The top diagram in figure 15 shows the current flow through the low side switch. The bottom diagram represents the voltage at the tapping point (see fig. 9 and 10). The intermitted green line shows the flow without dl/dt control. The high over voltage of about 37V is clearly visible. The over voltage is limited to about 23V (full line) by using the dl/dt control.

The full blue line shows a situation with higher stray inductance than the full green line. The longer switching times given by different stray inductance are clearly visible when the over voltage at the tapping point is kept almost constant by the dl/dt control.
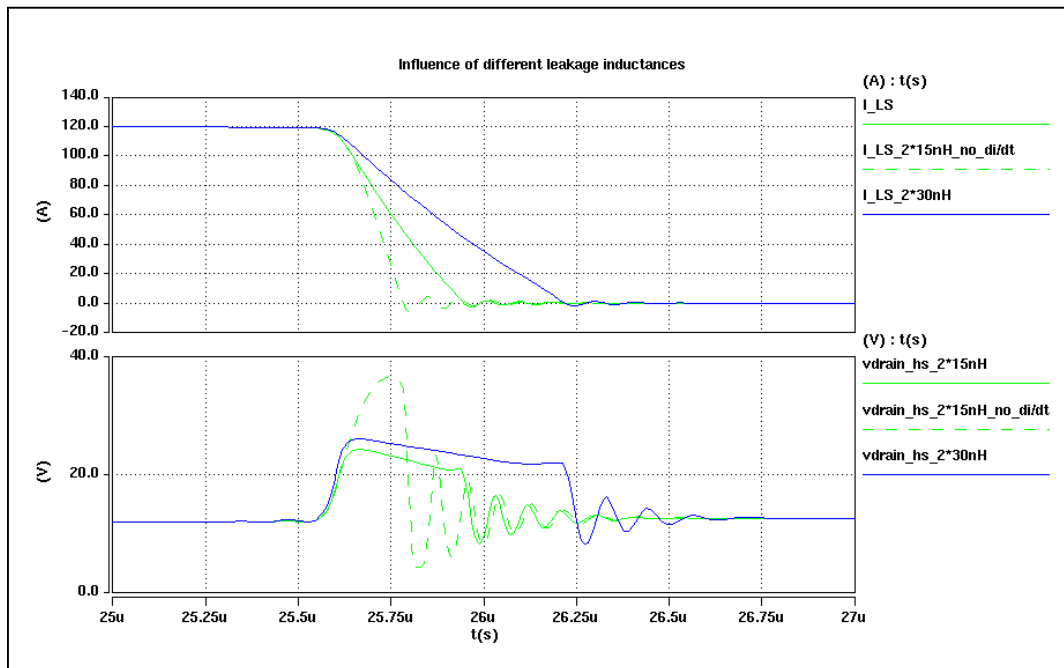
Figure 16 shows the gate voltage corresponding to this situation and the driver output current for the low side switch.

The upper diagram in figure 16 shows V_{GS} of the low side switch, the middle diagram the corresponding driver currents and the lower
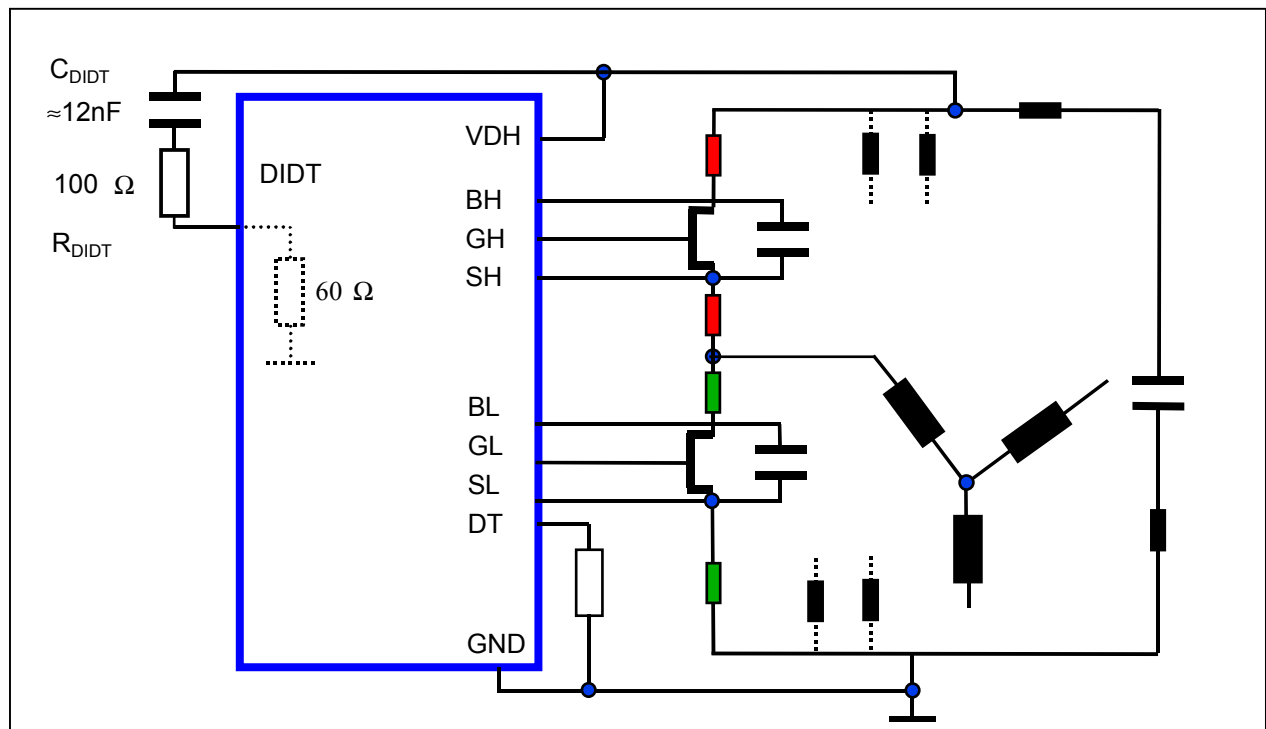


Fig.14: External wiring of the dI/dt pin

Fig.15: Over voltage limiting by the dI/dt control

diagram the voltage at the tapping point. The green line shows the uncontrolled case, the blue line the case with active dI/dt control. It is clearly visible here that the dI/dt control reduces the driver currents immediately or in this case reduces them to zero as soon as the overvoltage occurring at the tapping point activates the dI/dt control. V_{GS} remains almost

constant and thus the switching time of the Mosfets is increased to the necessary size.

The following conditions must be observed in the dimensioning of the external components and the layout of the power unit:

A) Time constant of the RC element at the dI/dt pin together with the internal
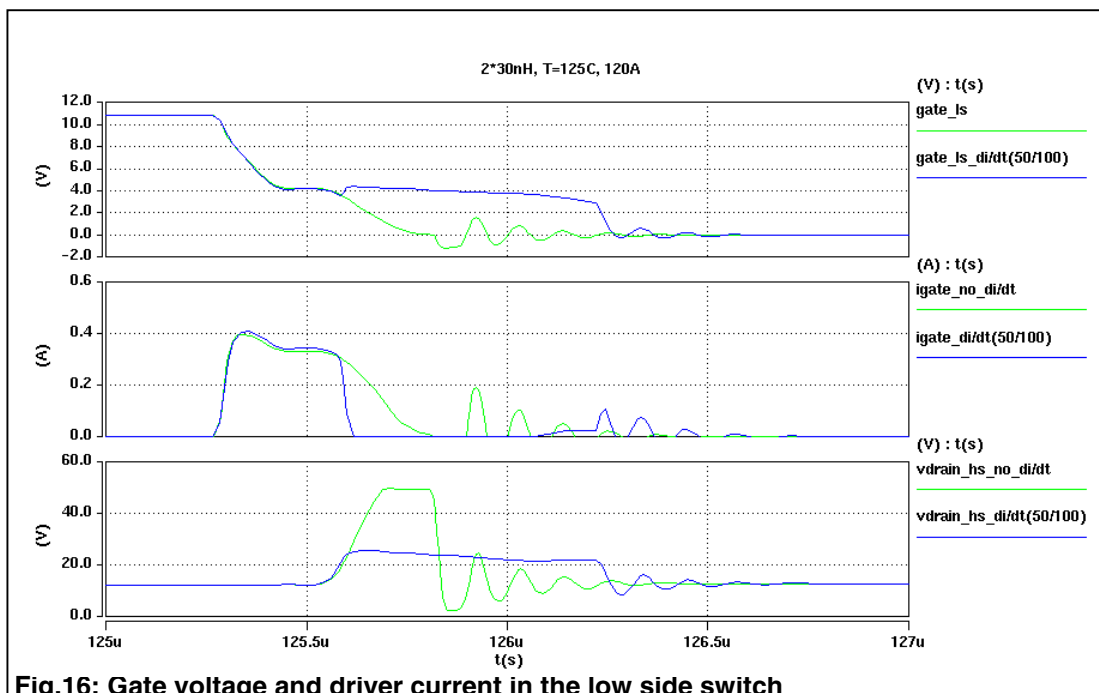
Fig.16: Gate voltage and driver current in the low side switch

impedance of the DIDT pin towards GND

B) Choice of the tapping point for the dI/dt control with appropriate design of the voltage divider at the dI/dt pin

C) Avoiding dipping of the voltage at the SLX pins below –7V related to Logic-GND

4.8.1. Time Constant of the RC Element at the dI/dt Pin

Transient overvoltages during the switching process have a duration of less than 1µs. These transient voltages have to be transferred to the DIDT pin.

Therefore the high pass filter has to be dimensioned in that way that the RC time is in the range of 2-3µs.

4.8.2. Selection of the tapping point for the dI/dt control with appropriate design of the voltage divider at the dI/dt pin

Two essential points need to be considered when selecting the tapping point for the dI/dt control.

Firstly the tapping point should measure the overvoltages in the three half bridges as evenly as possible otherwise the control effect is different for the three half bridges.

Secondly the over voltage generated by

Since the emphasis will be on reducing the stray inductance in the design of the power unit and a few other aspects need to be considered as a rule, compromises may be necessary under some circumstances.

A good compromise is shown in fig. 17. Here the drain potentials of the high side switches are tapped directly and combined in star shape via 100Ω resistors. The star-shaped combination forms a medium over voltage from the respective drain potentials which form a suitable input signal for the dI/dt pin.

The user will first consider when dimensioning the voltage divider at the dI/dt pin which over voltage he wants at the maximum at his tapping point. Based on this value, the voltage divider must now be dimensioned so that about 5V arrive as a signal at the dI/dt pin at this selected over voltage.

It should also be noted that the voltage at the tapping point will be lower than the maximum voltage in the circuit (see figure 8). Avoiding dipping of the voltage at the SLX pins below –6V related to Logic-GND

The TLE6280GP has its own source connection for every low side switch.

This enables good checking of the V_{GS} of these switches because these connections can be made as close as possible to the source pin of
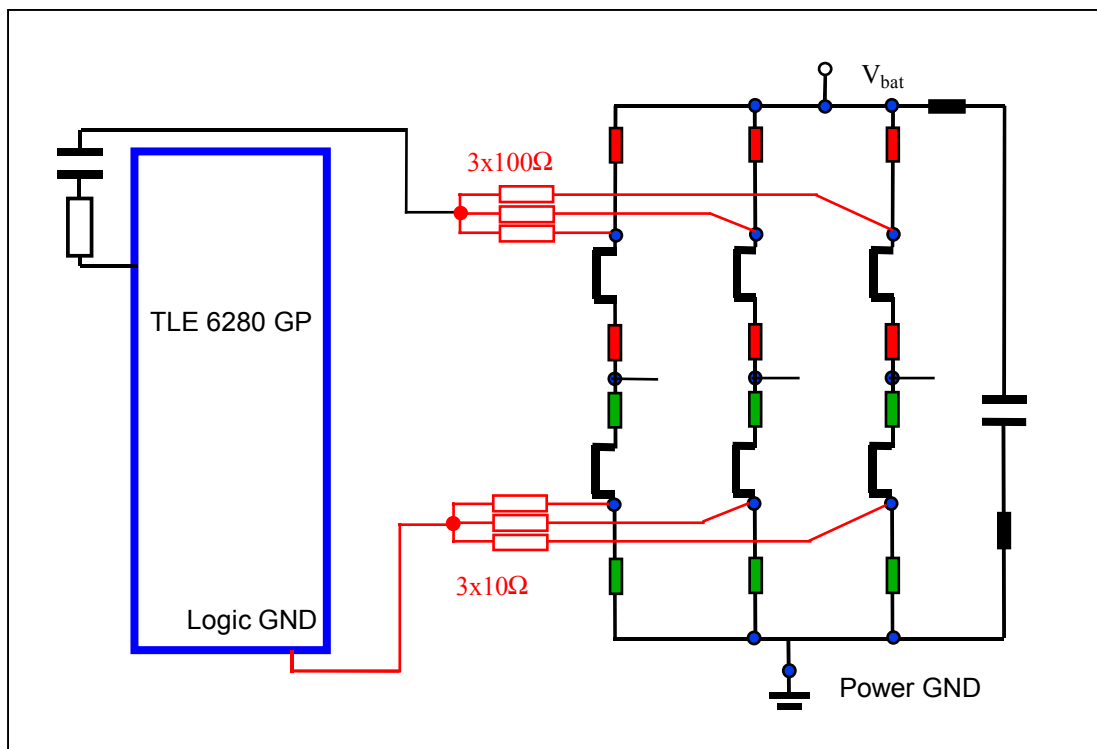
switching at this point should be high enough for the dI/dt control to respond.

the Mosfet.

Therefore the common part of the power path

Fig.17: Example for tapping the Logic-GND and the dI/dt signal

and the trigger circuit of the Mosfet are minimized and faults in the trigger circuit are kept to a minimum.

The Logic-GND of the TLE6280GP can be connected with the power ground of the bridge. This concept reaches its limits as soon as the maximum ratings of the SLx pins are violated. This happens when the voltage at the source of the low side switches drops even temporarily below –7V related to Logic-GND.

If this is the case, the GND pin of the driver is not connected with the Power-Ground. Here too, tapping of the source potentials of the low side switches and a star-shaped combination through resistors is useful. This common point then represents the Logic-GND.

An absolutely symmetrical structure of the inverter with as evenly distributed stray inductance as possible is optimum for functioning of the dI/dt control.

5. Conclusion

The first member of the Infineon Technologies gate driver IC family is designed especially for high current applications.

Beside the basic features, necessary to drive such a high current bridge like

- high output performance
- full gate voltages even at low supply voltages
- power package allowing high ambient temperatures

the TLE6280GP offers additional features like

- diagnosis
- short circuit protection
- current limitation
- dI/dt control.

The advantages of the dI/dt control are:

- The switching losses in the Mosfaets of the bridge can be minimized.
- The costs for the used Mosfets can be minimized by limiting the overvoltages in the bridge.
- The cost for the EMC filters can be reduced by regulating the maximum dI/dt.

This feature set is unique on the market for driver ICs and enables the user to achieve optimized system solutions for electric power steering, electro-hydraulic power steering, cooling fans and other high current 3-phase drives.

6. Product family overview

Missing

7. Disclaimer

8. Infineon goes business Excellence

"Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction."

Dr. Ulrich Schuhmacher