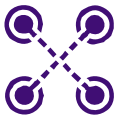

WIRELESS

88W8686

Integrated MAC/Baseband/RF Low Power SoC

IEEE 802.11a/g/b

Datasheet

Doc. No. MV-S103342-00, Rev. D
February 20, 2007
Document Classification: Proprietary

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Features

The Marvell® 88W8686 is a low-cost, low-power highly-integrated IEEE 802.11a/g/b MAC/Baseband/RF WLAN system-on-chip (SoC), designed to support IEEE 802.11a or 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5, and 11 Mbps.

The device provides the combined functions of the IEEE Standard 802.11/802.11b Direct Sequence Spread Spectrum (DSSS), 802.11a/g Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct conversion WLAN RF radio on a single integrated chip.

The core functional units of the 88W8686 are connected with a high throughput interconnect system, as shown in Figure 1.

The 88W8686 is equipped with a fully integrated RF to baseband transceiver that operates in both the 2.4 GHz ISM radio band for 802.11g/b WLAN applications and 5 GHz UNII radio band for 802.11a WLAN applications. It contains all the circuitry to support both transmit and receive operations.

The transceiver architecture includes a Marvell second-generation radio, designed specifically for co-existence with cellular phones. Cellular band transmit spurious tone, noise, and receive jammer considerations have been designed for into the device. Due to very low spectral emissions in the cellular phone receive band, the device does not interfere with cellular phone reception and is immune to high power cellular phone transmission signals.

For optimum performance, the gain adjustment of the integrated LNA and AGC on the receive path is seamlessly controlled by baseband functions. The entire receive path has over 90 dB of voltage gain and gain control range.

Integrated transmitters up-convert the quadrature baseband signal, and then deliver the RF signals to external power amplifiers for 2.4 GHz and 5 GHz radio band transmission.

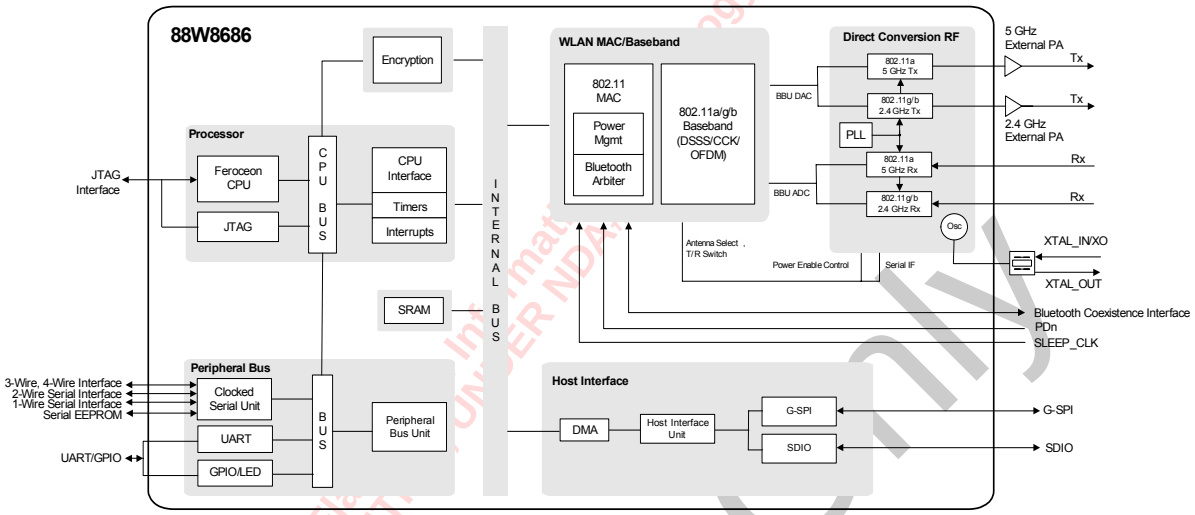
Local oscillator frequencies are generated by a fully integrated programmable frequency synthesizer without any external components. The loop bandwidth is optimized for phase noise and dynamic performance and quadrature signals are generated on-chip.

For security, the 88W8686 supports the IEEE 802.11i security standard through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) security mechanisms.

For video, voice, and multimedia applications, the 88W8686 supports 802.11e Quality of Service (QoS). A Bluetooth coexistence interface is also supported.

The 88W8686 supports both a generic SPI (G-SPI) and SDIO host interface and is available in QFN and flip chip packages.

Figure 1: Top Block Diagram



Reference Designs

Marvell reference designs are highly-integrated low cost, production quality designs that provide a quick time-to-market solution for customers developing single chip IEEE 802.11a/g/b WLAN solutions.

The 88W8686 maintains software driver compatibility with current Marvell two-chip solutions (88W8385 and 88W8015). Customers already engaged in designing current Marvell solutions can leverage a fully validated tool chain. For further information, contact Marvell representatives.

APPLICATIONS

- Cellular handsets
- Consumer electronic devices that require low power consumption

GENERAL FEATURES

- Ultra low-power dissipation
- Single-chip integration of 802.11a/g/b wireless RF and baseband, MAC, CPU, memory, and host interfaces
- Integrates all RF to baseband transmit and receive operations, with support for external PAs
- Fully integrated frequency synthesizers with optimized phase noise performance for OFDM applications
- Integrated direct conversion WLAN RF radio
- Supports 19.2, 20, 24, 26, 38.4, and 40 MHz oscillator clock sources
- Software backward compatible with 88W8385 and 88W8015 devices

PAYLOAD DATA RATES

- IEEE 802.11 data rates of 1 and 2 Mbps
- IEEE 802.11b data rates of 5.5 and 11 Mbps
- IEEE 802.11a/g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission

PACKAGING

- 68-pin QFN package
- 280 µm pitch flip chip
- 500 µm pitch flip chip[1]

PROCESSOR

CPU

- Integrated Marvell Feroceon® CPU(ARMv5TE-compliant)
- Offloads wireless protocol stack processing from host CPU
- 128 MHz operating frequency

DMA

- Independent 2-channel Direct Memory Access (DMA)

NETWORKING FUNCTIONS

WLAN MAC

- Supports Ad-Hoc and Infrastructure modes
- Supports Contention Free (CF)-Poll and CF-ACK for operation under Point Coordination Function (PCF)
- Supports Request-to-Send (RTS)/Clear-to-Send (CTS) for operation under Distributed Coordination Function (DCF)
- Hardware filtering of 64 multicast and 96 unicast addresses and additional firmware options
- On-chip Tx and Rx FIFOs for maximum throughput
- Support for 802.11e QoS
- Support for 802.11h DFS statistics processing
- Supports Open System and Shared Key Authentication services
- Supports long and short preamble generation on a frame-by-frame basis
- Supports IEEE Power Save mode

WLAN BASEBAND

- DSSS and OFDM modulation
- Advanced Equalizer for Complementary Code Keying (CCK) modes
- Differential Binary Phase Shift Keying (DBPSK), Differential Quadrature Phase Shift Keying (DQPSK), and CCK modulation modes
- 16-QAM and 64-QAM modulation
- On-chip A/D and D/A converters for Inphase/ Quadrature (I/Q) channels
- Targeted for multi-path delay spreads up to 680 ns in 11 Mbps mode and 150 ns in 54 Mbps mode
- Supports 802.11h (DFS and TPC) statistics gathering
- Supports 802.11j channels (Japan)

1. 500 µm flip chip option supports 802.11g/b only.

WLAN RF

Rx Path

- On-chip gain selectable LNA with optimized noise figure and power consumption
- Highly integrated architecture eliminates need for external SAW filter
- High dynamic range AGC function in receive mode
- Immune to high power cellular phone transmission signals

Tx Path

- Image-reject transmitter to reduce external RF filter count for 2.4 GHz radio transmit
- Supports external PA with power control for both 2.4 GHz and 5 GHz operation
- Supports closed and open loop power control in increments of 0.5 dB
- Very low spectral emissions in the cellular phone receive band

WLAN Encryption

- WEP 64- and 128-bit encryption with hardware TKIP processing
- WPA (Wi-Fi Protected Access)
- CCMP hardware implementation as part of 802.11i security standard

Networking Coexistence

- Supports Marvell 2-Wire Bluetooth Coexistence Arbitration (2WBCA) scheme
- Supports Marvell 3-Wire Bluetooth Coexistence Arbitration (3WBCA) scheme
- Supports Marvell 4-Wire Bluetooth Coexistence Arbitration (4WBCA) scheme

Host Interfaces

- G-SPI device interface
- SDIO device interface

Memory

Frame Buffer

- Internal SRAM for Tx frame queues and Rx data buffers

Boot ROM

- Boot ROM

Peripheral Bus Interfaces

- General Purpose Input Output (GPIO)
- Flexible GPIO interface with Light Emitting Diode (LED) driver to indicate Tx/Rx activities
- Universal Asynchronous Receiver/Transmitter (UART)
- Clocked Serial Unit
  - 3-Wire, 4-Wire (3W4W) Interface
  - 2-Wire Serial Interface (TWSI)
  - 1-Wire Serial Interface
  - SPI Serial (EEPROM)

Test

- On-chip diagnostic registers

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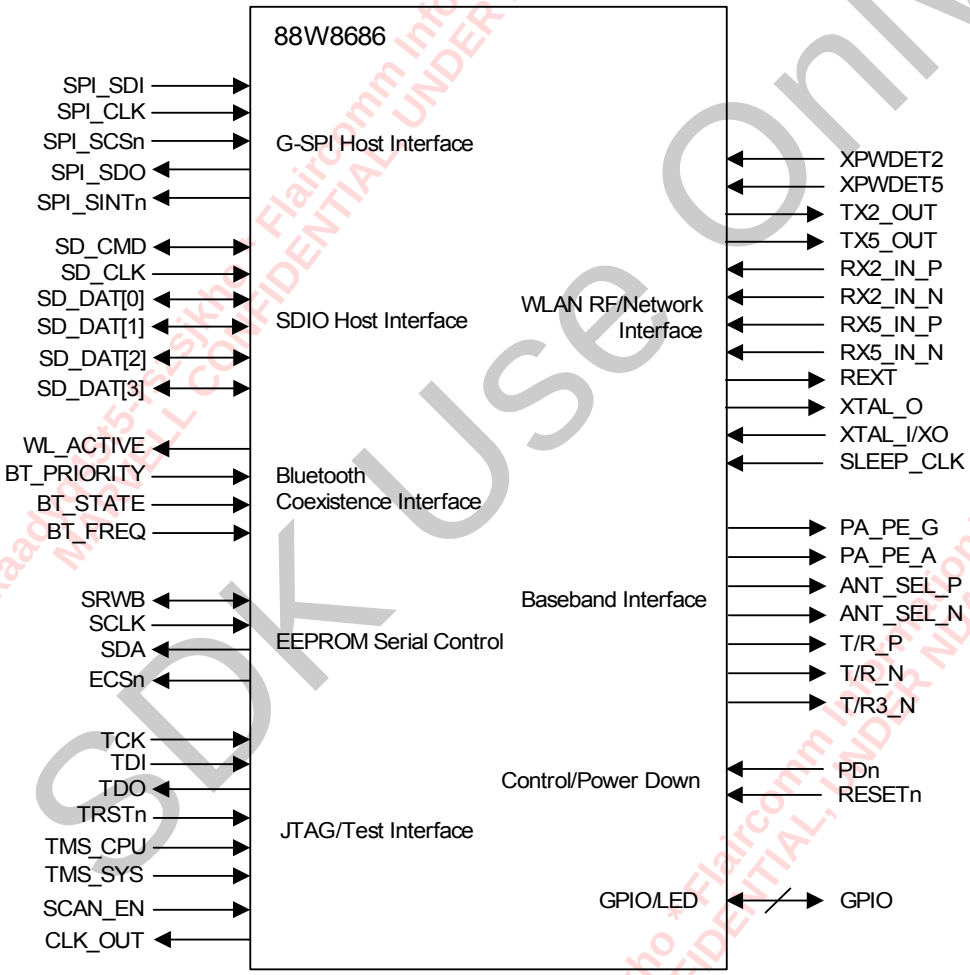
Section 1. Package and Power

1.1 Signal Diagram

Figure 2 shows a list of the signals for the device.

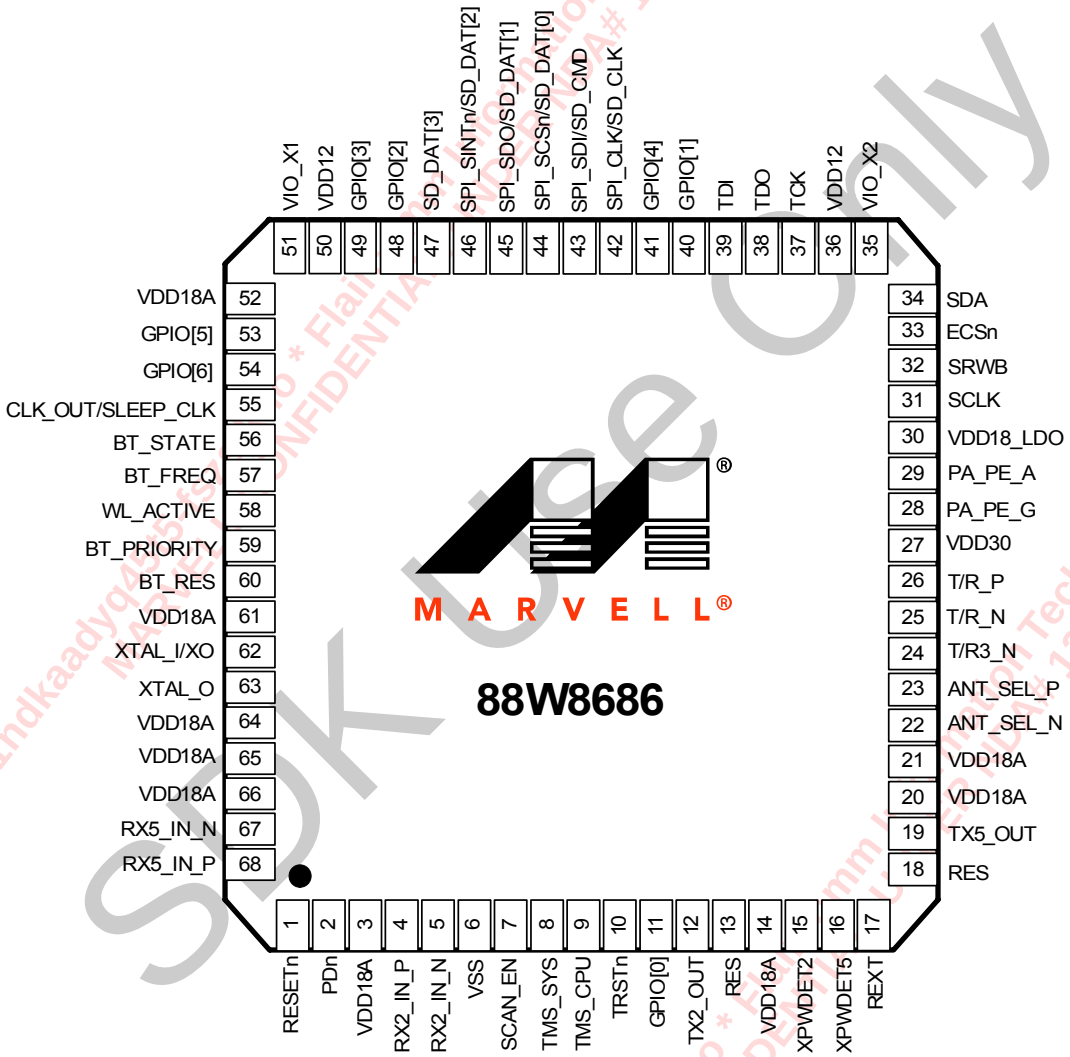
Figure 2: Signal Diagram



1.2 QFN Package

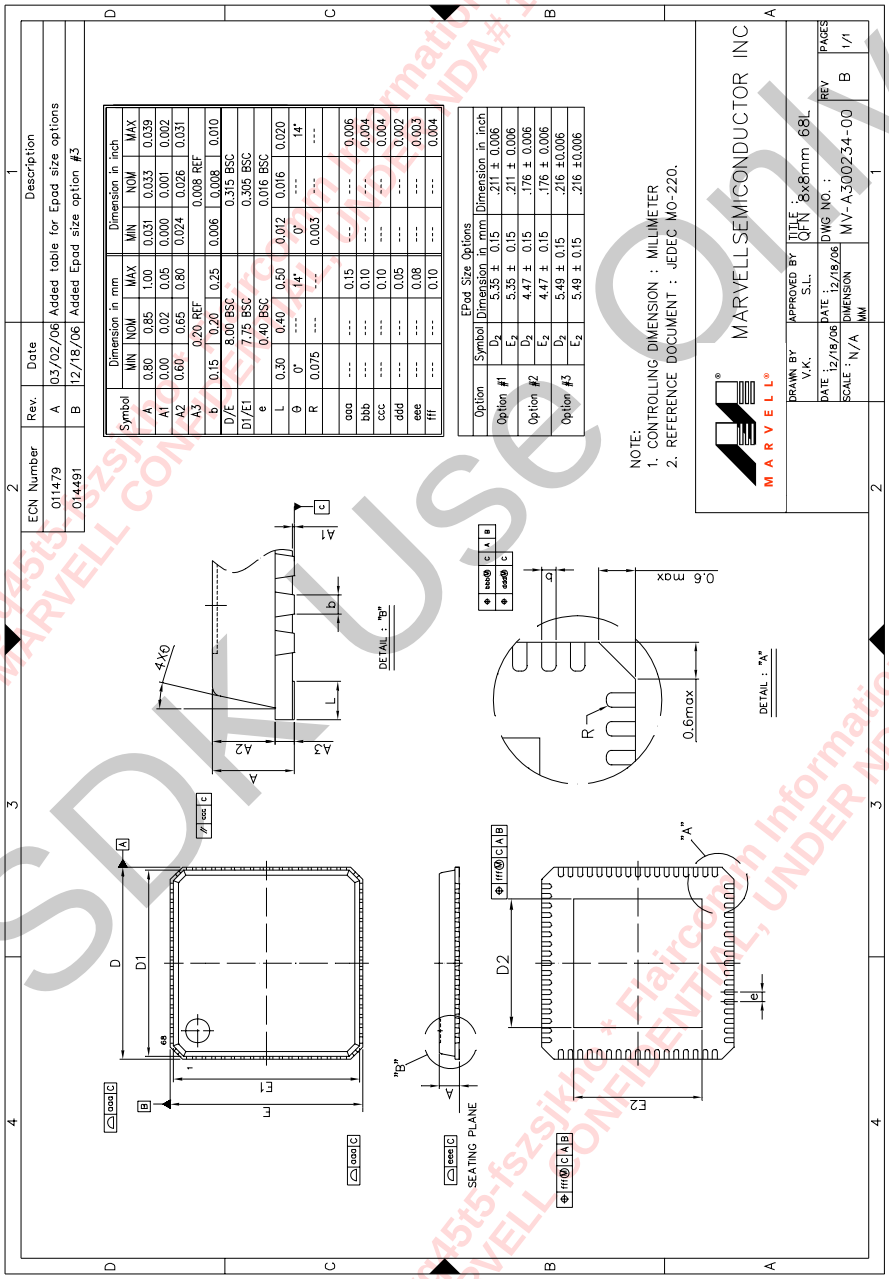
1.2.1 QFN Pinout—68-Pin

Figure 3: QFN Package Pinout—68-Pin



1.2.2 QFN Mechanical Drawing—68-Pin

Figure 4: QFN Mechanical Drawing—68-Pin



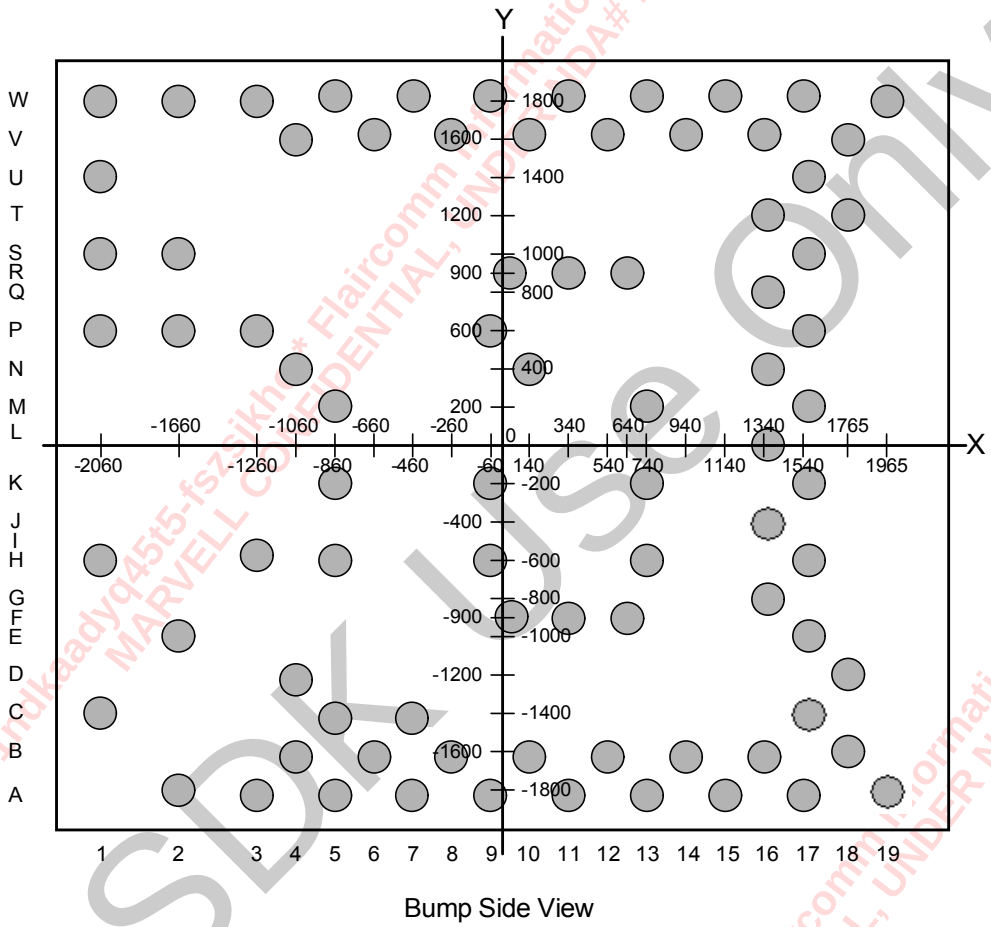
Notes

- All dimensions in mm.
- See Section 7. "Part Order Numbering/Package Marking" on page 143 for package marking and pin 1 location.
- QFN package uses Epad size option #1.

1.3 Flip Chip Packages

1.3.1 Flip Chip Package—280 µm Pitch

Figure 5: Flip Chip Pad Locations—280 µm Pitch



Bump Side View

Note

Visual aspect ratio not to scale.

Table 1: Flip Chip Locations—280 µm Pitch

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
RESETn	1	V6	-660	1625
PDn	2	V4	-1060	1600
VDD18A	3	S2	-1660	1000
RX2_IN_P	4	S1	-2060	1000
RX2_IN_N	5	P1	-2060	600
VSS	6	K5	-860	-200
SCAN_EN (VSS)	7	L16	1365	0
TMS_SYS	8	B14	940	-1625
TMS_CPU	9	B18	1765	-1600
TRSTn	10	A13	740	-1825
GPIO[0]	11	V14	940	1625
TX2_OUT	12	H1	-2060	-600
RES	13	--	--	--
VDD18A	14	E2	-1660	-1000
XPWDET2	15	A3	-1260	-1825
XPWDET5	16	A5	-860	-1825
REXT	17	B4	-1060	-1625
RES	18	--	--	--
TX5_OUT	19	A2	-1660	-1800
VDD18A	20	D4	-1060	-1225
VDD18A	21	C7	-460	-1425
ANT_SEL_N	22	A7	-460	-1825
ANT_SEL_P	23	B8	-260	-1625
T/R3_N	24	B6	-660	-1625
T/R_N	25	B10	140	-1625
T/R_P	26	B12	540	-1625
VDD30	27	F11	340	-900
PA_PE_G	28	A9	-60	-1825
PA_PE_A	29	A11	340	-1825

Table 1: Flip Chip Locations—280 µm Pitch (Continued)

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
VDD18_LDO	30	H13	740	-600
SCLK	31	A15	1140	-1825
SRWB	32	B16	1340	-1625
ECSn	33	C17	1565	-1400
SDA	34	A17	1540	-1825
VIO_X2	35	F12	640	-900
VDD12	36	K13	740	-200
TCK	37	E17	1565	-1000
TDO	38	G16	1365	-800
TDI	39	H17	1565	-600
GPIO[1]	40	J16	1365	-400
GPIO[4]	41	K17	1565	-200
SPI_CLK/SD_CLK	42	M17	1565	200
SPI_SDI/SD_CMD	43	N16	1365	400
SPI_SCSn/SD_DAT[0]	44	P17	1565	600
SPI_SDO/SD_DAT[1]	45	Q16	1365	800
SPI_SINTn/SD_DAT[2]	46	S17	1565	1000
SD_DAT[3]	47	V18	1765	1600
GPIO[2]	48	U17	1565	1400
GPIO[3]	49	V16	1340	1625
VDD12	50	K9	-60	-200
VIO_X1	51	T16	1365	1200
VDD18A	52	H5	-860	-600
GPIO[5]	53	W17	1540	1825
GPIO[6]	54	W15	1140	1825
CLK_OUT/SLEEP_CLK	55	W13	740	1825
BT_STATE	56	W11	340	1825
BT_FREQ[2]	57	V8	-260	1625
WL_ACTIVE	58	V12	540	1625
BT_PRIORITY	59	V10	140	1625

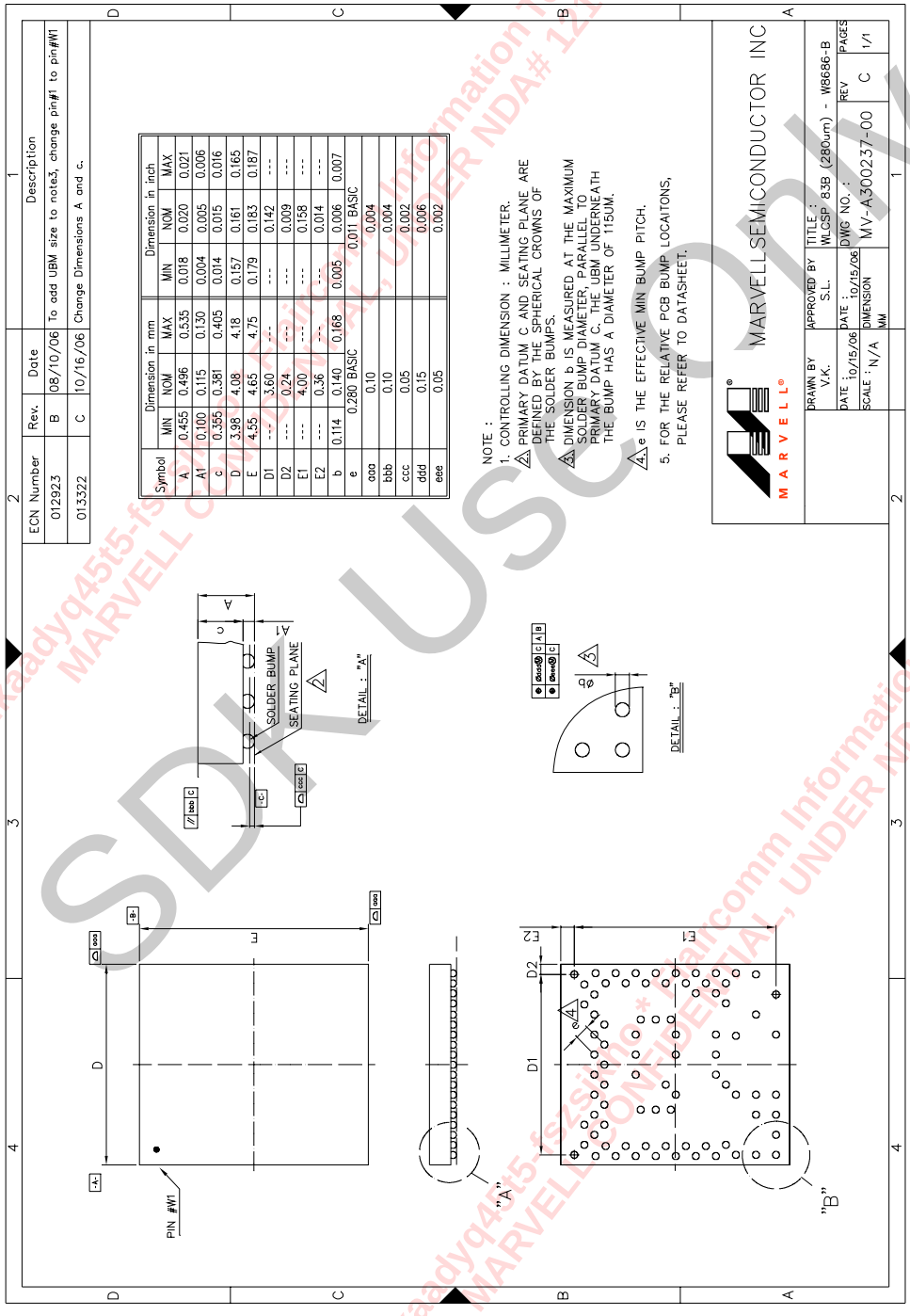
Table 1: Flip Chip Locations—280 µm Pitch (Continued)

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
BT_RES	60	W9	-60	1825
VDD18A	61	P9	-60	600
XTAL_I/XO	62	W7	-460	1825
XTAL_O	63	W5	-860	1825
VDD18A	64	R9	40	900
VDD18A	65	W3	-1260	1800
VDD18A	66	P3	-1260	600
RX5_IN_N	67	W2	-1660	1800
RX5_IN_P	68	W1	-2060	1800
GPIO[11]	--	D18	1765	-1200
GPIO[12]	--	T18	1765	1200
GPIO[13]	--	A19	1965	-1800
GPIO[14]	--	W19	1965	1800
VSS	--	C1	-2060	-1400
		U1	-2060	1400
		P2	-1660	600
		H3	-1260	-575
		N4	-1060	400
		C5	-860	-1425
		M5	-860	200
		H9	-60	-600
		F9	40	-900
		N10	140	400
		R11	340	900
		R12	640	900
		M13	740	200

1. Alphanumeric designations are approximations to the grid shown in Figure 5.
2. When not using BT_FREQ, tie to ground. See Table 7, “Bluetooth Coexistence Interface,” on page 35.

1.3.2 Flip Chip Mechanical Drawing—280 µm Pitch

Figure 6: Flip Chip Mechanical Drawing—280 µm Pitch

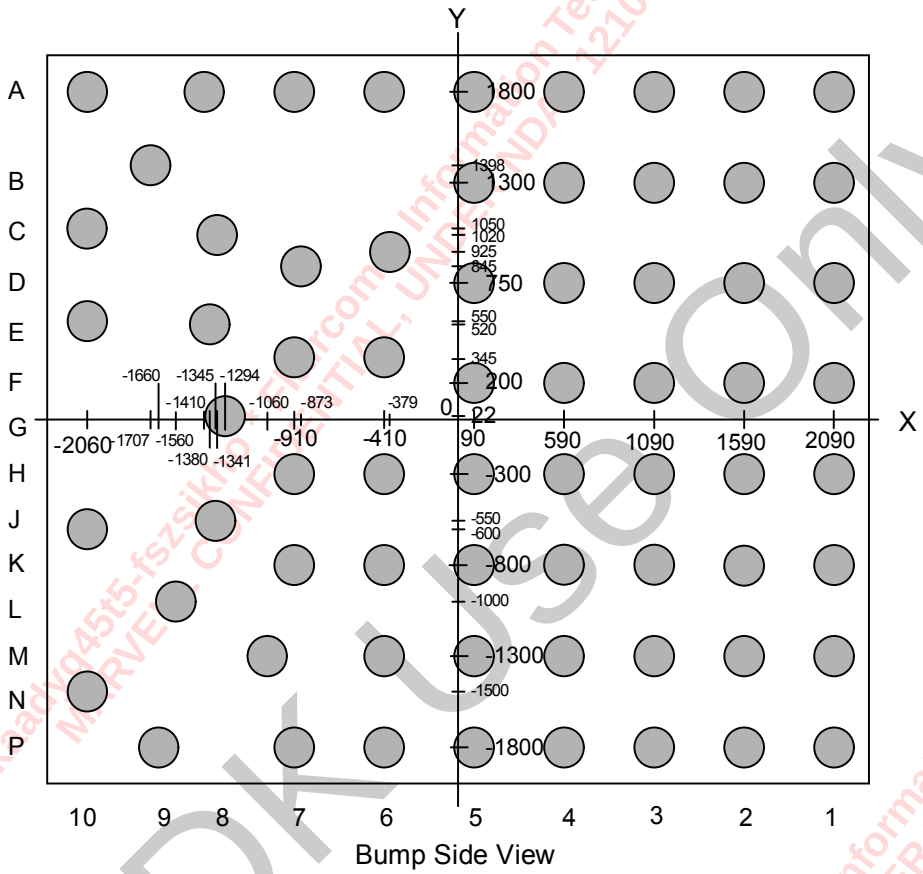


Notes

- All dimensions in mm.
- See Section 7. "Part Order Numbering/Package Marking" on page 143 for package marking and pin 1 location.

1.3.3 Flip Chip Package—500 µm Pitch

Figure 7: Flip Chip Pad Locations—500 µm Pitch



Notes

- 500 µm pitch flip chip package supports 802.11g/b applications only.
- Visual aspect ratio not to scale.

Table 2: Flip Chip Locations—500 µm Pitch

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
RESETn	1	A4	590	1800
PDn	2	A4	590	1800
VDD18A	3	B9	-1707	1398
RX2_IN_P	4	C10	-2060	1050
RX2_IN_N	5	E10	-2060	550
SCAN_EN (VSS)	7	G8	-1294	22
TMS_SYS	8	D4	590	750
TMS_ARM	9	F5	90	200
TRSTn	10	H6	-410	-300
GPIO[0]	11	F4	590	200
TX2_OUT	12	J10	-2060	-600
VDD18A	14	L9	-1560	-1000
XPWDET2	15	P6	-410	-1800
RES	16	M6	-410	-1300
REXT	17	P9	-1660	-1800
VDD18A	20	K7	-910	-800
VDD18A	21	P7	-910	-1800
ANT_SEL_N	22	M5	90	-1300
ANT_SEL_P	23	M4	590	-1300
T/R3_N	24	K5	90	-800
T/R_N	25	M3	1090	-1300
T/R_P	26	P4	590	-1800
VDD30	27	K6	-410	-800
PA_PE_G	28	P5	90	-1800
VDD18_LDO	30	K4	590	-800
SCLK	31	P3	1090	-1800
SRWB	32	M2	1590	-1300
ECSn	33	K2	1590	-800

Table 2: Flip Chip Locations—500 µm Pitch (Continued)

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
SDA	34	P2	1590	-1800
VIO_X2	35	P1	2090	-1800
VDD12	36	K3	1090	-800
TCK	37	M1	2090	-1300
TDO	38	H5	90	-300
TDI	39	K1	2090	-800
GPIO[1]	40	H1	2090	-300
GPIO[4]	41	H2	1590	-300
SPI_CLK/SD_CLK	42	F1	2090	200
SPI_SDI/SD_CMD	43	F2	1590	200
SPI_SCSn/SD_DAT[0]	44	D1	2090	750
SPI_SDO/SD_DAT[1]	45	D2	1590	750
SPI_SINTn/SD_DAT[2]	46	B1	2090	1300
SD_DAT[3]	47	B2	1590	1300
GPIO[2]	48	F3	1090	200
GPIO[3]	49	D3	1090	750
VIO_X1	51	A1	2090	1800
VDD18A	52	E6	-410	345
GPIO[5]	53	A2	1590	1800
GPIO[6]	54	B3	1090	1300
CLK_OUT/SLEEP_CLK	55	A3	1090	1800
BT_STATE	56	B4	590	1300
BT_FREQ[2]	57	E8	-1380	520
WL_ACTIVE	58	B5	90	1300
BT_PRIORITY	59	A5	90	1800
XTAL_I/XO	62	A6	-410	1800
XTAL_O	63	A7	-910	1800
VDD18A	64	D5	90	750
VDD18A	65	A8	-1410	1800

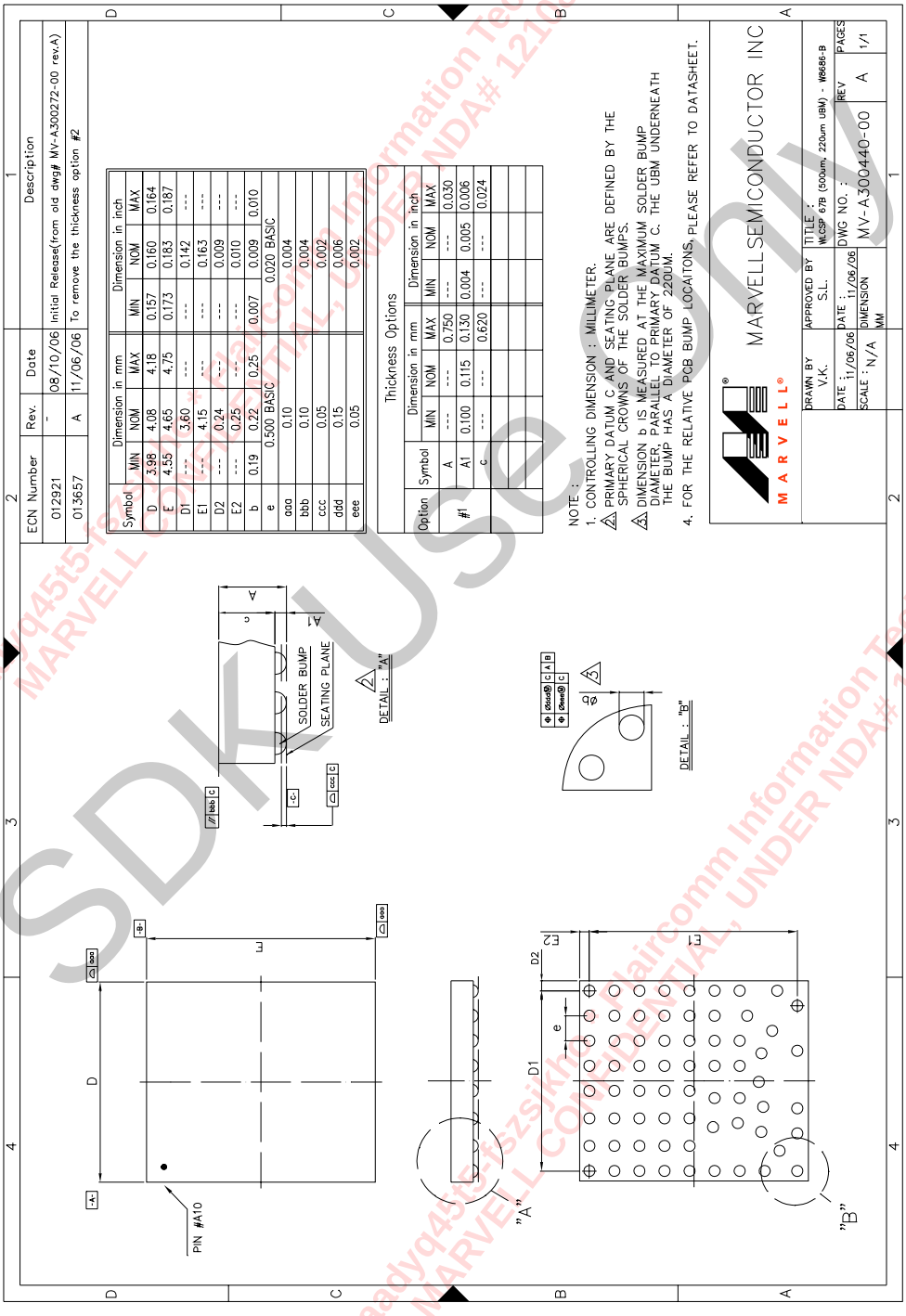
Table 2: Flip Chip Locations—500 µm Pitch (Continued)

Pin Name	68-Pin QFN #	Alpha Numeric Designation[1]	Flip Chip Pad Location Relative to Die Center (bump side)	
			X	Y
VSS	--	N10	-2060	-1500
		A10	-2060	1800
		J8	-1345	-550
		C8	-1341	1020
		M7	-1060	-1300
		H7	-910	-300
		E7	-910	345
		C7	-873	845
		C6	-379	925
		H4	590	-300
		H3	1090	-300

1. Alphanumeric designations are approximations to the grid shown in Figure 7.
2. When not using BT_FREQ, tie to ground. See Table 7, "Bluetooth Coexistence Interface," on page 35.

1.3.4 Flip Chip Mechanical Drawing—500 µm Pitch (220 µm UBM)

Figure 8: Flip Chip Mechanical Drawing–500 µm Pitch (220 µm UBM)

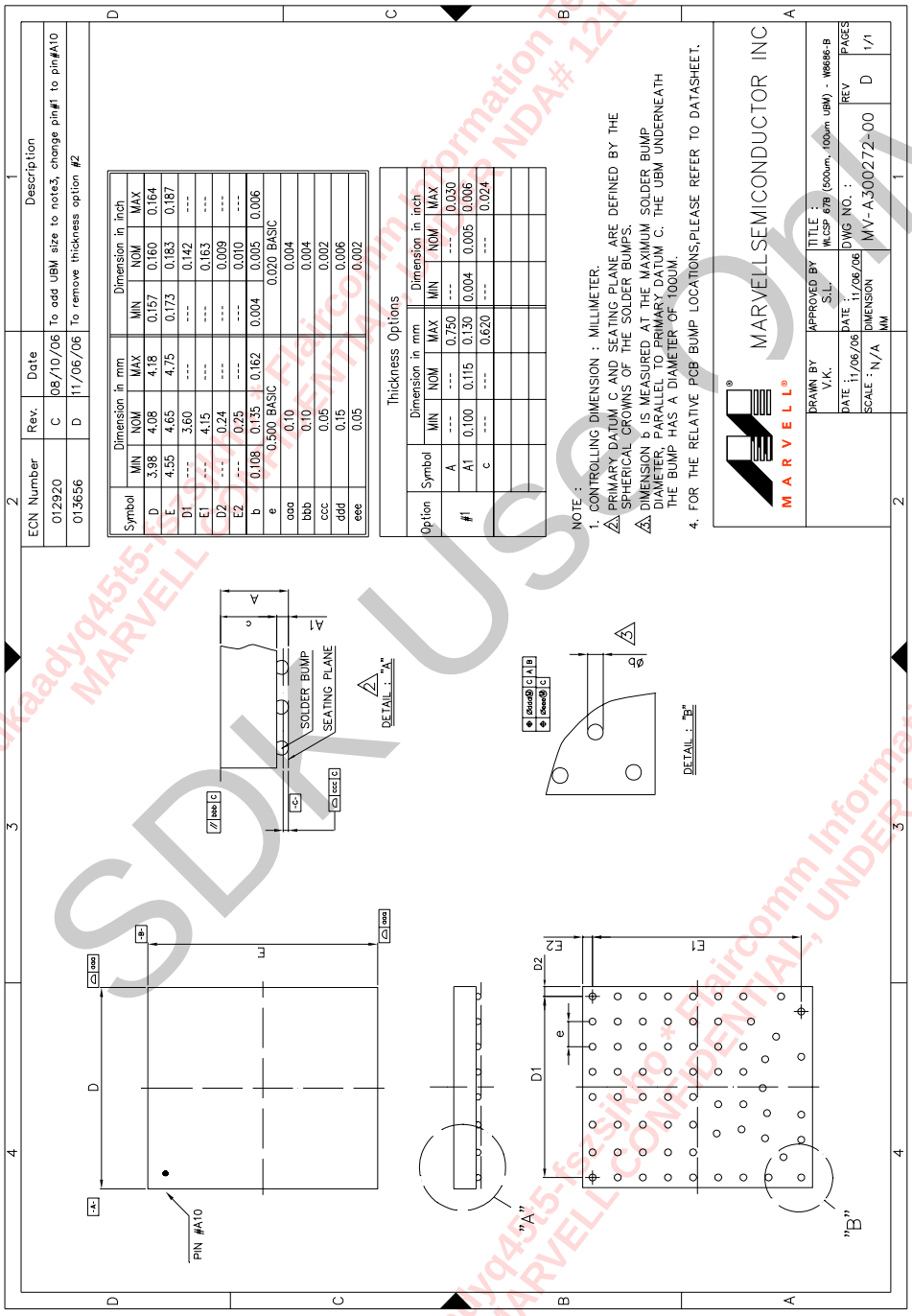


Notes

- All dimensions in mm.
- See Section 7. "Part Order Numbering/Package Marking" on page 143 for package marking and pin 1 location.

1.3.5 Flip Chip Mechanical Drawing—500 µm Pitch (100 µm UBM)

Figure 9: Flip Chip Mechanical Drawing–500 µm Pitch (100 µm UBM)



Notes

- All dimensions in mm.
- See Section 7. "Part Order Numbering/Package Marking" on page 143 for package marking and pin 1 location.

1.4 Pin Description

Table 3: Pin Types

Pin Type	Description
I/O	Digital input/Output
I	Digital input
O	Digital output
A, I	Analog input
A, O	Analog output

Table 4: WLAN RF/Network Interface

68-Pin QFN Pin#	Pin Name	Type	Description
15	XPWDET2	A, I	2.4 GHz Power Amplifier Power Detection Signal
16	XPWDET5	A, I	5 GHz Power Amplifier Power Detection Signal **NOTE:** Not available on the 500 µm flip chip package.
12	TX2_OUT	O	2.4 GHz Transmit Output Baseband in-phase output data.
19	TX5_OUT	O	5 GHz Transmit Output Baseband in-phase output data. **NOTE:** Not available on the 500 µm flip chip package.
4	RX2_IN_P	I	2.4 GHz Transmit Positive Input Baseband in-phase output data–differential positive signal.
5	RX2_IN_N	I	2.4 GHz Transmit Negative Input Baseband in-phase output data–differential negative signal.
68	RX5_IN_P	I	5 GHz Transmit Positive Input Baseband in-phase output data–differential positive signal. **NOTE:** Not available on the 500 µm flip chip package.
67	RX5_IN_N	I	5 GHz Transmit Negative Input Baseband in-phase output data–differential negative signal. **NOTE:** Not available on the 500 µm flip chip package.
17	REXT	A, O	Bias Current Resistor Used for current reference.
63	XTAL_O	O	Crystal / Crystal Oscillator Output Used only for internal oscillator mode.
62	XTAL_I/XO	I	Crystal / Crystal Oscillator / System Clock Input Accepts 19.2/20/24/26/38.4/40 MHz clock signals from a crystal oscillator (frequency stability ±20 ppm). AC coupled reference clock supported. See Section 6.6.1.1 "Input Clock Modes" on page 121.

Table 4: WLAN RF/Network Interface (Continued)

68-Pin QFN Pin#	Pin Name	Type	Description
55	CLK_OUT/ SLEEP_CLK	I	**Test Clock Mode**: CLK_OUT See Table 10, "Joint Test Action Group (JTAG) and Test Interface," on page 37. **Sleep Clock Mode**: SLEEP_CLK Clock Input for External Sleep Clock **NOTE:** SLEEP_CLK is used by the WLAN and Bluetooth MAC. The input clock frequency is typically 32 kHz/32.768 kHz/3.2 kHz. The Bluetooth radio chip supply is 3.2 kHz. The WLAN requires 32 kHz.

Table 5: Baseband Interface

68-Pin QFN Pin#	Pin Name	Type	Description
28	PA_PE_G	O	PA Power Enable Control (802.11g Mode) Controls the power amplifier enable input. 0 = disable 1 = enable
29	PA_PE_A	O	PA Power Enable Control (802.11a Mode) Controls the power amplifier enable input. 0 = disable 1 = enable **NOTE:** Not available on the 500 µm flip chip package.
23	ANT_SEL_P	O	Differential Antenna Select Positive Output Provides the antenna select positive control signal. Default value is 1. **ANT_SEL_N / ANT_SEL_P / Antenna** 0 / 0 / -- 0 / 1 / Antenna 1 1 / 0 / Antenna 0 1 / 1 / -- **NOTE:** Also used as RF switch control for single Bluetooth/WLAN antenna configurations.

Table 5: Baseband Interface (Continued)

68-Pin QFN Pin#	Pin Name	Type	Description
22	ANT_SEL_N	O	Differential Antenna Select Negative Output Provides the antenna select negative control signal. Default value is 0. **ANT_SEL_N / ANT_SEL_P / Antenna** 0 / 0 / -- 0 / 1 / Antenna 1 1 / 0 / Antenna 0 1 / 1 / -- **NOTE:** Also used as RF switch control for single Bluetooth/WLAN antenna configurations.
26	T/R_P	O	Transmit Switch Control Positive Output Connects to the Tx/Rx switch on the board (if used). Default value is 1.
25	T/R_N	O	Transmit Switch Control Negative Output Connects to the Tx/Rx switch on the board (if used) Default value is 0.
24	T/R3_N	O	Transmit Switch 3 (for 802.11a RF switch) Negative Output Default value is 1.

Table 6: Host Interfaces–G-SPI/SDIO

68-Pin QFN Pin#	Pin Name	Type	Description
42	SPI_CLK/ SD_CLK	I/O	**G-SPI Mode**: SPI_CLK G-SPI Clock Input **SDIO 4-bit Mode**: SD_CLK Clock Input **SDIO 1-bit Mode**: SD_CLK Clock Input **SDIO SPI Mode**: SD_CLK Clock Input
43	SPI_SDI/ SD_CMD	I/O	**G-SPI Mode:** SPI_SDI G-SPI Data Input **SDIO 4-bit Mode**: SD_CMD Command/Response **SDIO 1-bit Mode:** SD_CMD Command Line **SDIO SPI Mode:** SD_CMD Data Input
44	SPI_SCSn/ SD_DAT[0]	I	**G-SPI Mode:** SPI_SCSn G-SPI Chip Select Input (active low) **SDIO 4-bit Mode:** SD_DAT[0] Data Line Bit [0] **SDIO 1-bit Mode:** SD_DAT[0] Data Line **SDIO SPI Mode:** SD_DAT[0] Data Output
45	SPI_SDO/ SD_DAT[1]	I/O	**G-SPI Mode:** SPI_SDO G-SPI Data Output **SDIO 4-bit Mode**: SD_DAT[1] Data Line Bit [1] **SDIO 1-bit Mode**: SD_DAT[1] Interrupt **SDIO SPI Mode**: SD_DAT[1] Reserved
46	SPI_SINTn/ SD_DAT[2]	I/O	**G-SPI Mode:** SPI_SINTn G-SPI Interrupt Output (active low) **SDIO 4-bit Mode**: SD_DAT[2] Data Line Bit [2] or Read Wait (optional) **SDIO 1-bit Mode**: SD_DAT[2] Read Wait (optional) **SDIO SPI Mode**: SD_DAT[2] Reserved

Table 6: Host Interfaces–G-SPI/SDIO (Continued)

68-Pin QFN Pin#	Pin Name	Type	Description
47	SD_DAT[3]	I/O	**SDIO 4-bit Mode:** SD_DAT[3] Data Line Bit [3] **SDIO 1-bit Mode:** SD_DAT[3] Reserved **SDIO SPI Mode:** SD_DAT[3] Card Select (active low)

Table 7: Bluetooth Coexistence Interface

68-Pin QFN Pin#	Pin Name	Type	Description
58	WL_ACTIVE	O	Bluetooth WLAN Active **2-Wire BCA Mode**: When high, WLAN is transmitting or receiving packets. **3-Wire BCA Mode**: 0 = Bluetooth device allowed to transmit 1 = Bluetooth device not allowed to transmit In 3/4WBCA mode, the signal output is programmable and can be low during both Bluetooth Rx and Tx timeslots. This pin drives low when PDn is asserted. In WLAN sleep mode, all I/O pads are powered down. This pad will stay at a low state when in power down mode.
59	BT_PRIORITY	I	Bluetooth Priority **2-Wire BCA Mode**: When high, Bluetooth is transmitting or receiving high priority packets. **3-Wire BCA Mode**: When high, Bluetooth is requesting to transmit or receive packets.
56	BT_STATE	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx BT_STATE is used to input the Bluetooth priority and direction of traffic following the assertion of the BT_PRIORITY input.
57	BT_FREQ	I	**4-Wire BCA Mode:** Bluetooth Frequency Asserted (logic high) when the Bluetooth transceiver hops into the restricted channels defined by the coexistence mechanism. **2-Wire, 3-Wire BCA Mode:** Tie to ground (VSS).
60	BT_RES	O	Reserved Tie to ground (VSS).

Table 8: EEPROM Serial Control

68-Pin QFN Pin#	Pin Name	Type	Description
32	SRWB	I/O	Internal pull-up. Serial Interface Read/Write Control Serial interface data input for EEPROM.
31	SCLK	I	Internal pull-up. Serial interface clock output for EEPROM or power management device programming interface control.
34	SDA	O	Serial Interface Data Output for EEPROM When this pin is used as an input, the signal is latched at the rising edge of SCLK.
33	ECSn	O	Internal pull-up. EEPROM Chip Select Output (active low)

Table 9: GPIO/LED Control

68-Pin QFN Pin#	Pin Name	Type	Description
54	GPIO[6]	I/O	Internal pull-up. General Purpose Input/Output These pins are asynchronous to internal clocks. Several of these pins can be selected to perform alternate functions such as an LED controller. When not used, these pins should be left floating. **NOTE:** The number of GPIO pins is dependent upon the package. • 68-pin package has GPIO pins [6:0] • 280-µm flip chip package has GPIO pins [6:0] and [14:11] • 500-µm flip chip package has GPIO pins [6:0] • GPIO[14:11]—General GPIO • GPIO[6]—General GPIO/UART SOUT output (strap pin) • GPIO[5]—General GPIO/UART DTR output (strap pin) • GPIO[4]—WLAN MAC wake-up input/Interrupt input • GPIO[3]—General GPIO/UART DSR input • GPIO[2]—General GPIO/UART RTS output (strap pin) • GPIO[1]—LED output (strap pin) (Tx power or Rx ready LED) • GPIO[0]—external oscillator control/SLEEPn During power down sleep mode, the external crystal oscillator is disabled, and, if implemented, also powered down by GPIO[0].
53	GPIO[5]		
41	GPIO[4]		
49	GPIO[3]		
48	GPIO[2]		
40	GPIO[1]		
11	GPIO[0]		

Table 10: Joint Test Action Group (JTAG) and Test Interface

68-Pin QFN Pin#	Pin Name	Type	Description
37	TCK	I	Internal pull-up. **JTAG Mode:** JTAG Test Clock **UART Mode:** UART CTS Input
39	TDI	I	Internal pull-up. **JTAG Mode:** JTAG Test Data Input **UART Mode:** UART SINT Input
38	TDO	O	**JTAG Mode:** JTAG Test Data Output **Functional Mode:** External 5 GHz LNA Output
10	TRSTn	I	Internal pull-up. **JTAG Mode:** JTAG Test Reset (active low) **Functional Mode:** External LNA Output
9	TMS_CPU	I	Internal pull-down. JTAG Test Mode Select This input selects the CPU JTAG controller.
8	TMS_SYS	I	Internal pull-down. JTAG Test Mode Select This input selects the system JTAG controller.
7	SCAN_EN	I	Internal pull-down. Scan Enable Can be tied to ground (VSS) or left floating.
55	CLK_OUT/ SLEEP_CLK	O	**Test Clock Mode**: CLK_OUT Test Clock Output **Sleep Clock Mode**: SLEEP CLOCK See Table 4, “WLAN RF/Network Interface,” on page 31

Table 11: Control and Power Down

68-Pin QFN Pin#	Pin Name	Type	Description
2	PDn	I	Full Power Down (active low) 0 = full power down mode 1 = normal mode Connect to power down pin of host or 1.8V.
1	RESETn	I	Internal pull-up. Reset (active low)

Table 12: Power and Ground

68-Pin QFN Pin#	Pin Name	Type	Description
36	VDD12	Power	1.2V Digital Core Power Supply
50			
3	VDD18A	Power	1.8V Analog Power Supply
14			
20			
21			
52			
61			
64			
65			
66			
30	VDD18_LDO	Power	1.8V Digital I/O and Internal Voltage Regulator Power Supply
27	VDD30	Power	3.0V Digital I/O Power Supply
51	VIO_X1	Power	1.8V/3.3V Host Supply
35	VIO_X2	Power	1.8V/3.3V Digital Power Supply
6	VSS	Ground	Ground

Table 13: Reserved

68-Pin QFN Pin#	Pin Name	Type	Description
13	RES	--	Reserved Do not connect these pins. Leave these pins floating.
18	RES	--	Reserved Do not connect these pins. Leave these pins floating.
60	BT_RES	--	Reserved Tie to ground (VSS).

1.5 Power

The 88W8686 requires the following supply voltages:

- **VDD12**—1.2V Digital Core Power Supply
- **VDD18A**—1.8V Analog Power Supply
- **VDD18_LDO**—1.8V Digital I/O and Internal Voltage Regulator Power Supply
- **VDD30**—3.0V Digital I/O Power Supply
- **VIO_X1**—1.8V/3.3V Host Supply
- **VIO_X2**—1.8V/3.3V Digital Power Supply

Table 14—Table 18 list the pins operating from each voltage supply.

Table 14: VDD18A Supply

QFN Pin#	Pin Name
15	XPWDET2
16	XPWDET5

Table 15: VDD18_LDO Supply

QFN Pin#	Pin Name
56	BT_STATE
58	WL_ACTIVE
59	BT_PRIORITY
57	BT_FREQ

Table 16: VDD30 Supply

QFN Pin#	Pin Name
22	ANT_SEL_N
23	ANT_SEL_P
24	T/R3_N
25	T/R_N
26	T/R_P
28	PA_PE_G
29	PA_PE_A

Table 17: VIO_X1 Supply

QFN Pin#	Pin Name	QFN Pin#	Pin Name
1	RESETn	44	SPI_SCSn/SD_DAT[0]
2	PDn	45	SPI_SDO/SD_DAT[1]
7	SCAN_EN	46	SPI_SINTn/SD_DAT[2]
8	TMS_SYS	47	SD_DAT[3]
11	GPIO[0]	48	GPIO[2]
40	GPIO[1]	49	GPIO[3]
41	GPIO[4]	53	GPIO[5]
42	SPI_CLK/SD_CLK	54	GPIO[6]
43	SPI_SDI/SD_CMD	55	CLK_OUT/SLEEP_CLK

Table 18: VIO_X2 Supply

QFN Pin#	Pin Name	QFN Pin#	Pin Name
--[1]	GPIO[14]	32	SRWB
--[1]	GPIO[13]	33	ECSn
--[1]	GPIO[12]	34	SDA
--[1]	GPIO[11]	37	TCK
9	TMS_CPU	38	TDO
10	TRSTn	39	TDI
31	SCLK	--	--

1. Available on 280 µm flip chip package.

1.5.1 Power Supply Configurations

For flexibility, the 88W8686 integrates an on-chip voltage regulator. The VDD12 supply can be derived from this regulator.

Table 19 shows the connection configurations for the VDD18_LDO and VDD12 power supplies in various applications.

Table 19: VDD18_LDO and VDD12 Power Supply Configurations

Configuration	VDD18_LDO	VDD12
Internal voltage regulator with/without Bluetooth coexistence interface	Connected	Not connected
External 1.2V supply with/without Bluetooth coexistence interface	Connected	Connected

1.5.2 Power Management

Table 20—Table 22 list the state of the functional pins when in power down mode.

Table 20: Tri-State Floating

QFN Pin#	Tri-State (Floating)	QFN Pin#	Tri-State (Floating)
--[1]	GPIO[11]	44	SPI_SCSn/SD_DAT[0]
7	SCAN_EN	45	SPI_SDO/SD_DAT[1]
8	TMS_SYS	46	SPI_SINTn/SD_DAT[2]
9	TMS_CPU	47	SD_DAT[3]
34	SDA	49	GPIO[3]
40	GPIO[1]	55	CLK_OUT/SLEEP_CLK
41	GPIO[4]	56	BT_STATE
42	SPI_CLK/SD_CLK	57	BT_FREQ
43	SPI_SDI/SD_CMD	59	BT_PRIORITY

1. Available on 280 µm flip chip package.

Table 21: Output Low

QFN Pin#	Output Low	QFN Pin#	Output Low
10	TRSTn	33	ECSn
11	GPIO[0]	37	TCK
22	ANT_SEL_N	38	TDO
24	T/R3_N	39	TDI
25	T/R_N	48	GPIO[2]
28	PA_PE_G	53	GPIO[5]
29	PA_PE_A	54	GPIO[6]
31	SCLK	58	WL_ACTIVE

Table 22: Output High

QFN Pin#	Output High
--[1]	GPIO[12]
--[1]	GPIO[13]
--[1]	GPIO[14]
23	ANT_SEL_P
26	T/R_P
32	SRWB

1. Available on 280 µm flip chip package.

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Section 2. Processor

The 88W8686 Processor blocks include:

- Embedded CPU
- Two Channel DMA
- CPU Interrupts
- CPU Timers
- Reset Configuration

2.1 Embedded CPU

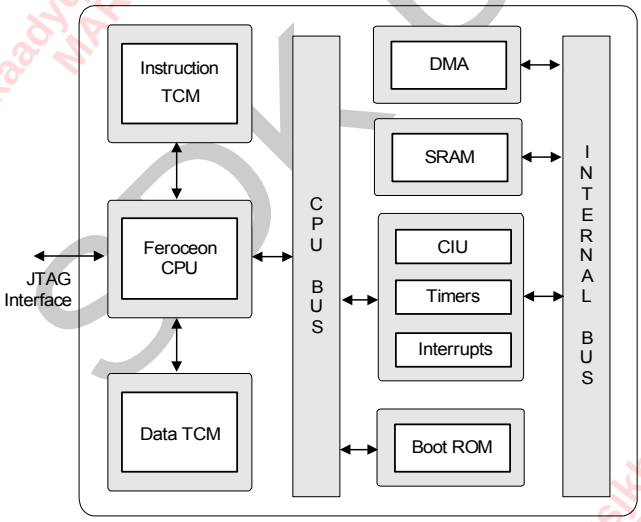
The 88W8686 contains an embedded high performance Marvell Feroceon® ARMv5TE-compliant processor.

The CPU has the following features:

- Core processor implementing the Instruction Set Architecture (ISA) Version ARMv5TE
- Tightly Coupled Memory (TCM) for Instructions and Data
- 32-bit ARMv5TE-compliant instruction set
- 32-bit data buses between the processor core and the Instruction and Data TCM

The CPU Interface Unit (CIU) functions as an interface bridge between the CPU bus and the Internal Bus. Data travels bidirectionally.

Figure 10: Embedded CPU Architecture



The 88W8686 supports TCM to store instructions and data. The Instruction TCM stores all code required for wireless applications. When the CPU executes a command, it fetches the instruction from Instruction TCM memory first.

When an instruction or data is specified within the address range of the corresponding TCM, the CPU retrieves data from the TCM. When the instruction or data cannot be found in TCM, the CPU accesses the CPU bus or the internal bus.

2.2 Two Channel DMA

The 88W8686 Direct Memory Access (DMA) controller has two independent DMA channels.

The DMA channels optimize system performance by moving large amounts of data without significant CPU intervention. Rather than having the CPU read data from one source and write it to another, the DMA channel can be programmed to automatically transfer data independent of the CPU. This frees the CPU and allows it to continue executing other instructions simultaneously with the movement of data.

The main features of the DMA controller include:

- Two independent DMA channels
- Simultaneous data transfer in different directions
- From 1 byte to 64 kB of data transfer per programmed operation
- Burst length of each transfer can be set from 1 to 32 bytes
- Non-word aligned data transfer
- Chained Mode DMA operation
- Firmware programmable DMA operation

Each DMA channel can move data between source and destination as follows:

- Source and destination both on the internal bus
- Source and destination both on the host bus
- Source and destination both on the internal bus and host bus

2.2.1 DMA Transfers

Each DMA channel uses internal buffers for moving data. Data is transferred from the source device into an internal buffer and from the internal buffer to the destination device. The DMA channel can be programmed to move up to 64 kB of data per transaction. The burst length of each transfer of DMA can be set from 1 to 32 bytes.

Accesses can be non-aligned in both the source and the destination. Data can flow in different directions through different DMA channels. The DMA channels support chained mode of operation. The descriptors are stored in memory (on internal or host bus), and the DMA channel moves the data until the Null Pointer is reached. The DMA operation can be initiated only by the CPU or host when writing a register.

2.2.2 DMA Channel Arbitration

The DMA controller has a programmable arbitration scheme between both channels. Each channel can be programmed to have priority so that a selected channel has the higher priority or to have the same priority in an alternating fashion. The DMA arbiter control register can be reprogrammed any time, regardless of the status of the channel (active or not active).

2.3 CPU Interrupts

The interrupt controller provides a simple firmware interface to the interrupt system. The internal CPU accepts two priorities of interrupt:

- Fast Interrupt Request (FIQ) for fast, low-latency interrupt handling
- Interrupt Request (IRQ) for standard interrupt handling

The IRQ and FIQ interrupts use the same interrupt source. However, two separate sets of enable set/enable clear registers are used.

The 88W8686 has a two-level interrupt scheme. In the first level of interrupt, the unit generating the event is indicated. The exceptions to this are the timer and DMA units, in which each individual timer and each DMA channel generate Level 1 interrupts. The first level interrupt registers are located on the internal CPU bus for fast access. The second level of interrupt is located within each of the units, and is used to determine which interrupt event within the unit generated the interrupt.

All Level 2 (unit level) interrupt sources to the Level 1 interrupt controller are active high and level-sensitive. Each unit interrupt can be masked at the Level 1 interrupt controller, and each individual interrupt event can be masked at the Level 2 interrupt controller.

Figure 11 shows both Level 1 and Level 2 of the interrupt scheme, and includes the details of Level 1.

Figure 12 also shows the detail of the Level 2 interrupt within most internal units. For information on the Level 2 interrupts for each host interface, contact Marvell FAEs.

Figure 11: Interrupt Diagram

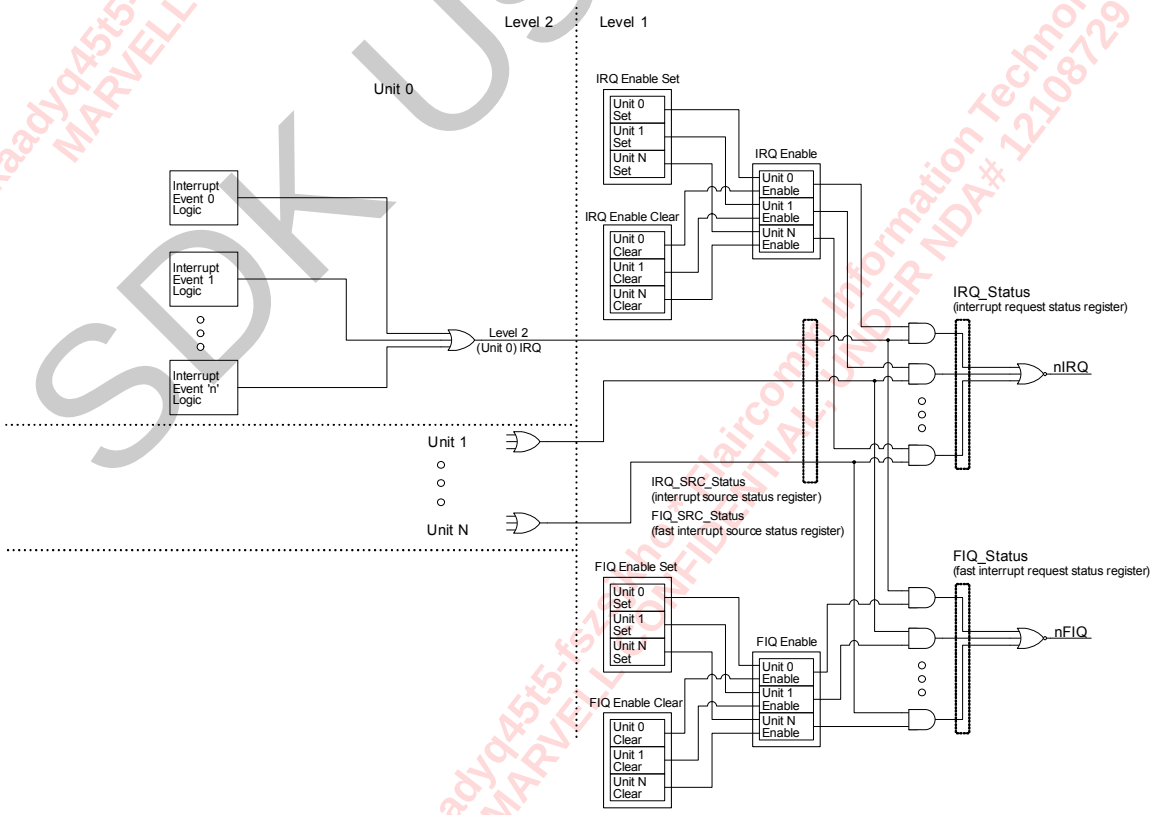


Figure 12: Level 2 Interrupt

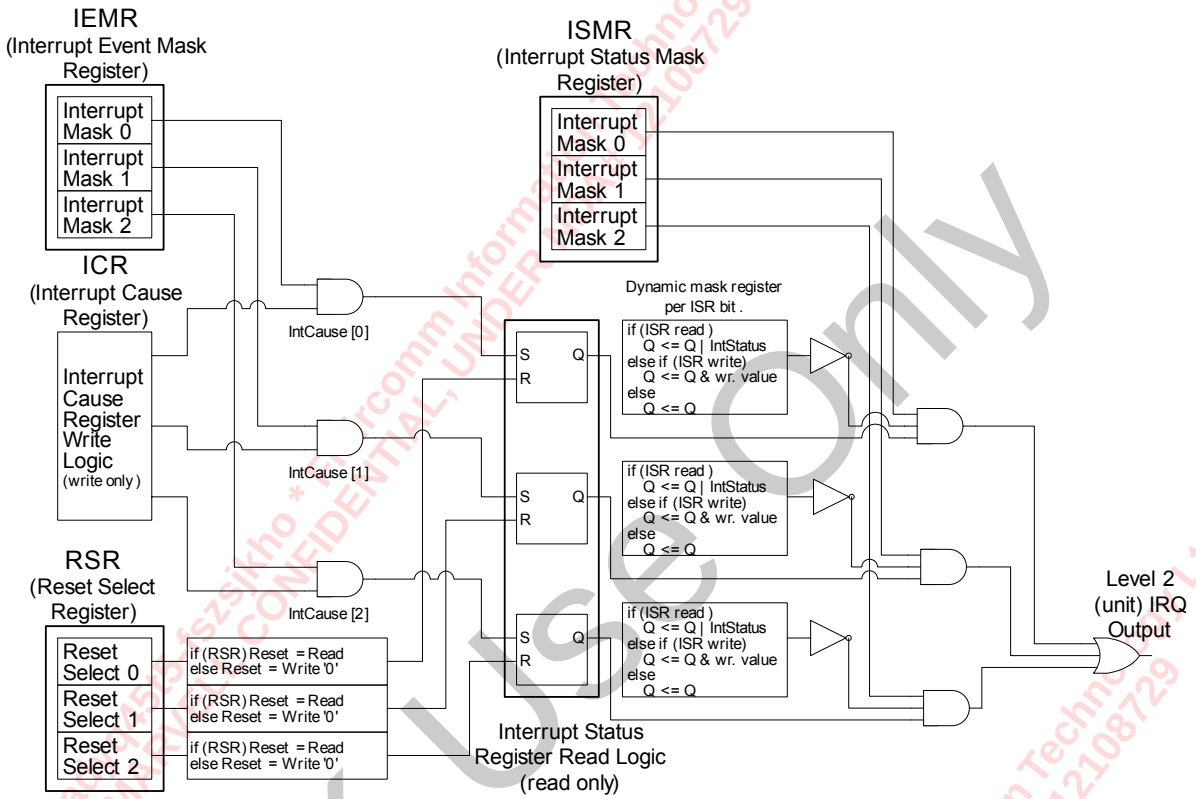


Table 23: Interrupt Register (IRQ and FIQ) Mapping in Interrupt Controller Unit

Interrupt	Interrupt Source
Intr[18]	Wireless Encryption Unit (WEU) Interrupt
Intr[17]	Internal Bus Advance Encryption Unit (AEU) Interrupt
Intr[16]	DMA Control Unit (DCU) Channel 1 Interrupt
Intr[15]	DMA Control Unit (DCU) Channel 0 Interrupt
Intr[13]	Clocked Serial Unit (CSU) Interrupt
Intr[12]	GPIO Unit (GPU) Interrupt
Intr[11]	Serial Interface Unit (UART) Interrupt
Intr[10]	WLAN MAC Control Unit (MCU) interrupt
Intr[8]	Host Interface Unit (HIU) Interrupt
Intr[7:4]	General Purpose Timer Unit (RTU) Interrupt
Intr[3]	CommTx Interrupt
Intr[2]	CommRx Interrupt
Intr[1]	Firmware Enabled Programmed Interrupt

2.4 CPU Timers

Four timers are defined within the 88W8686 device. These timers are for general use by the CPU.

Each timer is a 16-bit wide down counter with an enable signal derived from either a 1 kHz clock or 1 MHz clock, with a resolution of 1 ms and 1 µs, respectively.

- Timer 1 is the slow timer with 1 kHz input.
- Timer 2, Timer 3, and Timer 4 are the fast timers with 1 MHz input.

The reference clock to the RTU is 29.35 MHz, and the RTU uses a prescaler logic to generate 1 kHz and 1 MHz for internal timer usage.

Two modes of operation are available: periodic and one-shot.

- In periodic timer mode, counter generates an interrupt at a constant interval.
- In one-shot mode, timer only generates one interrupt when it reaches 0.

The interrupt signals also feed into the interrupt controller to produce FIQs and IRQs.

2.4.1 Timer Operation

Timer operation is described in the following steps.

1. Timer is loaded and, when enabled, counts down to 0.
2. Upon reaching 0, an interrupt is generated.
3. If timer is in the periodic mode after reaching a 0 count, it reloads its initial value and continues to decrement. Otherwise, it remains at 0 until a firmware reset is issued.

The interrupts can be masked.

2.5 Reset Configuration

The 88W8686 is reset to its default operating state under the following conditions:

- Power-on reset
- Software/Firmware reset

2.5.1 Internal Reset

The 88W8686 device is reset and the internal CPU begins the boot sequence when any of the following internal reset events occurs:

- Device receives power and VDDL supplies rises (this triggers internal POR circuit)
- Internal CPU issues a software reset
- Host driver issues a soft reset
- Watchdog timer expires (used for debug purposes only)

2.5.2 External Reset

The 88W8686 device is reset and the internal CPU begins the boot sequence when the RESETn input pin transitions from low to high.

2.5.3 Calibration

The 88W8686 performs calibration when the device is powered up. In addition, calibration is also performed under the following operating conditions:

- Exiting receive mode
- Exiting transmit mode
- Change of channel frequency

2.5.4 Configuration Pins

The 88W8686 uses the following pins as configuration inputs to set parameters following a reset. The definition of these pins changes immediately after reset to their usual function. To set a configuration bit to 0, attach a 100 kΩ resistor from the appropriate pin to ground. No external circuitry is required to set a configuration bit to 1.

Table 24: Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[12:10]	GPIO[5] GPIO[6] TDO	XOSC Frequency Select 000 = reserved 001 = 26 MHz 010 = 19.2 MHz 011 = 38.4 MHz 100 = 20 MHz 101 = 24 MHz 110 = 40 MHz 111 = 38.4 MHz (default)
CON[6:5]	SCLK ECSn	Firmware Boot ROM 00 = boot from UART 01 = reserved 10 = boot from SPI EEPROM 11 = boot from host interface bus (default)
CON[3]	T/R_N	Core Voltage Supply Source Indicator Read by firmware.
CON[1:0]	ANT_SEL_N PA_PE_G	Host Interface 00 = G-SPI 01 = reserved 10 = reserved 11 = SDIO

Section 3. Network Functions

This section provides information about the following Network function blocks and features:

- Wireless LAN
- Networking Coexistence

3.1 Wireless LAN

3.1.1 WLAN Medium Access Controller

With the embedded CPU, the 88W8686 WLAN Medium Access Controller (MAC) provides all the required functions, plus many optional features of the IEEE 802.11 standard.

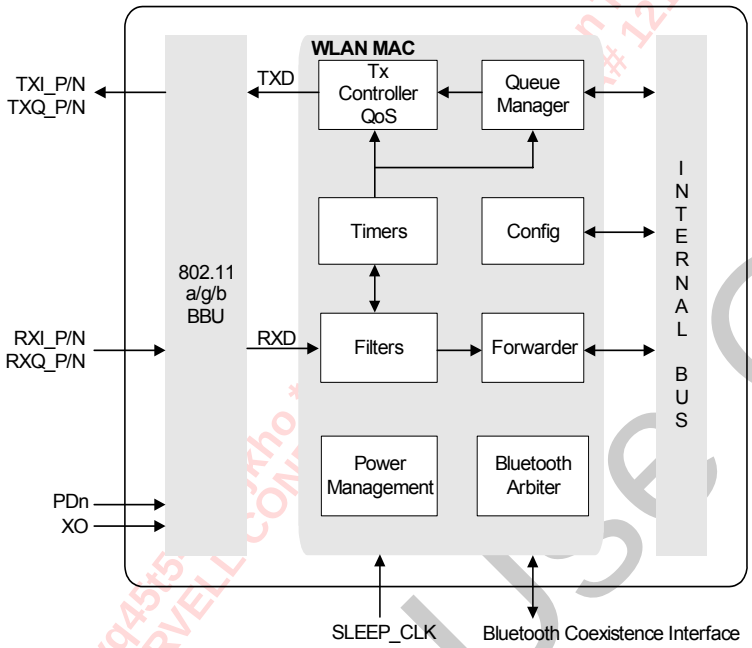
The 88W8686 WLAN MAC provides:

- Frame exchange at the MAC level to deliver data
- Received frame filtering and validation (Cyclic Redundancy Check (CRC))
- Generation of MAC header and trailer information (MAC Protocol Data Units (MPDUs))
- Fragmentation and defragmentation of data frames (MAC Service Data Units (MSDUs))
- Fair access to the shared wireless medium through the following access methods:
  - Distributed Coordination Function (DCF)
  - Point Coordination Function (PCF)
  - Enhanced Distributed Channel Access (EDCA)
- Quality of Service (QoS) compliant to the WMM and draft IEEE 802.11e standards
- Management Information Base (MIB) support
- Power Management
- Auto Rate Adaptation
- Dynamic Frequency Selection

3.1.1.1 Data Flow

Figure 13 shows a simplified block diagram of the major blocks of the WLAN MAC.

Figure 13: WLAN MAC Block Diagram



- **Baseband Processor interface—**used in communication with the BBU during transmission and reception of MAC frames.
- **Internal Bus interface**—allows the MAC to access shared memory and allows the MAC to be configured by the local CPU.
- **Bluetooth Arbitration interface**—used for Bluetooth coexistence.

The Timers block generates the internal clocks that support MAC transmit and receive operations. In addition, it supports the power down and low power modes.

The Configuration block allows access to configurable MAC functions.

3.1.1.1.1 Receive Path

On the receive path, MAC frames received over the wireless medium are passed to the MAC through the BBU interface. The major block on the receive path is the Filters block, which extracts address, timing, and frame type information from received frames and notifies the appropriate blocks. It performs validation of received frames.

3.1.1.1.2 Transmit Path

On the transmit path, data from the host system is queued in memory by the local CPU. The MAC retrieves data for transmission at the appropriate time.

The major blocks on the transmit path are:

- Queue Manager block—fetches and processes data coming from the local CPU
- Tx Controller block—implements the logic necessary to support DCF, PCF, and EDCA access methods and it responds to requests to transmit MAC frames over the wireless medium

3.1.1.2 Beaconing

For reliable communication to occur over the wireless medium, the stations (clients) in a Basic Service Set (BSS) must synchronize to a common time base. A Beacon frame is sent periodically to implement the Timing Synchronization Function (TSF) among the associated stations and to inform stations of impending traffic.

The Beacon frame is scheduled to occur regularly at the Target Beacon Transmission Time (TBTT). However, because the Beacon is a frame like all other frames, the Beacon frame must compete for the medium and may not be transmitted at the appointed TBTT.

3.1.1.2.1 Beaconing in an Independent BSS

In an Independent Basic Service Set (IBSS), the synchronization mechanism is distributed among the stations in the BSS. The mobile station that starts the BSS resets its TSF timer to 0 and transmits a Beacon, choosing a Beacon period. This process establishes the basic time base for the BSS.

When the TBTT is reached, each station in the IBSS attempts to send a Beacon frame. However, each station relies on a random delay value after the TBTT to transmit its Beacon frame.

If the station receives a Beacon frame from another station before the delay expires, the receiving station cancels its Beacon transmission. If the station does not receive a Beacon frame before the delay expires, the Beacon frame is transmitted as scheduled.

In an IBSS, a station updates its TSF timer from the received Beacon frame only when the received value is greater than the current value in the TSF timer station. This rule ensures that the faster timer value is spread throughout the BSS.

3.1.1.2.2 Beaconing in an Infrastructure BSS

In an infrastructure BSS, the AP (Access Point) is responsible for transmitting the Beacon frames regularly. The AP attempts to transmit the Beacon frame at the TBTT.

Since the Beacon frame must compete for the medium like other frames, it can be delayed beyond the TBTT due to other traffic and backoff delays. In addition, because the Beacon frame is sent to a broadcast address, it is not retransmitted in case of errors. Regardless of timing or transmission errors of a previous Beacon frame, the AP attempts to send the following Beacon frame at the next TBTT.

3.1.1.3 Frame Exchange

The 802.11 MAC frame exchange protocol requires the participation of all stations in the WLAN. This requirement means that all stations decode and react to the information in the MAC header of every frame they receive. The 802.11 MAC relies on a frame exchange protocol in which the source of the frame is allowed to determine whether the frame has been successfully received at the destination.

Although about thirty frames are defined for the 802.11 WLAN MAC, basic frame exchange is described below. In environments with low demand for bandwidth, the minimum frame exchange consists of two frames:

- Frame sent
- Frame acknowledgement

If the source does not receive acknowledgement, the source attempts to retransmit the frame. The frame and its acknowledgement are an atomic unit of the MAC protocol. They are not to be interrupted by any other station.

In environments with high demands for bandwidth, four frames are used.

- Request to Send (RTS)
- Clear to Send (CTS)
- Frame sent
- Frame acknowledgement

The source sends an RTS to the destination, and the destination sends a CTS back to the source. When the source receives the CTS frame, it sends the frame pending following an SIFS interval. When the destination receives the frame correctly, the destination returns an acknowledgement. This 4-way exchange is an atomic unit of the MAC protocol.

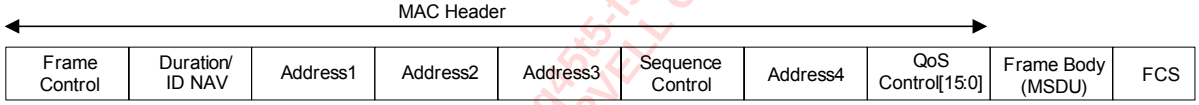
3.1.1.3.1 Frame Format

The IEEE 802.11a/g/b frame format requires up to four addresses depending on frame type. A particular frame type can contain one, two, three, or four address fields. The position of the address in the address fields determines its function. Addresses are specified according to the 802.11a/g/b standard as a collection of 6 bytes. The types of addresses defined for the WLAN are:

- Transmitter Address (TA)—identifies the MAC that transmitted the frame onto the wireless medium. The TA is used by stations to identify the MAC to which they need to send a response.
- Receiver Address (RA)—identifies the MAC receiving a frame over the wireless medium.
- Source Address (SA)—identifies the MAC that originated the frame. This address does not always match the TA address because of the indirection that is performed by the Distribution System. The SA field should be used to indicate that a frame has been received to higher layer protocols.
- Destination Address (DA)—identifies the final destination address where the frame is sent. This address does not always match the RA address because of the indirection performed by the Distribution System.
- In an infrastructure BSS, the MAC address of the AP is used as the Basic Service Set ID (BSSID). This is a unicast address.

The 88W8686 supports QoS frames as specified in the WMM and draft IEEE 802.11e standards.

Figure 14: IEEE 802.11a/g/b Frame Format



3.1.1.3.2 Lifetime and Retry Counters

Lifetime and retry counters limit the number of times that a frame can be retransmitted. When the MAC determines that it is no longer required to transmit a frame, the transmission of the frame is cancelled, and the host driver is notified by the local CPU.

3.1.1.4 Fragmentation

The MAC can fragment a frame to increase the probability that the frame is delivered without errors in the presence of interference.

A frame is divided into one or more fragments equal to the length of the fragmentation threshold. No more than one fragment smaller that the fragmentation threshold is generated. When a frame is fragmented, the sequence control field in the frame header indicates the placement of the individual fragment among the set of fragments.

The lowest numbered fragment is transmitted first. Subsequent fragments are transmitted immediately after acknowledgement of the previous fragment is received. This process is known as a fragment burst. If a fragment is not acknowledged, the normal rules of frame retransmission apply.

3.1.1.5 Access Mechanism

The 802.11 MAC is a Carrier Sense Multiple Address/Collision Avoidance (CSMA/CA) "listen before talk" access mechanism. It relies on the physical carrier sense from the Physical Layers (PHY) and the virtual carrier sense implemented in the Network Allocation Vector (NAV) of every frame to determine the state of the medium.

The decision of a station that the medium is idle is based on timing intervals. The timing intervals are kept current through the NAV. The WLAN MAC recognizes five timing intervals, shown in Table 25.

Table 25: MAC Timing Intervals

Timing Interval	Description
SIFS	Short Interframe Space Shortest interval; determined by the PHY.
Slot Time	Slot Time Determined by the PHY.
PIFS	Priority Interframe Space The PIFS is equal to the SIFS plus one slot time.
DIFS	Distributed Interframe Space The DIFS is equal to the SIFS plus two slot times.
EIFS	Extended Interframe Space The EIFS is larger than the other intervals. It allows the frame exchange to complete correctly when the received frame contains errors.
AIFS	Arbitration Interframe Space

3.1.1.5.1 DCF Operation

DCF operates during the contention-based period (CBP) when all stations are competing for access to the medium. The following steps describe a CBP session.

1. MAC receives a request to transmit a frame.
2. Physical and virtual carrier sense mechanisms are checked.
3. When both mechanisms indicate medium is idle for a DIFS or EIFS (in case of errors) interval, MAC begins transmission of frame. Transmitter must also make sure that backoff process, which was started at the end of previous transmission, is completed.
4. When MAC detects medium to be idle through both physical and virtual sensing mechanisms, MAC decrements backoff value by one slot time.
5. When transmission is not successful (no acknowledgement received), a new backoff interval is selected, and backoff countdown is begun again.
6. Once backoff interval has expired, MAC begins transmission.

This process continues until transmission is successful or is cancelled.

3.1.1.5.2 PCF Operation

The PCF operates as a poll and response function during a period known as the Contention-Free period (CFP). During the CFP, the Point Coordinator (PC) has complete access to the medium, and the DCF is prevented from gaining access. The CFP alternates with the CBP.

The following steps describe a CFP session.

1. PC gains access to medium.
2. PC begins to deliver traffic to stations in its infrastructure BSS following a beacon transmission containing a DTIM element.
3. PC polls stations on its polling list.
4. When a station polled has traffic to send, it can send one frame for each CF_Poll frame it received.
5. When a station does not have traffic to send, it does not respond to the poll.
6. PC announces the end of CFP by transmitting a contention-free end (CF_End) frame.

CF_End frame causes all stations that had their NAVs set from the initial Beacon frame to reset the NAV. At this time, the stations are able to compete for access to the medium under DCF operation.

3.1.1.6 Quality of Service

In addition to the Contention-Free Queue (CFQ) to support the IEEE 802.11e QoS function, the 88W8686 includes the queues shown in Table 26. The queue priority is listed in descending order, which is observed during the CFP. During a CFP, the CFQ has the highest priority.

Table 26: QoS Queues

Queue	Description
CMQ	Control/Management Queue
BWQ	Bandwidth Allocation/Request Queue
TCQ[7]	Traffic Category Queue 7
TCQ[6]	Traffic Category Queue 6
TCQ[5]	Traffic Category Queue 5
TCQ[4]	Traffic Category Queue 4
TCQ[3]	Traffic Category Queue 3
TCQ[2]	Traffic Category Queue 2
TCQ[1]	Traffic Category Queue 1
TCQ[0]	Traffic Category Queue 0

3.1.1.6.1 Backoff

During the contention-based periods, backoff periods are invoked, each using its set of CWMin, CWMax, and AIFS periods as specified in clause 9.2.5.2 of IEEE 802.11e. The CMQ and the BWQ use the AIFS 7 time and do not have a backoff.

3.1.1.7 Management Information Base

The 88W8686 WLAN MAC supports management and troubleshooting operations for network infrastructure devices. The device constructs Management Information Base (MIB) parameters as defined in part 11.4 of the IEEE 802.11 specification.

3.1.1.8 Power Management

The 88W8686 Power Management Unit (PMU) controls the state of the 802.11a/g/b RF radio, baseband, and the Time Base Generator (TBG) blocks of the 88W8686.

The PMU supports the following functions:

- Standby mode for the integrated 802.11a/g/b BBU
- Standby and power down modes for the 802.11a/g/b RF radio
- Power down mode
  - Internal PLL and external oscillator shut down
  - Wake on GPIO interrupt or wake-up timer or host interface command
- Shut down of the RF radio and baseband without entering power save mode (PSM)
- Low frequency clock calibration
- External power down
- External sleep clock

The power management function allows stations in either an IBSS or a BSS to enter a low power mode of operation. Because of the differences in operation between an IBSS and the infrastructure BSS, two mechanisms for power management have been developed.

3.1.1.8.1 Power Management in an Independent BSS

In an IBSS, power management is controlled by the individual mobile stations. It is implemented through a Beacon frame and a time interval called the Announcement (or Ad Hoc) Traffic Indication Message window. The Announcement Traffic Indication Message (ATIM) governs the time a station must remain awake to accept traffic.

3.1.1.8.1.1 Station in Low Power Mode

For a station to enter a low power mode, a station must complete a frame handshake with another station with power management set in the frame header. Until the handshake is completed, the station must remain in the awake state.

When the handshake is completed, the station may enter a low power mode. However, the following restrictions apply to the station while in a low power mode.

- Station must wake-up to receive every Beacon transmission.
- Station must stay awake for a period of time (ATIM window) after each Beacon.
- If power saving station receives a frame during ATIM window, it must acknowledge the frame and remain awake until end of the next ATIM window.
- If power saving station receives a multicast frame during ATIM window, it must remain awake until the end of the next ATIM window.
- All stations that send a Beacon frame must not enter power save mode until they receive a Beacon frame from another station in the BSS. This restriction ensures that there is at least one station in the IBSS that is awake and able to respond to requested frames.

3.1.1.8.1.2 Sending Station

The sending station supports functions to communicate with a station in a low power mode. It is required to assess the power saving state of the destination. Sending stations must buffer the frames to be sent to the destination in low power mode until the destination awakens and acknowledges the ATIM frame.

- Sending station sends a frame to announce a data frame to a specific destination and/or multicast frames during the ATIM window.
- For a specific destination, the sending station cannot transmit its frame until after it has received an acknowledgement from the destination.
- When acknowledgement is received from a destination, sending station sends corresponding data frame after the end of the ATIM window.
- For multicast frames, no acknowledgement is expected. Sending station can send multicast frame after the end of the ATIM window.

3.1.1.8.2 Power Management in an Infrastructure BSS

In an infrastructure BSS, the power management mechanism is centralized in the AP. It is implemented through frame exchange and specific information transmitted in the Beacon frame. The Beacon frame indicates whether a station has buffered frames or buffered multicast frames are pending. The Delivery Traffic Indication Map (DTIM) governs the time a station must remain awake to accept multicast frames.

3.1.1.8.2.1 Station in Low Power Mode

In a infrastructure BSS, a station is not required to wake-up for each Beacon frame. Frame exchange is used to communicate with the AP on the station's status.

- Station must complete a successful handshake with the AP with power management set to inform the AP when the station enters the low power mode.
- Station must send the AP the number of Beacon periods that the station is in low power mode through its association request frame.
- Station must send a power save poll (PS_Poll) frame to the AP to request frames buffered by the AP while station was in low power mode.

3.1.1.8.2.2 Access Point

The AP is responsible for buffering data frames for stations in power saving mode and delivering frames to stations when they wake-up and make a request. The steps below describe AP functions that support power management.

- AP buffers data frames for each station in low power mode.
- AP buffers multicast frames when it has any associated stations that are in low power mode.
- When AP buffers frames for a station in low power mode, the AP sets the Association ID (AID) in the Traffic Indication Map (TIM) for the corresponding station in each Beacon frame transmitted.
- When AP buffers multicast frames, the special AID bit is set to indicate buffered multicast frames are pending.

Buffered multicast frames are sent immediately after the Beacon frame announcing the DTIM. When more than one buffered multicast frame is pending, the more data bit is set in the frame control field.

After the transmission of buffered multicast frames, the AP sends frames to active stations and delivers buffered frames for those stations that make a request.

3.1.1.8.3 Power Save Mode

Power save mode (PSM) implementation in the 88W8686 is achieved through the coordination of the driver, firmware, and hardware. See the Power Management Architecture document for details.

3.1.1.8.4 External Power Down

The PDn pin controls the external full power down with an internal pull-up resistor.

3.1.1.8.5 Sleep Clock

The sleep clock used by the PMU during power save modes can be generated by an internal clock source or provided from an external clock source. When an external sleep clock source is used, the internal sleep clock can be disabled to save power.

3.1.1.9 Auto Rate Adaptation

When enabled, auto rate adaptation automatically drops the data rate for packet transmissions. This happens after the first attempt. If it fails, the MAC retries the frames with a lower data rate to improve the likelihood of a successful transmission.

3.1.1.10 Dynamic Frequency Selection

The IEEE 802.11 standards govern two different frequency ranges. 802.11g/b products operate within the 2.4 GHz range, and 802.11a products operate within the 5 GHz range. Because different countries around the world have allocated portions of the 5 GHz range to radar applications in addition to Wi-Fi, WLAN devices are required to detect the presence of radar pulses when operating in the 5 GHz range, and change channels when a conflict is detected. The 802.11 standard includes provisions for APs to inform wireless clients of the appropriate channel for local usage.

Dynamic Frequency Selection (DFS) for the 5 GHz range is covered by the IEEE 802.11h standard and FCC requirements.

The 88W8686 WLAN MAC supports DFS by accepting DFS pulse data from the baseband unit and storing that data into the DFS queue for software interpretation.Software is notified of a DFS pulse arrival through interrupts.

3.1.2 WLAN Baseband

The 88W8686 Baseband Processor Unit (BBU) is compliant to the IEEE 802.11 specification. The BBU supports Orthogonal Frequency Division Multiplexing (OFDM) multicarrier modulation for both 2.4 GHz and 5 GHz radio bands. In addition, it supports Direct Sequence Spread Spectrum (DSSS) Inphase/Quadrature (I/Q) modulation for the 2.4 GHz band specified in the IEEE 802.11b standard.

To ensure the best performance under severe multi-path and interference conditions, the BBU implements advanced digital signal processing techniques. On the receive path, the 88W8686 includes soft Viterbi decoding, coarse and fine frequency offset adjustment, and channel adaptation to the incoming signal.

The 88W8686 includes on-chip A/D and D/A converters for precision encoding/decoding of all modulation modes.

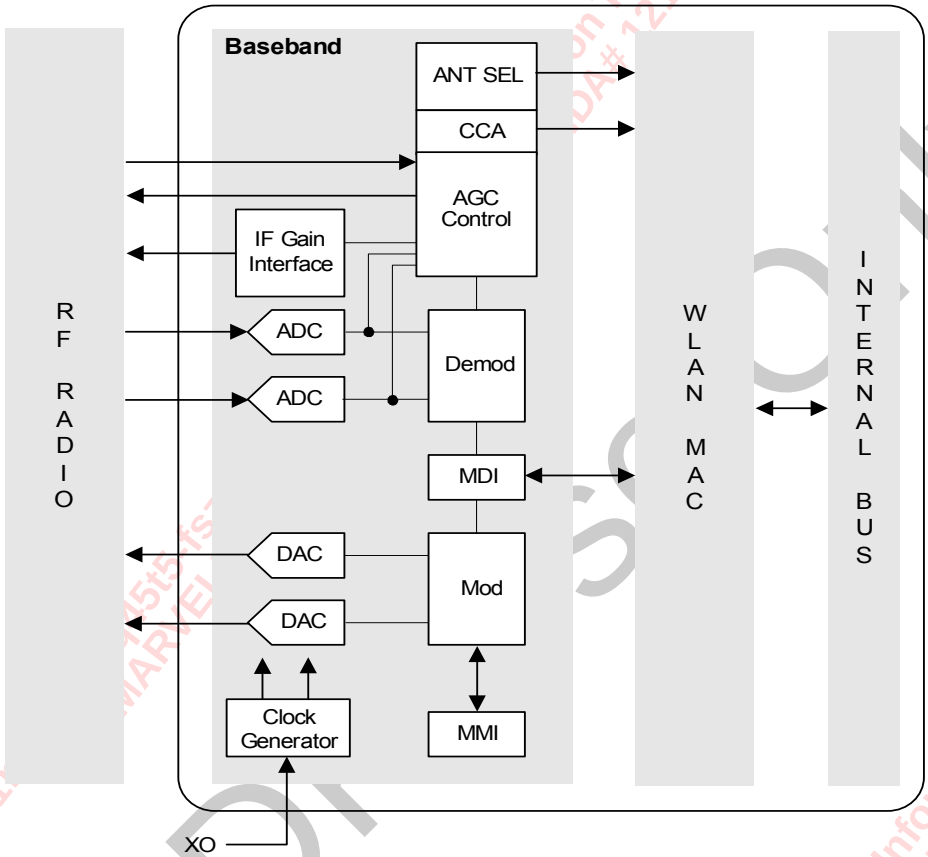
The BBU supports:

- Full implementation of IEEE 802.11a/g/b OFDM/DSSS PHY specification
- 802.11/802.11b data rates of 1, 2, 5.5, and 11 Mbps
- 802.11a/g data rates of 6, 9, 12, 18, 24, 36, 48, 54 Mbps
- 802.11h Dynamic Frequency Selection (DFS)/Transmit Power Control (TPC)
- 802.11j channels (Japan)
- DBPSK, DQPSK, and CCK modulation schemes
- BPSK, QPSK, 16-QAM, and 64-QAM modulation
- Adaptive Receive Filter for DSSS modes
- Adaptive Equalizer for high rate modes
- Exceptional multi-path delay spreads up to 680 ns in 11 Mbps mode and 150 ns in 54 Mbps mode

3.1.2.1 BBU Description

Figure 15 shows the functional blocks of the baseband processor.

Figure 15: BBU Block Diagram



3.1.2.1.1 BBU Transmitter

Figure 16: BBU Transmit Path—802.11b

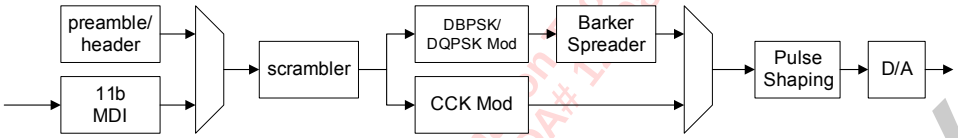


Figure 17: BBU Transmit Path—802.11a/g

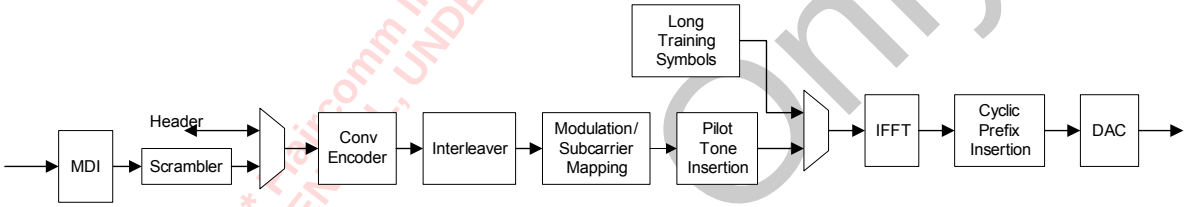
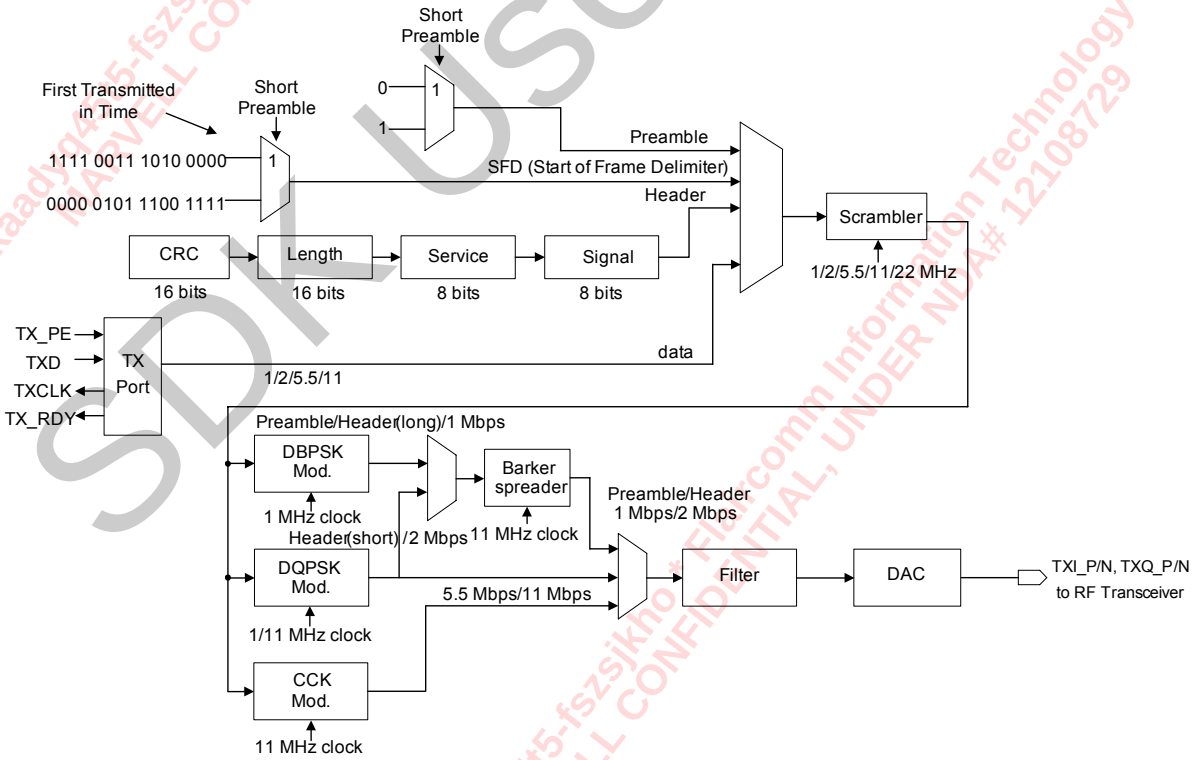


Figure 18: BBU Transmitter—802.11b



3.1.2.1.2 BBU Receiver

Figure 19: BBU Receive Path—802.11b

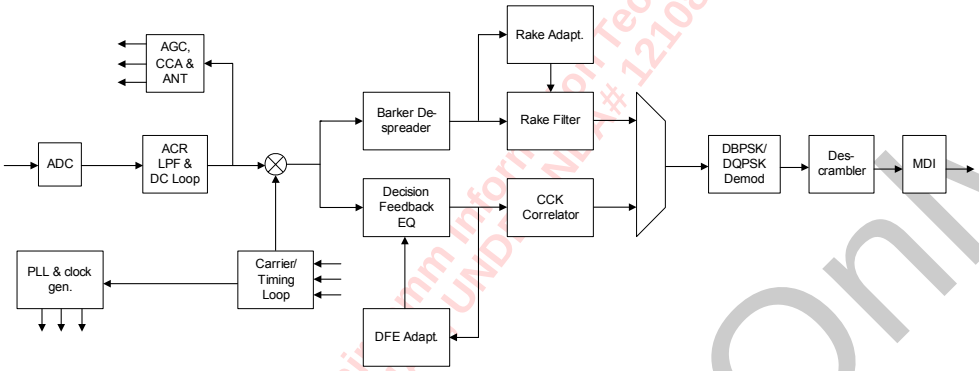
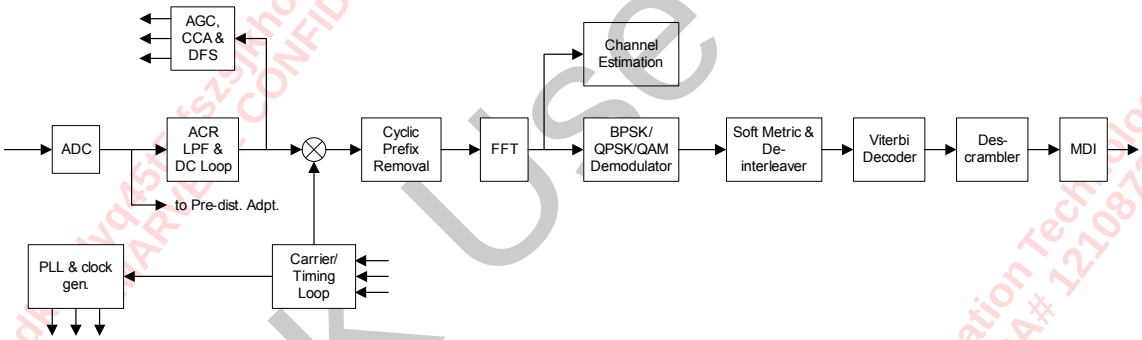


Figure 20: BBU Receive Path—802.11a/g



3.1.2.2 Dynamic Frequency Selection

The 88W8686 BBU supports Dynamic Frequency Selection (DFS) to detect the presence of radar signals. There are two modes of DFS operation: Channel Availability Check and In-Service Monitoring.

3.1.2.2.1 Channel Availability Check

During channel availability check, all stations are disabled and only the master device is monitoring the radar signal. The duration of the monitoring is up to 60 seconds or less if a radar signal is detected.

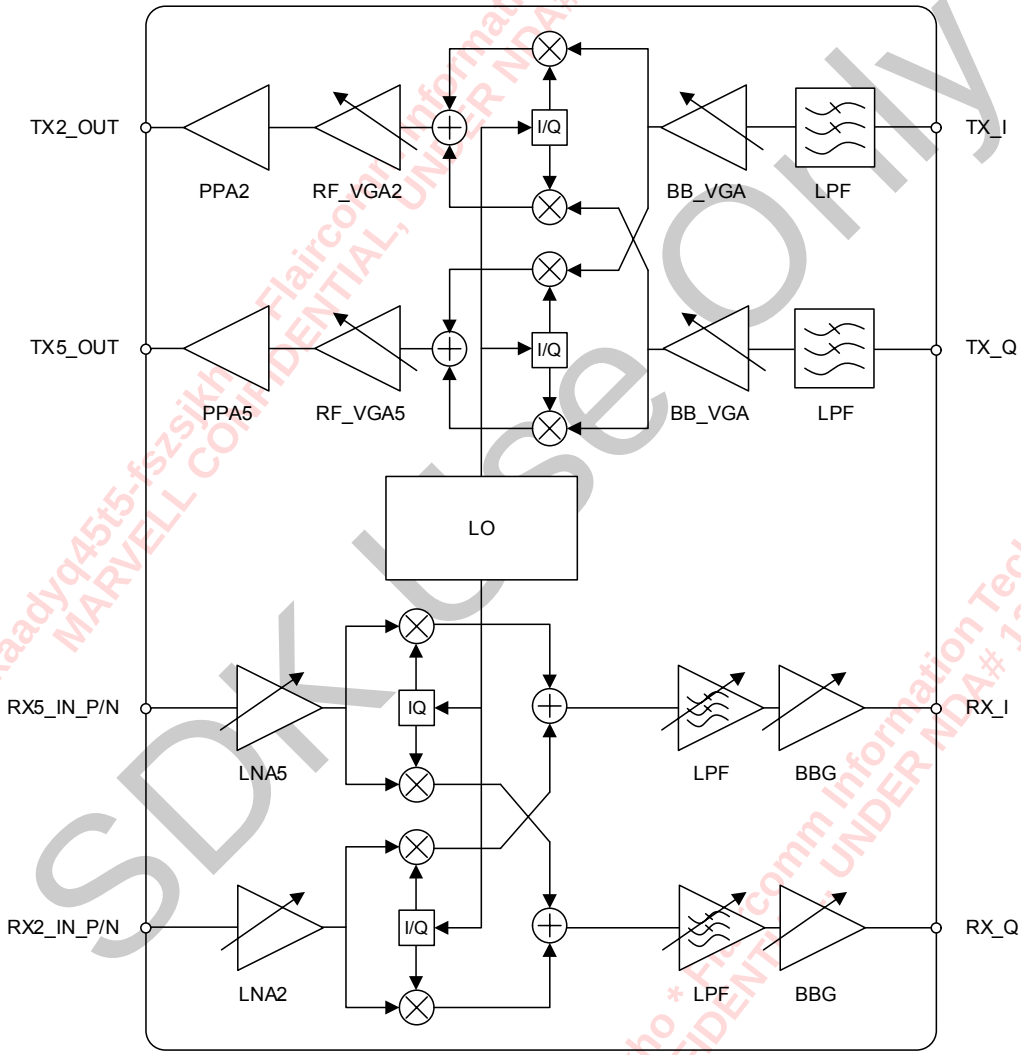
3.1.2.2.2 In-Service Monitoring

During in-service monitoring, all stations are enabled.

3.1.3 WLAN Radio

The 88W8686 direct conversion WLAN RF radio integrates all the necessary functions for receive and transmit, including LNAs, up and down converters, adjustable gain amplifier, filter, and pre-drivers. Figure 21 shows a simplified block diagram of the radio.

Figure 21: WLAN Radio Block Diagram



The LNAs and adjustable gain amplifiers are controlled by the baseband functionality. Channel frequencies are controlled through an internal serial bus, programmed through software.

3.1.3.1 Frequency Channel Support

High rate frequency channels supported for operation in the 2.4 GHz ISM and 5 GHz UNII radio bands are shown in Table 27–Table 30.

Table 27: 802.11g Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
1	2.412	X	X	--	--	X
2	2.417	X	X	--	--	X
3	2.422	X	X	--	--	X
4	2.427	X	X	--	--	X
5	2.432	X	X	--	--	X
6	2.437	X	X	--	--	X
7	2.442	X	X	--	--	X
8	2.447	X	X	--	--	X
9	2.452	X	X	--	--	X
10	2.457	X	X	X	X	X
11	2.462	X	X	X	X	X
12	2.467	--	X	--	X	X
13	2.472	--	X	--	X	X
14	2.484	--	--	--	--	X

Table 28: 802.11a Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
36	5.180	X	X	X	X	--
40	5.200	X	X	X	X	--
44	5.220	X	X	X	X	--
48	5.240	X	X	X	X	--
52	5.260	X	X	X	X	--
56	5.280	X	X	X	X	--
60	5.300	X	X	X	X	--
64	5.320	X	X	X	X	--
149	5.745	X	X	X	X	--
153	5.765	X	X	X	X	--
157	5.785	X	X	X	X	--
161	5.805	X	X	X	X	--
165	5.825	X	X	X	X	--

Table 29: 802.11h Channels Supported

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
100	5.500	X	X	X	X	--
104	5.520	X	X	X	X	--
108	5.540	X	X	X	X	--
112	5.560	X	X	X	X	--
116	5.580	X	X	X	X	--
120	5.600	X	X	X	X	--
124	5.620	X	X	X	X	--
128	5.640	X	X	X	X	--
132	5.660	X	X	X	X	--
136	5.680	X	X	X	X	--
140	5.700	X	X	X	X	--

Table 30: 802.11j Channels Supported (Japan)

Channel	Frequency (GHz)	North America	Europe	Spain	France	Japan MKK
183	4.915	--	--	--	--	X
184	4.920	--	--	--	--	X
185	4.925	--	--	--	--	X
187	4.935	--	--	--	--	X
188	4.940	--	--	--	--	X
189	4.945	--	--	--	--	X
192	4.960	--	--	--	--	X
196	4.980	--	--	--	--	X
7	5.035	--	--	--	--	X
8	5.040	--	--	--	--	X
11	5.055	--	--	--	--	X
12	5.060	--	--	--	--	X
16	5.080	--	--	--	--	X
34	5.170	--	--	--	--	X
38	5.190	--	--	--	--	X
42	5.210	--	--	--	--	X
46	5.230	--	--	--	--	X

3.1.3.2 Operating Modes

The 88W8686 supports dual-band 802.11a and 802.11g/b operation in both the 5 GHz and 2.4 GHz radio bands, respectively. For each device, some of the internal blocks are shared between the two modes of operation. Therefore, the device is designed to operate in only one mode at a time.

3.1.3.2.0.1 Software/Firmware

The MAC follows a programming procedure to switch from 802.11g/b to 802.11a mode, or vice versa, without affecting MAC operation.

3.1.3.2.1 Power Amplifier Control

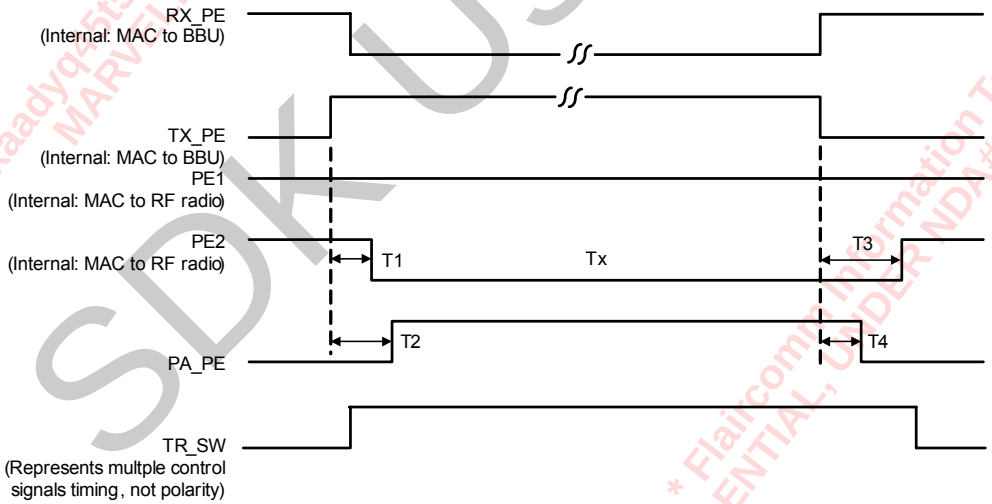
In both 802.11g/b and 802.11a modes, the external PA is controlled by PA_PE_G/A. If the external PA is equipped with an analog signal indicating the transmitted power level, the signal can be fed back to the device for power control purposes. For details of external PA operation, see Section 3.1.3.4.4 "Tx Power Control" on page 73.

- Connect the PA_PE_A pin directly to the 5 GHz external PA.
- Connect the PA_PE_G pin directly to the 2.4 GHz external PA.

3.1.3.2.2 Power Control Sequence (MAC Interface)

Figure 22 shows the power control sequence from the MAC interface to the power amplifier.

Figure 22: Typical Power Control Sequence



Note: The number of signals and polarity are dependant on the TR_SW setting of the application.

The states of the PE1 and PE2 signals determine the operating modes described in Section 3.1.3.2 "Operating Modes" on page 71. TR_SW is not used by the 88W8686. TR_SW is a signal generated by the MAC to control the Tx/Rx switch component located on the board between the antenna and the 88W8686. The switching sequence of PE1, PE2, and PA_PE are internal to the 88W8686 and are controlled by the MAC.

3.1.3.3 Receive Path

The 88W8686 receiver consists of:

- 2.4 GHz LNA/quadrature down conversion mixers
- 5 GHz LNA/quadrature down conversion mixers
- Variable gain amplifiers
- Pair of baseband LPFs
- Programmable gain amplifiers (analog signal processing on the quadrature demodulated signals)

The 88W8686 Rx architecture supports either 2.4 GHz or 5 GHz operation. When selecting 802.11a mode of operation, the 2.4 GHz LNA/mixer combination is in a power-down state. The 5 GHz LNA/mixer combination is active along with the rest of the Rx blocks to down-convert and process the analog signal received. When selecting 802.11g/b mode of operation, the 5 GHz LNA/mixer combination is in a power down state while the 2.4 GHz LNA/mixer combination is active for receive operation.

3.1.3.3.1 Receive Automatic Gain Control

The 88W8686 supports a proprietary AGC interface between the radio and baseband processor. To manage overall gain distribution, the total gain is distributed among the RF and baseband stages. The total gain is realized through variable gain stages within each of the RF, and baseband sections. The gain adjustment of the integrated LNA and AGC is seamlessly controlled by the baseband processor functions integrated into the 88W8686.

3.1.3.3.2 Baseband Circuits

The quadrature demodulator down converts and I/Q splits the signal received to in-phase and quadrature phase. Signals are then passed through a pair of LPFs to reject the adjacent channel energy, and a pair of variable gain stages amplify the signal to the full scale of the analog to digital converters.

Both the corner frequency of the LPF and the offset of the baseband stages are calibrated automatically. These calibrations occur frequently enough to adjust for changes in environmental conditions.

3.1.3.4 Transmit Path

3.1.3.4.1 2.4 GHz Operation

The 2.4 GHz transmit path includes:

- Pair of LPFs
- Pair of baseband variable gain amplifiers
- Quadrature up-converter
- RF variable gain amplifier
- 2.4 GHz preamplifier

3.1.3.4.2 5 GHz Operation

The 5 GHz transmit path includes:

- Pair of LPFs
- Pair of baseband variable gain amplifiers
- Quadrature up-converter
- RF variable gain amplifier
- 5 GHz preamplifier

3.1.3.4.3 Tx Radio Band Operation

The baseband LPF removes aliasing products from the DAC, while the variable gain amplifiers is used for power control. The preamplifier is designed to support a wide range of external power amplifiers. The embedded power control loop is also flexible enough to accept a wide range of power detector characteristics.

3.1.3.4.4 Tx Power Control

The transmitter signal path is affected by changes in environmental conditions and the accuracy of external components. Therefore, proper gain control is required to account for gain variations in the transmit signal path due to temperature and process variations.

Gain control is accomplished with a power control loop circuit. The loop consists of a power detector that monitors the actual PA output during every Tx packet and compares that level with a power detect threshold. The gain is then adjusted on the next Tx packet.

When first powered up, the 88W8686 is set to receive mode (transmit in standby mode). In transmit mode, the device transmits the first packet of data with the predefined gain setting. The output power detection circuit monitors and adjusts the gain setting by either increasing or decreasing the transmit gain, depending on the output of the power detection circuit. The gain adjustment is performed once per packet. Typically, it takes a few packets for the gain to settle to appropriate settings.

The XPWDET2 or XPWDET5 pin must be connected to the output of a power sense signal of an off-chip PA (pseudo DC signal). This signal is then compared against an on-chip programmable thresholds selected by VT_PWDET_HI and VT_PWDET_LO.

The required thresholds for a selected power level is specific to the characteristics of the PA used in the design. Generating the proper control mapping and programming the thresholds accordingly is required.

3.1.3.5 Programmable Frequency Synthesizer

3.1.3.5.1 Clock Input Source

The reference clock for the 88W8686 is derived from one of two types of clock input sources:

- CMOS clock input (>1.0V to 1.8V)
- Low swing clock input (0.4V to 1.0V)

When using a full CMOS clock input swing, the input can be DC or AC coupled. Lower clock input swings require an AC coupling capacitor.

3.1.3.5.2 Channel Frequencies

The RF radio channel frequency is programmed through the RF registers.

3.1.4 WLAN Encryption

3.1.4.1 Wireless Encryption Unit

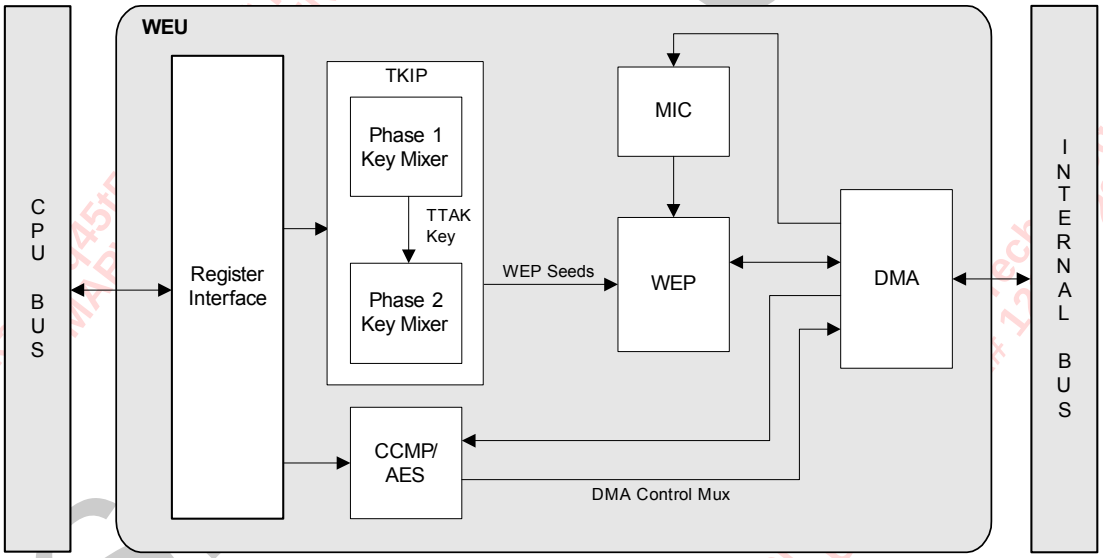
The 88W8686 Advanced Wireless Encryption Unit (WEU) is compliant to 802.11i MAC Security Enhancements. The WEU contains hardware support for encryption and decryption using Counter-Mode/CBC-MAC Protocol (CCMP) and Temporal Key Integrity Protocol (TKIP).

CCMP uses Advanced Encryption Standard (AES) algorithm with 128-bit key for encryption, decryption, and Message Integrity Code (MIC) generation. CCMP protects the integrity of both MPDU data field and selected portion of the IEEE 802.11 MPDU header. Refer to Federal Information Processing Standard (FIPS) PUB 197 for further information on the AES algorithm.

TKIP uses the Wired Equivalent Privacy (WEP) cipher algorithm with 128-bit temporal key for encryption and decryption.

Figure 23 shows a block diagram of the WEU.

Figure 23: WEU Block Diagram



3.1.4.1.1 AES Encryption

When performing AES encryption, the WEU performs encryption or decryption of an entire frame, in 128-bit blocks. The WEU works closely with firmware to complete the full encryption/decryption for each packet.

WEU features include:

- Support for 128-bit key size
- Support for encryption and decryption operations
- Optional Counter Mode with CBC-MAC Protocol (CCMP) processing mode
  - Message Integrity Code (MIC) over packet data and partial MPDU header
  - Counter mode encryption generation and checking
- Interrupt flags for the CPU upon completion

3.1.4.1.2 WEP Processing

Wired equivalent privacy (WEP) relies on an encryption/decryption algorithm used in the IEEE 802.11 standard. The algorithm is a symmetric stream cipher. The same key and algorithm are used for both encryption and decryption. Key management is performed by firmware.

3.1.4.1.2.1 TKIP Processing

When performing WEP processing (64- or 128-bit), TKIP processing is supported (optionally).

3.2 Networking Coexistence

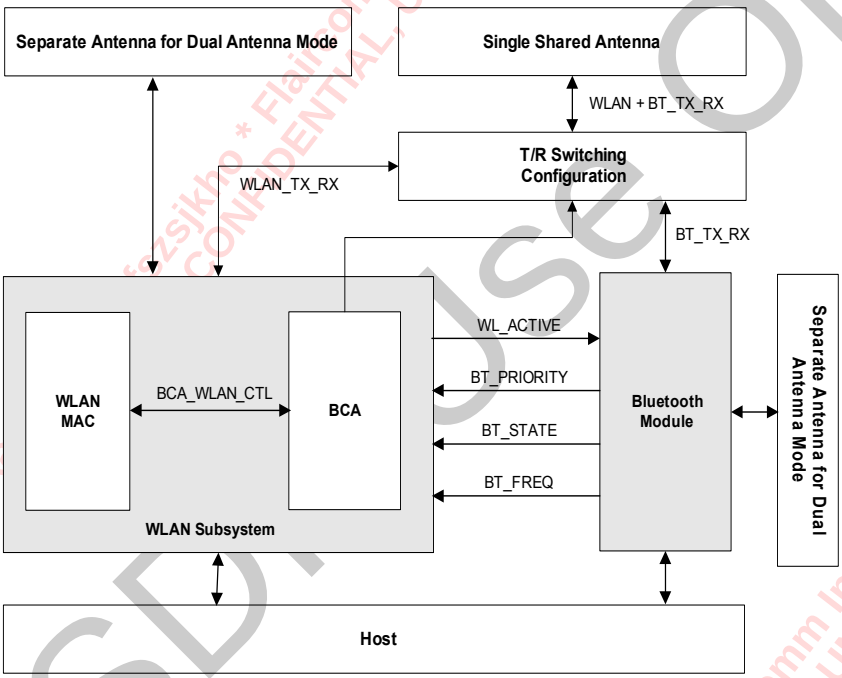
The 88W8686 supports coexistence capability with co-located Bluetooth devices.

There are three Bluetooth Coexistence Arbitration (BCA) schemes in the 88W8686:

- Marvell 2-Wire Bluetooth Coexistence Arbitration (2WBCA) scheme
- Marvell 3-Wire Bluetooth Coexistence Arbitration (3WBCA) scheme
- Marvell 4-Wire Bluetooth Coexistence Arbitration (4WBCA) scheme

Only one of the BCA schemes can be used at a time. In addition, the 88W8686 contains a Switch Module (SM) that controls antenna switching for single antenna applications. For dual antenna applications, the SM is normally bypassed.

Figure 24: Bluetooth Top Block Diagram



3.2.1 System Level Configuration

Hardware configurability enables the following system-level configuration options:

- Bluetooth 1.1 or Bluetooth 1.2 Adaptive Frequency Hopping (AFH)
- Marvell QoS-aware 2-wire coexistence signaling interface or 3/4-wire coexistence signaling interface
- Single shared antenna or dual antenna
  - For single antenna system, single 3-port or dual 2-port T/R switching configuration
  - For single antenna system with 3-port T/R switch, 2-bit encoded or 3-bit once-hot switch control
- Configurable timing on coexistence signaling interface and T/R switch control interface
- Programmable external Bluetooth device signal polarity
- Future-proofed firmware programmable and system-configurable QoS classification and prioritization

3.2.2 BCA Overview

3.2.2.1 1WBCA

The 1WBCA accepts a single input (BT_RF_ACTIVE) from the Bluetooth device. The 1WBCA stops the WLAN device from transmitting when BT_RF_ACTIVE is asserted by de-asserting the PA_EN signal. In addition, the 1WBCA asserts the CCA signal to the WLAN MAC when BT_RF_ACTIVE is asserted.

There is no support for single antenna when using 1WBCA.

3.2.2.2 2WBCA

- BT_PRIORITY—input signal to inform the SoC that high priority Bluetooth traffic is about to be exchanged between the Bluetooth devices. The assertion of this signal should proceed the actual Bluetooth packet slot time. De-assertion of this signal does not necessarily mean that there is no Bluetooth activity.
- WL_ACTIVE—output signal from the SoC to indicate that the WLAN is active (either Tx or Rx packets).

Both signals are active high signals.

The 2WBCA accepts one input (BT_PRIORITY) from the Bluetooth device, requesting access to the medium for a priority Bluetooth event. The BCA unit outputs a control (WL_ACTIVE) signal to the Bluetooth device to signal when the WLAN is active. The Bluetooth device should not attempt to transmit when the WL_ACTIVE signal is high.

By default, the 2WBCA considers the following times to be WLAN high priority Rx requests:

- Following SIFS interval after Tx
- Between TBTT and Beacon received (or TBTT expired)

All other times when the WLAN device is not transmitting are considered to be low priority Rx requests. The 2WBCA determines Tx priority based on the frame type and register settings.

3.2.2.3 3WBCA

The 3WBCA uses these three signals:

- BT_PRIORITY (BT_RF_ACTIVE)—input signal to inform the SoC that Bluetooth traffic is actively in Tx or Rx mode. The assertion of this signal precedes the actual Bluetooth packet slot time.
- WL_ACTIVE (BT_TX_CONFXn) —output signal from the SoC to the Bluetooth device to indicate permission to Tx. If this output is low, then the Bluetooth device can Tx. This signal stays low for the duration of Bluetooth transmission.
- BT_STATE—input to inform the SoC whether Bluetooth is in Tx or Rx mode and the priority level of the traffic. Priority information on the BT_STATE input pin is signaled after the BT_PRIORITY signal is asserted. The Bluetooth Tx/Rx information on the BT_STATE input pin is signaled after priority information.

The 3WBCA accepts two inputs (BT_RF_ACTIVE, BT_STATE) from the Bluetooth device. The BT_PRIORITY input informs the BCA that the Bluetooth device requests access to the medium. The BT_STATE input informs the BCA of the priority of BT_RF_ACTIVE and the direction of the Bluetooth data (Tx or Rx). When 3WBCA is used in a single antenna system, only priority information is used (direction of Bluetooth data is ignored).

The BCA unit outputs a control (BT_TX_CONFXn or WL_ACTIVE) to the Bluetooth device to signal when the BCA has granted medium access to the Bluetooth device. The Bluetooth device should not attempt to transmit when the BT_TX_CONFXn or WL_ACTIVE signal is high. The 3WBCA determines Rx and Tx priority based on the frame type and register settings.

3.2.2.4 4WBCA—Extension of 3WBCA

- BT_PRIORITY (BT_RF_ACTIVE)—input signal to inform the SoC that the Bluetooth device requests access to the medium.
- WL_ACTIVE (BT_TX_CONFXn)—output signal from the SoC to indicate permission to Tx. If low, the Bluetooth device can Tx. This signal stays low for the duration of Bluetooth transmission.
- BT_STATE—input signal to inform the SoC of the BT_REQUEST priority and the direction of the Bluetooth data (Tx or Rx).
- BT_FREQ—input signal to inform the SoC whether Bluetooth traffic will be using a channel that overlaps with the WLAN channel or not.

The 4WBCA is based on the 3WBCA with the addition of an input signal specifying whether the Bluetooth device will be using a channel that overlaps with the WLAN channel (in band) or does not overlap with the WLAN channel (out of band). The same control registers affect the 3WBCA and 4WBCA schemes.

The 4WBCA accepts three inputs (BT_PRIORITY, BT_STATE, BT_FREQ) from the Bluetooth device. The BT_PRIORITY input informs the BCA that the Bluetooth device requests access to the medium. The BT_STATE input informs the BCA of the priority of the BT_RF_ACTIVE and the direction of the Bluetooth data (Tx or Rx). The BT_FREQ input informs the BCA whether Bluetooth traffic will be using a channel that overlaps with the WLAN channel or not. To use the BT_FREQ function, the host system must know what WLAN channel is being used and program the Bluetooth device with a list of Bluetooth channels considered to be overlapping.

See Section 3.2.2.3 "3WBCA" for programming details.

3.2.3 WLAN/Bluetooth Channel Information Exchange

Since Bluetooth and 802.11g/b WLAN use the same 2.4 GHz frequency band, each can cause interference with the other. The level of interference depends on the respective frequency channel used by Bluetooth and WLAN (other factors can impact interference, like Tx power and Rx sensitivity of the device).

In a system with both Bluetooth and WLAN, the common host receives information about WLAN channel usage and passes this information to the Bluetooth device. For Bluetooth 1.2 devices with AFH enabled, the Bluetooth device can block channel usage that overlaps the WLAN channel in use.

When the Bluetooth device avoids all channels used by the WLAN, the impact of interference is greatly reduced, but not completely eliminated. For Bluetooth 1.1 devices, the Bluetooth device cannot block WLAN channel usage and an active BCA scheme at the MAC level is required. The BCA scheme can also be used with Bluetooth 1.2 devices to further reduce the impact of interference to a minimum.

3.2.3.1 Dual/Single Antenna Support

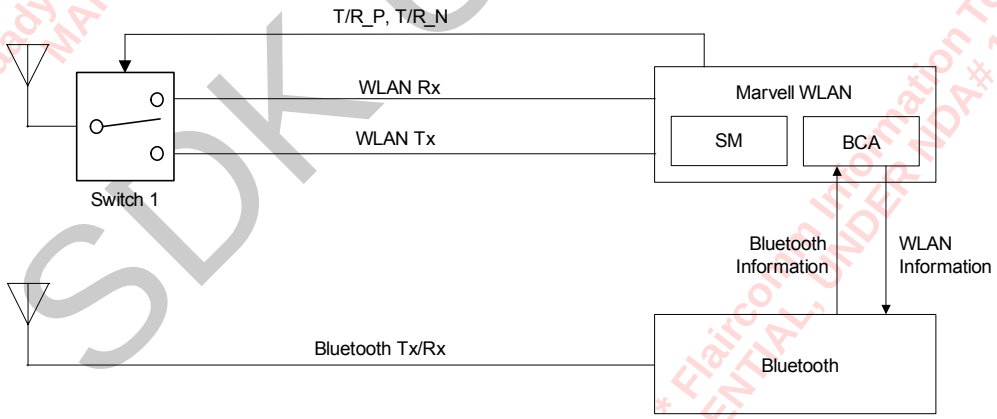
The 2WBCA, 3WBCA, and 4WBCA all support dual and single antenna configurations.

3.2.3.1.1 Generic Dual Antenna Configuration

In most dual antenna configurations, both WLAN and Bluetooth have their own dedicated antennas. In this case, the BCA allows simultaneous WLAN and Bluetooth transactions, resulting in higher WLAN/Bluetooth network performance.

Figure 25 shows the generic dual antenna configuration.

Figure 25: Generic Dual Antenna Configuration



3.2.3.1.2 Generic Single Antenna Configuration

In single antenna configurations, both WLAN and Bluetooth share one antenna. In this case, the BCA must ensure that only one device is allowed to use the antenna. A single antenna configuration has an advantage of lower cost and board space saving, compared to the dual antenna configuration.

The external RF switches for the single antenna need additional control signals for switch control. This is accomplished by Switch Module (SM) logic in the 88W8686. Two possible external RF switch configurations are supported:

- Single Antenna with two 2-way switches, shown in Figure 26
- Single Antenna with one 3-way switch (some 3-way switches which have internal decoders need only 2-bit control (use only T/R_P, T/R_N pins); others need 3-bit one-hot control), shown in Figure 27

Figure 26: Single Antenna—Two, 2-Way Switches

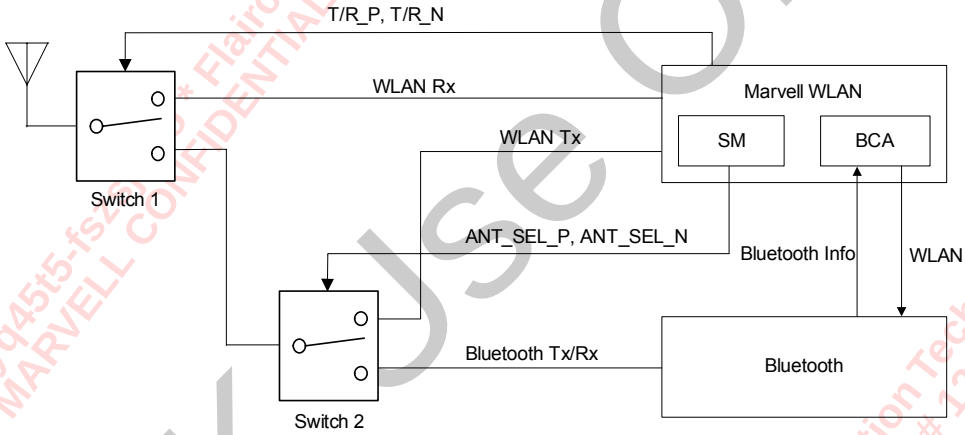
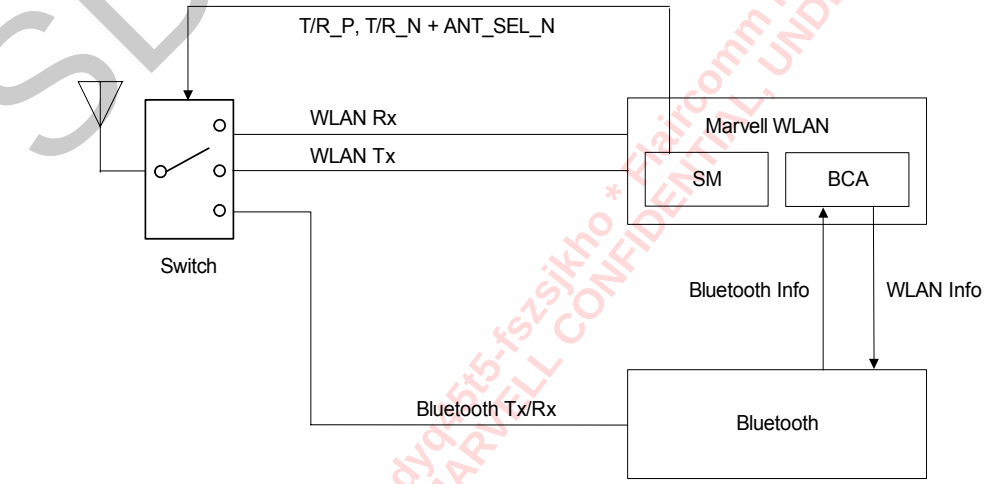


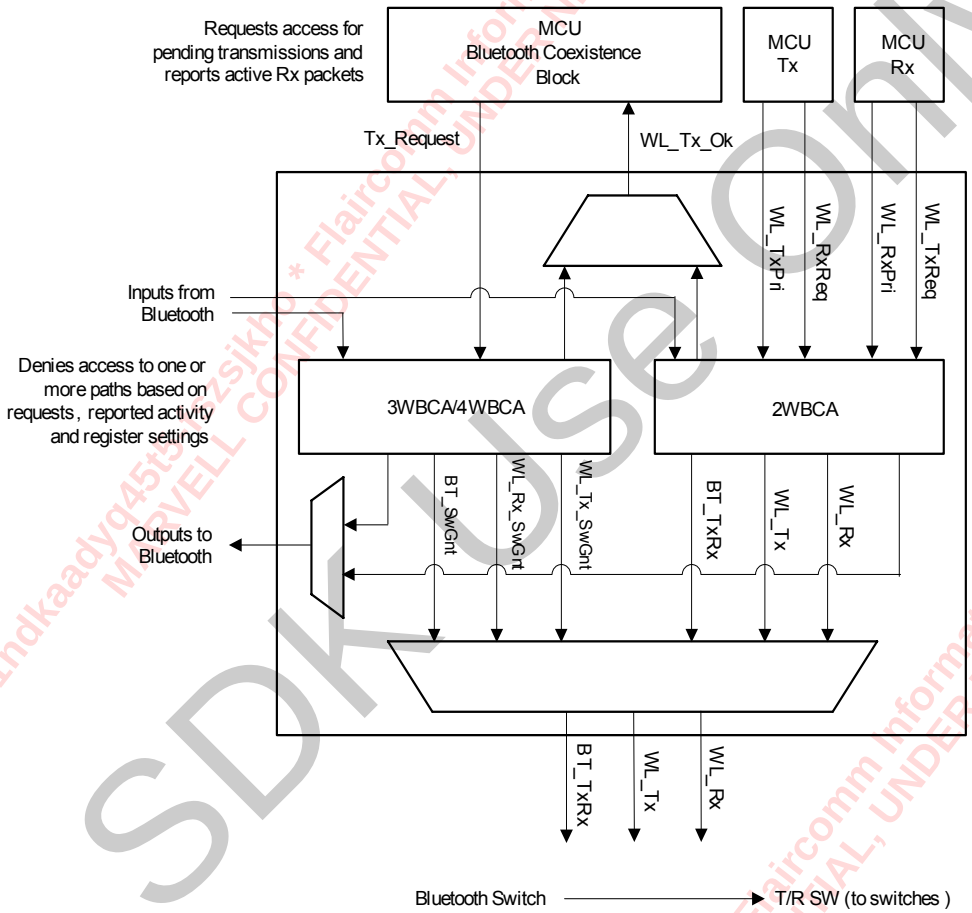
Figure 27: Single Antenna—One, 3-Way Switch



3.2.4 2-Wire BCA

The 2WBCA interface decides which device has primary access to the shared wireless medium according to the 2WBCA (CSR) coexistence scheme. The 2WBCA interface makes its decision based on input signals from the Bluetooth device, input signals from the 802.11 MAC device, and MAC register settings. The inputs signals from the 802.11 and Bluetooth device report activity or priority for their respective devices. The 2WBCA interface module compares any conflicting traffic based on a programmable table in the MAC registers.

Figure 28: 2WBCA Block Diagram



3.2.4.1 2-Wire BCA Arbitration Tables

The arbitration scheme is as follows:

- WLAN high-priority packets have priority over all Bluetooth packets. Bluetooth high-priority packets have priority over WLAN low-priority packets.
- The Bluetooth and WLAN arbitration windows may overlap each other. Regardless of who issued the request first, the grant decision for Bluetooth is based on whether the WLAN request (sampled at the end of the Bluetooth arbitration window) is of a priority such that the arbiter decides not to grant to Bluetooth. If Bluetooth does not receive a grant after the Bluetooth arbitration window and the WLAN arbitration window expires, then WLAN is given the grant. If the WLAN arbitration window expires BEFORE the Bluetooth arbitration window expires, WLAN is automatically given grant. The arbitration logic is not symmetric between WLAN and Bluetooth. As long as WLAN arbitration window expires while Bluetooth is not granted, WLAN is granted. This is true for both single and dual-antenna configurations.
- During WLAN grant state, if it decides that the latest Bluetooth request is of high importance, the arbiter may stop the WLAN while it is in the middle of packet transfer. With the exception for high-priority WLAN packets, there is no guarantee that WLAN can transmit or receive the entire packet. This approach optimizes the performance of Bluetooth voice applications at the expense of WLAN performance.

Table 31: Single Antenna Default Arbitration Table

WLAN Tx Request	WLAN Tx Priority	WLAN Rx Request	WLAN Rx Priority	Bluetooth Priority	Result
0	0	1	0	1	Stop Low Priority WLAN Rx High Priority Bluetooth OK
0	0	1	1	1	High Priority WLAN Rx OK Stop High Priority Bluetooth
1	0	0	0	1	Stop Low Priority WLAN Tx High Priority Bluetooth OK
1	1	0	0	1	High Priority WLAN Tx OK Stop High Priority Bluetooth

Table 32: Dual Antenna Default Arbitration Table

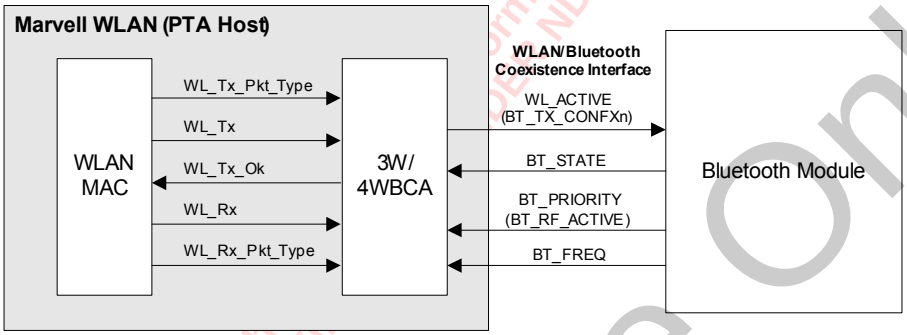
WLAN Tx Request	WLAN Tx Priority	WLAN Rx Request	WLAN Rx Priority	Bluetooth Priority	Result
0	0	1	0	1	Low Priority WLAN Rx OK High Priority Bluetooth OK
0	0	1	1	1	High Priority WLAN Rx OK High Priority Bluetooth OK
1	0	0	0	1	Stop Low Priority WLAN Tx High Priority Bluetooth OK
1	1	0	0	1	High Priority WLAN Tx OK Stop High Priority Bluetooth

3.2.5 3-Wire BCA and 4-Wire BCA

The 3WBCA and 4WBCA units operate the same, except that the 4WBCA includes an additional input signal to specify to the SoC whether the Bluetooth device is using a channel that overlaps with the WLAN channel.

The 4WBCA coexistence framework is based on the IEEE 802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme. This scheme is recommended for next generation mobile phones.

Figure 29: 3W/4WBCA High-Level Block Diagram



3.2.5.1 WLAN Packet Classification

WLAN packet information includes the 6-bit Pkt_Type (apply to either WLAN Tx or Rx packets). The arbitration unit has two 64-bit programmable masks (WL_Tx_Pri_Mask and WL_Rx_Pri_Mask) to mask off all the low-priority packet types. The remaining unmasked packet types are considered high-priority packet types (firmware puts 0 on the WL_Pri_Mask corresponding to the packet type that has low-priority). By default, only WLAN ACK packet types have a 1 in the mask.

{WL_Tx_Pkt_Type, WL_Tx_Pri_Mask} -> WL_Tx_Pri

{WL_Rx_Pkt_Type, WL_Rx_Pri_Mask} -> WL_Rx_Pri

3.2.5.2 Arbitration

The WLAN MAC includes a flexible packet level arbitration scheme between the WLAN and Bluetooth. An arbiter inside the arbitration block decides whether WLAN or Bluetooth can transmit.

{WL_Pri, WL_Tx_Rx, BT_Pri, BT_Tx_Rx} -> Arb_Decision

Table 33 shows the default Arb_Decision, which is geared towards performance optimization for both WLAN and Bluetooth, based on coexistence test results. Arb_Decision is controlled by two sets of 32-bit firmware-programmable registers for flexibility during performance tuning.

Decisions made by the arbitration scheme use the following inputs and register controls:

- Classification of each type of WLAN packet as high priority or low priority
- Recognition of each Bluetooth request as a request to transmit or receive high or low priority
- Selection of which traffic type has higher priority: high priority WLAN or high priority Bluetooth
- Selection of which traffic type has higher priority: low priority WLAN or low priority Bluetooth

3.2.5.2.1 Arbitration Scheme

The arbitration scheme is as follows (default behavior shown):

- WLAN high-priority packets have priority over all Bluetooth packets. Bluetooth high-priority packets have priority over WLAN low-priority packets. WLAN medium-priority packets have priority over Bluetooth medium and low-priority packets.
- If AFH is enabled in the Bluetooth device and sufficient guard-band outside the WLAN operating frequency is preserved, the Bluetooth device uses the OutOfBand (OOB) channel with respect to the WLAN device. Otherwise, the Bluetooth device uses the InBand (IB) and OOB channels with respect to the WLAN device. Firmware controls the arbiter for Bluetooth IB versus OOB by programming the arbitration mode configuration register.
- For the co-located devices running in dual antenna configuration:
  - WLAN Tx and Bluetooth Tx in OOB situation have little interference impact on each other.
  - WLAN Tx and Bluetooth Tx in IB situation have a sizable interference impact on each other. Therefore, the arbiter decision table allows either WLAN or Bluetooth Tx, based on their relative packet priorities.
  - WLAN Tx and Bluetooth Rx (both OOB and IB) have sizable interference impacts on Bluetooth Rx. Therefore, the decision table stops WLAN Tx when Bluetooth Rx is prioritized over WLAN Tx.
  - WLAN Rx and Bluetooth Tx (both OOB and IB) have sizable interference impacts on WLAN Rx. Therefore, the decision table stops Bluetooth Tx when WLAN Rx is prioritized over Bluetooth Tx.
- For Bluetooth requests, the arbiter has a Bluetooth arbitration window of approximately 75 µs (programmable) after assertion of the signal indicating the start of Bluetooth Tx/Rx high-priority packets. During the Bluetooth arbitration window, the arbiter checks if the WLAN has a Tx or Rx request. If the WLAN requests during the arbitration window, the arbiter makes an arbitration decision based on the arbiter decision table. Typically, for the Bluetooth device, once the arbiter allows it to transmit, the Bluetooth does not stop transmitting until the transmiting packet completes. For single antenna mode, if a higher priority WLAN request enters while the Bluetooth transaction is on going, the arbiter requests the T/R SM to stop Bluetooth immediately and allow the WLAN to use the antenna.
- For WLAN requests, the arbiter has a WLAN arbitration window (normally programmed to zero), but the arbiter may stop the WLAN while the WLAN is in the middle of packet transmission. Since WLAN arbitration window is typically zero, the WLAN is granted access immediately if there is no Bluetooth request at that time. Except for WLAN high-priority packets, there is no guarantee that WLAN can transmit or receive the entire packet (for single antenna case). The arbiter can stop the WLAN from transmitting or receiving (for single antenna case) in the middle of the packet if there is a new Bluetooth request, and the new arbiter decision is in favor of the Bluetooth packet. This approach optimizes the performance of Bluetooth voice application, but at the expense of WLAN performance.

3.2.5.2.2 Arbiter Decision Tables

Dual Antenna System Configuration

Table 33: Arbiter Decision Table (BT_FREQ_OOB Bit = 1, Always InBand)

Name	Value									
WLAN Priority 0 = low 1 = high	1	1	1	X	0	0	0	0	0	0
WLAN Tx_Rx 0 = Rx 1 = Tx	1	1	0	0	1	1	0	0	1	1
Bluetooth Priority[1] 0 = low 1 = high	X	X	X	X	0	1	0	1	0	1
Bluetooth Tx_Rx 0 = Rx 1 = Tx	0	1	1	0	0	0	1	1	1	1
BT_FREQ	1	1	1	1	1	1	1	1	1	1
Arbiter Decision (WL_Arb_TxOk_Cfg; BT_Arb_TxOk_Cfg registers)	WLAN Tx OK	WLAN Tx OK	WLAN Rx OK	WLAN Rx OK	WLAN Tx OK	WLAN Tx stop	WLAN Rx OK	WLAN Rx OK	WLAN Tx OK	WLAN Tx stop
	BT Rx OK	BT Tx stop	BT Tx stop	BT Rx OK	BT Rx OK	BT Rx OK	BT Tx stop	BT Tx OK	BT Tx stop	BT Tx OK

1. Bluetooth priority input will always be either high or low for existing external Bluetooth devices. Internal Bluetooth may be configured to support medium priority. Medium priority decision is not illustrated here for simplicity, but it follows the same pattern.

Table 34: Arbiter Decision Table, Bluetooth 1.2 Device (BT_FREQ_OOB Bit = 0, Always OutofBand)

Name	Value									
WLAN Priority 0 = low 1 = high	1	1	1	X	0	0	0	0	0	0
WLAN Tx_Rx 0 = Rx 1 = Tx	1	1	0	0	1	1	0	0	1	1
Bluetooth Priority[1] 0 = low 1 = high	X	X	X	X	0	1	0	1	0	1
Bluetooth Tx_Rx 0 = Rx 1 = Tx	0	1	1	0	0	0	1	1	1	1
BT_FREQ	0	0	0	0	0	0	0	0	0	0
Arbiter Decision (WL_Arb_TxOk_Cfg; BT_Arb_TxOk_Cfg registers)	WLAN Tx OK	WLAN Tx OK	WLAN Rx OK	WLAN Rx OK	WLAN Tx OK	WLAN Tx stop	WLAN Rx OK	WLAN Rx OK	WLAN Tx OK	WLAN Tx stop
	BT Rx OK	BT Tx stop	BT Tx stop	BT Rx OK	BT Rx OK	BT Rx OK	BT Tx stop	BT Tx OK	BT Tx stop	BT Tx OK

1. Bluetooth priority input will always be either high or low for existing external Bluetooth devices. Internal Bluetooth may be configured to support medium priority. Medium priority decision is not illustrated here for simplicity, but it follows the same pattern.

3.2.5.2.2.1 Single Antenna System Configuration

For a single antenna system, WLAN and Bluetooth priority solely determines the arbiter decision. The result of this is that the direction of data flow (Rx versus Tx) is ignored by the arbiter.

WL_Tx_Rx, BT_Tx_Rx, and BT_FREQ are ignored by the arbiter.

For this scheme, WLAN high-priority packets have priority over all Bluetooth packets by default. Bluetooth high-priority packets have priority over WLAN low-priority packets. WLAN medium-priority packets have priority over Bluetooth medium and low-priority packets.

In this mode, the arbiter must generate three output signals (WL_Tx_SwGnt, WL_Rx_SwGnt, BT_SwGnt) to the SM. The SM controls the select signals to the external switch(es). The outputs to the SM follow the timing of the original request signals. The arbiter does not insert additional delay to compensate for any latency requirement required by the BBU/RF/external switch.

Table 35: Arbiter Decision Table, Bluetooth 1.2/1.1 Device

Name	Value			
WLAN Priority 0 = low 1 = high	0	0	1	1
Bluetooth Priority 0 = low 1 = high	0	1	0	1
Arbiter Decision (SWL_Arb_TxOk_Cfg)	WLAN Tx/Rx OK	WLAN Tx/Rx stop	WLAN Tx/Rx OK	WLAN Tx/Rx OK
	Bluetooth Tx/Rx stop	Bluetooth Tx/Rx OK	Bluetooth Tx/Rx stop	Bluetooth Tx/Rx stop

3.2.5.2.2.2 Arbitration Table Variables

Table 36: Arbitration Table Variables

Variable	Description
WLAN_TX_RX	WLAN Tx/Rx Timeslot 0 = WLAN requests to receive, or the WLAN is in the middle of receiving a packet 1 = WLAN requests to transmit, or the WLAN is in the middle of transmitting a packet
BT_TX_RX	Bluetooth Tx/Rx Timeslot 0 = next Bluetooth timeslot is receive timeslot, or Bluetooth in middle of receiving a packet 1 = next Bluetooth timeslot is transmit timeslot, or Bluetooth in middle of transmitting a packet
Sleep Mode	Arbiter asserts WL_ACTIVE and Bluetooth device is always allowed to transmit when the WLAN module is in sleep mode.
Custom Coexistence Behavior	WLAN transaction decision and Bluetooth transaction decision outputs of the arbiter shown in Table 35 are generated from user-configurable vectors. The system designer can then overwrite the default values in the vectors and implement custom coexistence behavior. (see WL_Arb_TxOk_Cfg, BT_Arb_TxOk_Cfg registers for Dual Antenna mode, SWL_Arb_TxOk_Cfg [in Arb_Mode_Cfg reg] register bits for Single Antenna mode). The system designer can then overwrite the default values in the vectors and implement custom coexistence behavior.

3.2.6 Switch Module

The switch module (SM) generates the switch control signals to the RF switch(es). The outputs are set by three input signals from the arbitration module and registers settings. The switch module is not responsible for requesting access to the medium, reporting WLAN or Bluetooth activity, nor for deciding who has access to the medium. The SM should be used primarily in single antenna mode. In two antenna mode, the arbitration logic will stop WLAN transmissions that could collide. In both antenna configurations, if none of the three transceiver paths is selected then the SM can give the antenna to Bluetooth, WL_Rx, or alternate between the two using a configurable timer. The SM has no other programmable timing. The level of the four antenna control signals (T/R_P, T/R_N, ANT_SEL_P, and ANT_SEL_N) are independently set for each possible access condition (Bluetooth has access, WLAN Tx has access, WLAN Rx has access).

3.2.6.1 Switch Module Input Ports and States

Table 37: SM Input Ports and States

WL_Tx	WL_Rx	BT_TxRx	Result
0	0	0	Bluetooth has antenna (may be set to WL_Rx or alternate)
0	0	1	Bluetooth has antenna
0	1	0	WL_Rx has antenna
0	1	1	Bluetooth has antenna (programmable)[1]
1	0	0	WL_Tx has antenna
1	0	1	WL_Tx has antenna (programmable)[1]
1	1	0	WL_Tx has antenna (programmable)[1]
1	1	1	WL_Tx has antenna (programmable)[1]

1. More than one device is selected. The BCA unit will not generate this condition when Ant_Mode is set to singe-antenna mode. When Ant_Mode is set to dual-antenna mode, more than one device can be selected. Normally, the SM should not be used for dual-antenna configurations.

3.2.6.2 Switch Module Port List

Table 38: SM Port List

Module Port Name	I/O	Description
WLAN Tx	Input	Input signal to the switch module indicating the 802.11 transmit path should have access to the RF components. If WLAN Tx is asserted, neither WLAN Rx nor Bluetooth Tx/Rx should be asserted in single antenna mode. This signal comes from the arbitration engine.
WLAN Rx	Input	Input signal to the switch module indicating the 802.11 receive path should have access to the RF components. If WLAN Rx is asserted, neither WLAN Tx nor Bluetooth Tx/Rx should be asserted in single antenna mode. This signal comes from the arbitration engine.
Bluetooth Tx/Rx	Input	Input signal to the switch module indicating the Bluetooth device should have access to the RF components. If Bluetooth Tx/Rx is asserted, neither WLAN Tx nor WLAN Rx should be asserted in single antenna mode. This signal comes from the arbitration engine.
TR Switch P	Output	Output signal to one of the switch controllers. Value depends on who has access to the RF components and programmable registers. If BP_TR_SW is asserted, MAC Tx core drives the T/R_P pin instead.
TR Switch N	Output	Output signal to one of the switch controllers. Value depends on who has access to the RF components and programmable registers. If BP_TR_SW is asserted, MAC Tx core drives the T/R_N pin instead.
TR Switch 2P	Output	Output signal to the baseband. If BBU ANT_SEL is asserted, BBU drives the ANT_SEL_P pin instead.
TR Switch 2N	Output	Output signal to the baseband. If BBU ANT_SEL is asserted, BBU drives the ANT_SEL_N pin instead.
T/R Switch 3N	Output	Output to antenna switches for 802.11a/g/b support.

Section 4. Host Interfaces

The 88W8686 Host Interface Unit (HIU) connects several host interface bus units to the internal bus of the device. The connection of each host interface bus unit to the internal bus is multiplexed with the other host interface bus units. The HIU allows only one host interface unit to be active at a time.

The 88W8686 HIU supports the following host interfaces:

- G-SPI Interface
- SDIO Interface

4.1 G-SPI Interface

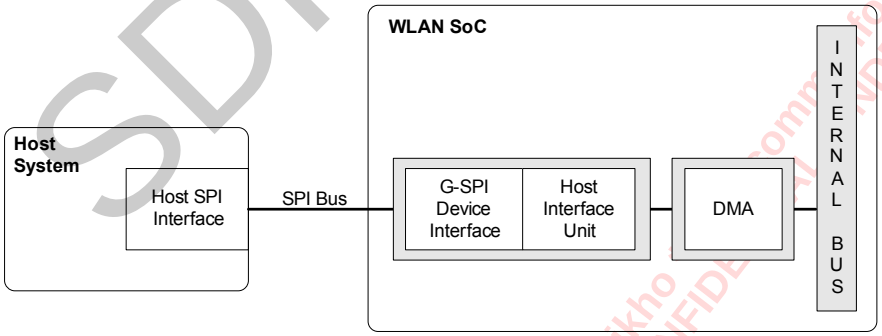
The 88W8686 supports a generic, half-duplex, DMA-assisted SPI host interface (G-SPI) that allows a host controller using a generic SPI bus protocol to access the WLAN device. The G-SPI interface contains interface circuitry between an external SPI bus and the internal shared bus, as shown in Figure 30.

The 88W8686 acts as the device on the SPI bus. The host unit can access the G-SPI registers directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SPI unit supports generic SPI Interface protocols as detailed in the following sections. The design is capable of 50 MHz operation. The interface supports the following functionality.

- SPI unit bus device operation
- SPI unit register read / write
- Interrupt generation to internal CPU
- Interrupt generation to the SPI unit host
- DMA to internal memories
- Wake interrupt to the Power Management Unit

Figure 30: G-SPI Interface Block Diagram



4.1.1 G-SPI Interface Signal Description

See Table 24, "Configuration Pins," on page 52 for host interface configuration settings.

Table 39 shows the signal mapping.

Table 39: G-SPI Interface Description

88W8686 Pin Name	Generic SPI Bus Protocol Name	Description
SPI_CLK	CLK	SPI Unit Clock Input
SPI_SCSn	SCSn	SPI Unit Active Low Chip Select Input
SPI_SDI	SDI	SPI Unit Data Input
SPI_SDO	SDO	SPI Unit Data Output
SPI_SINTn	INTn	SPI Unit Active Low Interrupt Output
RESETn	RSTn	Reset Input

4.1.2 G-SPI Interface Functional Description

The G-SPI supports a variety of simple address/data protocols over a standard G-SPI physical bus. The protocols supported are differentiated by the number of address bits and data ordering.

Each transaction is initiated by assertion of the active low signal SCSn. Following the assertion of SCSn, the SDI input is latched with every positive edge of SCLK. When data is output, it is clocked out with the negative edge of SCLK. The clock input SCLK is low at the start and completion of a transaction. The interrupt output signal (SINTn) is asserted by the card to interrupt the host.

4.1.2.1 Transaction Delays

The first block of data to be transferred is from the host to the device. This block of data contains an address and read/write control. The MSB of the address is low for read operations and high for write operations.

4.1.2.1.1 Write Transaction Delay

For write transactions, the data phase of a transaction immediately follows the address phase of the transaction. There is no need to extend the low time of the clock between address and data or for the host to clock any dummy cycles.

4.1.2.1.2 Read Transaction Delay

There is a delay required between the end of the address phase on the bus and the start of the data phase of the transaction. This delay is shown as TDRR (time delay read register) and TDRP (time delay read port). This delay represents the time delay required for the device to prepare valid data to return to the host.

This delay can be created in two different ways.

First, the read transaction delay is created by the host clocking a known number of dummy clock cycles to the device. The number of dummy clock cycles is specified in the Delay Read Register. There are two parameters in this register:

- Register read access
- Port read access

During the data phase of a transaction, the host continues to provide clock pulses and either drives data on the SDI input or read data from the SDO output.

4.1.2.2 Data Transfers

The host always accesses configuration registers in the G-SPI unit. To access internal memory space, some registers are defined as Port registers. When Port registers are accessed, the device reads or writes from internal memory space using the corresponding Base Address Register (BAR) and DMA engine.

Every transfer between host and device is a burst transfer (single address followed by multiple data). A transfer is terminated by the host after reading or writing the desired amount of data by de-asserting the SCSn input.

4.1.2.2.1 Port Register Access

When the host system reads Port Registers, there is no limit to the burst length (other than the limit imposed by the valid address range of the internal bus). When the host system writes to Port Registers, the only condition on burst length is that the length be a multiple number of DWORDS.

Port Registers (I/O Port, Command Port, Data Port) are used to access internal 32-bit memory space and are always accessed on 32-bit boundaries. Each of these port registers has a corresponding BAR for reads and writes (acting as a pointer to the starting physical address location). Internal memory is also accessed only on 32-bit boundaries. This is accomplished by programming the corresponding BAR with 32-bit aligned values. During these accesses, the lower 16 bits are always presented on the bus first.

4.1.2.2.1.1 Port Register Write Data

Write data to a Port Register is packed into sequential 32-bit memory locations starting at the location of the corresponding BAR. When reading from the Data and Command Ports of the device, the DMA engine continues to fill the FIFO whenever there is room for eight DWORDs (32-bits) of data. When writing data to the device, the de-assertion of the SCSn input causes a flush to the write FIFO.

4.1.2.2.1.2 Port Register Read Data

When reading data from the I/O Port of the device, it is selectable whether the DMA engine performs a single read or burst reads. Burst reads are treated like Data and Command Port reads. Single reads cause the DMA engine to perform a single DWORD access on the internal bus. A single read transaction must be terminated following the first or second 16-bit block of returned data.

4.1.2.2.2 Configuration Register Access

When the host system accesses registers other than the Port Registers, the burst length must be limited to one 16-bit data transfer, or two 16-bit data transfers if the address is on a DWORD boundary. When a unit on the internal bus accesses G-SPI Interface registers, the accesses must be a single DWORD access or smaller.

G-SPI Interface registers, with the exception of Port Registers, can be read from or written to on 16-bit boundaries. Transactions can be terminated after a single 16-bit word is read or written.

4.1.2.3 G-SPI Clock Frequency

The G-SPI clock frequency must not be greater than 2.5 times the internal bus clock frequency.

4.2 SDIO Interface

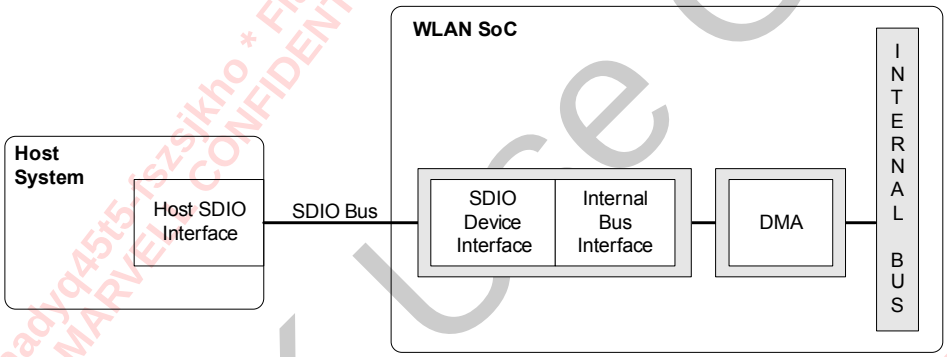
The 88W8686 supports a SDIO device interface that conforms to the industry standard SDIO Full-Speed card specification and allows a host controller using the SDIO bus protocol to access the WLAN device. The SDIO interface contains interface circuitry between an external SDIO bus and the internal shared bus, as shown in Figure 31.

The 88W8686 acts as the device on the SDIO bus. The host unit can access registers of the SDIO interface directly and can access shared memory in the device through the use of BARs and a DMA engine.

The SDIO device interface main features include:

- On-chip memory used for CIS
- Supports SPI, 1-bit SDIO, and 4-bit SDIO transfer modes at the full clock range of 0 to 50 MHz
- Special interrupt register for information exchange
- Allows card to interrupt host

Figure 31: SDIO Interface Block Diagram



4.2.1 SDIO Interface Signal Description

See Table 24, “Configuration Pins,” on page 52 for host interface configuration settings.

Table 40 shows the signal mapping between the 88W8686 device and the SDIO specification.

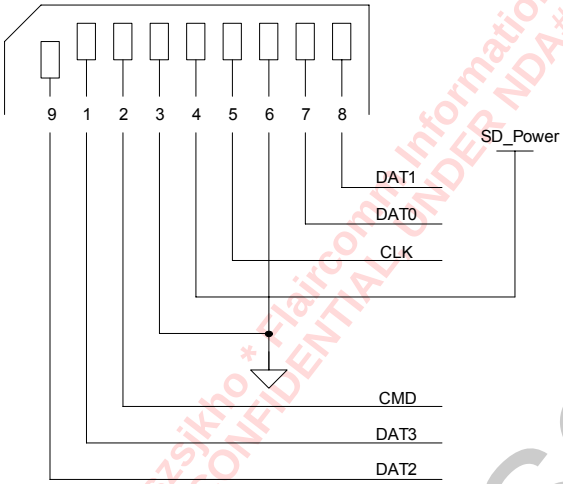
Table 40: SDIO Interface Signal Description

88W8686 Pin Name	Signal Name	Type	Description
SD_DAT[3]	DAT3	I/O	SDIO 4-bit mode: Data line bit [3] SDIO 1-bit mode: Not used SDIO SPI mode: Chip select (neg true)
SD_DAT[2]	DAT2	I/O	SDIO 4-bit mode: Data line bit [2] or Read Wait (optional) SDIO 1-bit mode: Read Wait (optional) SDIO SPII mode: Reserved
SD_DAT[1]	DAT1	I/O	SDIO 4-bit mode: Data line bit [1] SDIO 1-bit mode: Interrupt SDIO SPI mode: Interrupt
SD_DAT[0]	DAT0	I/O	SDIO 4-bit mode: Data line bit [0] SDIO 1-bit mode: Data line SDIO SPI mode: Data out
SD_CMD	CMD	I/O	SDIO 4-bit mode: Command/Response SDIO 1-bit mode: Command line SDIO SPI mode: Data in
SD_CLK	CLK	I/O	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock SDIO SPI mode: Clock

4.2.2 Functional Description

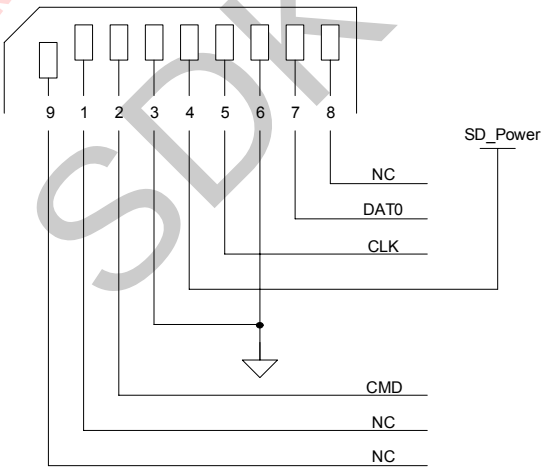
4.2.2.1 SDIO Connection/Function

Figure 32: SDIO Physical Connection—4-Bit Mode



In 4-bit SDIO mode, data is transferred on all 4 data pins (DAT[3:0]), and the interrupt pin is not available for exclusive use as it is utilized as a data transfer line. Thus, if the interrupt function is required, a special timing is required to provide interrupts. The 4-bit SDIO mode provides the highest data transfer possible, up to 100 Mbps.

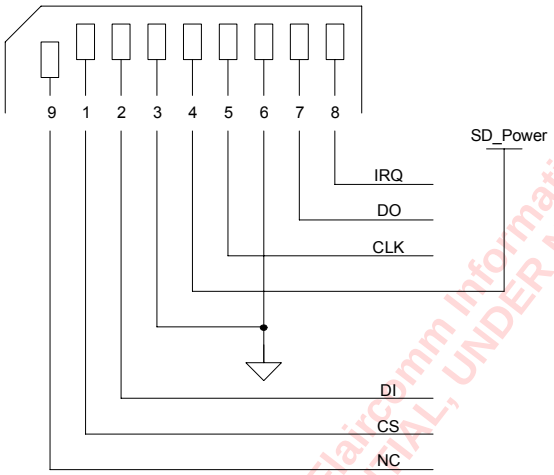
Figure 33: SDIO Physical Connection—1-Bit Mode



Note

In 1-bit SDIO mode, data is transferred on the DAT[0] pin only, and pin 8, which is undefined for memory, is used as the interrupt pin.

Figure 34: SDIO Physical Connection—SPI Mode



Note

In SPI mode pin 8, which is undefined for memory, is used as the interrupt pin.

Table 41: SDIO Electrical Function Definition

Pin	SDIO 4-bit Mode		SDIO 1-bit Mode		SPI Mode	
1	CD/DAT[3]	Data line 3	N/C	Not used	CS	Card Select
2	CMD	Command line	CMD	Command line	DI	Data input
3	VSS1	Ground	VSS1	Ground	VSS1	Ground
4	VDD	Supply voltage	VDD	Supply voltage	VDD	Supply voltage
5	CLK	Clock	CLK	Clock	SCLK	Clock
6	VSS2	Ground	VSS2	Ground	VSS2	Ground
7	DAT[0]	Data line 0	DATA	Data line	DO	Data output
8	DAT[1]	Data line 1 or Interrupt (optional)	IRQ	Interrupt	IRQ	Interrupt
9	DAT[2]	Data line 2 or Read Wait (optional)	RW	Read Wait (optional)	NC	Not used

4.2.2.2 SDIO Command List

All mandatory SDIO commands are supported for both SDIO and SPI modes. SDIO mode commands are shown in Table 42. SPI mode commands are shown in Table 43.

Table 42: SDIO Mode, SDIO Commands

Command	Command Name	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD3	SEND_RELATIVE_ADDR	SDIO Host asks for RCA
CMD5	IO_SEND_OP_COND	SDIO Host asks for and sets operation voltage
CMD7	SELECT/DESELECT_CARD	Sets SDIO target device to command state or back to standby
CMD15	GO_INACTIVE_STATE	Sets SDIO target device to inactive state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory

Table 43: SPI Mode, SDIO Commands

Signal Name	Type	Description
CMD0	GO_IDLE_STATE	Used to change from SDIO to SPI mode
CMD5	IO_SEND_OP_COND	Used in initialization state
CMD52	IO_RW_DIRECT	Used to read/write host register and CIS table
CMD53	IO_RW_EXTENDED	Used to read/write data from/to SQU memory
CMD58	CRC_ON_OFF	SPI only. Enable/disable CRC

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Section 5. Peripheral Bus Interface

The 88W8686 Peripheral Bus Unit (PBU) connects several low speed peripherals to the CPU bus of the device. The PBU buffers up to eight data units per bus transaction and supports both single and burst transfer modes.

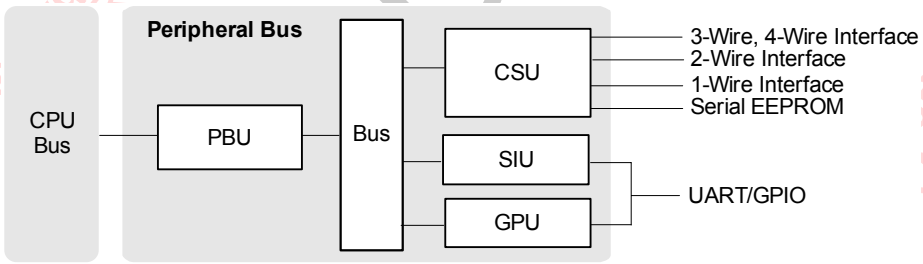
Features supported include:

- Clocked Serial Unit (CSU) for reading and writing the serial EEPROM
  - 3-Wire, 4-Wire (3W4W) Interface (internal interface to RF radio and wireless baseband)
  - 2-Wire Serial Interface (TWSI)
  - 1-Wire Serial Interface
  - SPI Serial (EEPROM) Interface
- 16550 UART controller (SIU)
- GPIO / External Interrupt / LED Interface unit (GPU)

5.1 Data Flow

Figure 35 shows the connection of low speed peripherals to the CPU bus. Data flow through the PBU is from the 88W8686 CPU bus interface through a FIFO to one of the peripheral devices. The peripheral device handles input and output operations to and from the external destination. Access to peripheral host devices occurs through CPU writes to the PBU address space.

Figure 35: PBU Block Diagram



5.2 Operation

Two asynchronous FIFOs are designed inside the PBU, one for transmit data and the other for receive data.

The FIFOs cross clock domains between the internal bus clock and the peripheral bus clock domain.

When the PBU intends to receive any cycles on the internal PBU, it must first wait until any current transactions are complete. Both sides of the PBU are synchronized by internal transmit and receive start and done signals.

5.3 Control

- Generate a peripheral soft reset
- Configure peripheral clock speeds

5.3.1 Soft Reset

Soft reset generates a 4-cycle length active low pulse after the rising edge of PCLK to initialize peripheral devices to their default states.

5.3.2 Peripheral Clock Speeds

Peripheral clock speeds are computed by the equation: PCLK = UART

5.4 Clocked Serial Unit

The CSU is used to exchange data with the RF radio, BBU, and external serial EEPROM. The CSU provides a read-only status to monitor the activity of low speed peripherals.The CSU includes the following features:

- Single host operation
- Programmable serial clock frequency

The CSU supports the following serial synchronous bus protocols for serial interface operation:

- 3-Wire, 4-Wire Serial Interface
- 2-Wire Serial Interface
- 1-Wire Serial Interface
- SPI Serial Interface

5.4.1 Serial Clock Frequency

The CSU uses the internal PCLK signal in the PBU to generate the correct serial clock frequency. In addition, it applies a clock prescaler to clock the input and output data to external devices.

5.4.2 3-Wire, 4-Wire Interface

For the RF radio, BBU, or EEPROM, the clock prescaler is based on the following equation, where SCLK is the serial clock, PCLK is the PBU internal clock, and PRER is the clock prescaler:

$$SCLK = \frac{PCLK}{2 \cdot (PRER)}$$

5.4.3 2-Wire Serial Interface

The 88W8686 2-Wire Serial Interface (TWSI) unit is an interface bridge between a 2-wire serial bus and the CPU. The main features of TWSI include:

- Programmable serial clock frequency
- Single master operation
- Single and multi-byte data transfer with minimum CPU interrupts
- MAC parallel interface for back-door access to external RF device
- Internal clock gating based on mode select
- Double read buffer

5.4.3.1 Serial Clock Frequency

For TWSI mode, the clock prescaler is based on the following equation, where SCLK is the serial clock, PCLK is the PBU internal clock, and PRER is the clock prescaler:

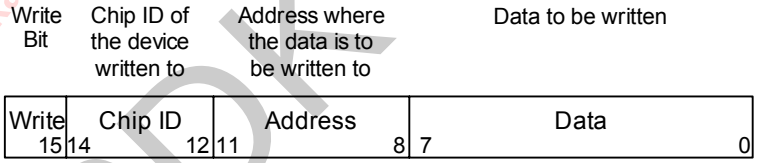
$$SCLK = \frac{PCLK}{5 \cdot (PRER)}$$

5.4.4 1-Wire Interface

The 88W8686 can be combined with the Marvell 88PW886 power management device to achieve ultra low power consumption. Each LDO in the 88PW886 can be individually programmed to power up, power down, or sleep.

A 1-wire serial interface is used between the 88W8686 and 88PW886 devices and is clocked by the internal sleep clock on the 88W8686. The 88PW886 has eight 8-bit registers that are programmed, as write only, by the 88W8686. The 88PW886 has a chip ID (101 or 010) on the interface for identification, as shown in Figure 36.

Figure 36: 1-Wire Data Format



5.4.5 SPI EEPROM

The 88W8686 supports a SPI EEPROM device to hold constants such as MAC address, CIS tables, or code for the internal processor. The 88W8686 supports 1-, 2-, and 3-byte address modes, which allows for EEPROM sizes from 4 KB to 1 MB. The SPI interface can run up to 5 MHz.

Note

Internal Boot ROM can access 2- and 3-byte addresses only.

5.4.5.1 Interface Description

The 88W8686 connects to the SPI EEPROM through the pins shown in Table 44.

Table 44: SPI EEPROM Interface Description

88W8686 Pin Name	EEPROM Pin Name	Description
ECSn	CS	EEPROM Chip Select Out
SDA	SI	Serial Output Pin of the 88W8686 Connected to the serial input pin of the SPI EEPROM.
SCLK	SCK	Serial Clock Signal Refer to the CSU section for more information.
SRWB	SO	Serial Read/Write Control Signal Connected to the serial out pin of the SPI EEPROM. The serial read/write control pin acts as an input in this mode.

5.4.5.2 Boot from SPI EEPROM

When CON[6:5] are programmed to 10, firmware reads and executes boot information from the SPI EEPROM See Table 24: "Configuration Pins" on page 52.

Notes

- EEPROM size must be sufficiently large to hold the firmware code when booting from EEPROM.
- Marvell supports a 2-byte or 3-byte address for SPI EEPROM.

5.4.5.3 SPI EEPROM External Memory

The SPI EEPROM can be used to store MAC addresses or other data. To access the EEPROM, the CPU executes read and write operations through the PBU unit ID into the CSU address space.

5.4.5.4 Write and Read Sequence

5.4.5.4.1 Byte Write

The 88W8686 supports the following Write instructions.

- WRITE—Simple Write instruction
- WRSR—Write to the EEPROM Status Register
- WREN—Write Enable command to the EEPROM
- WRDI—Write Disable command to the EEPROM

Figure 37: Byte Write Signal Diagram

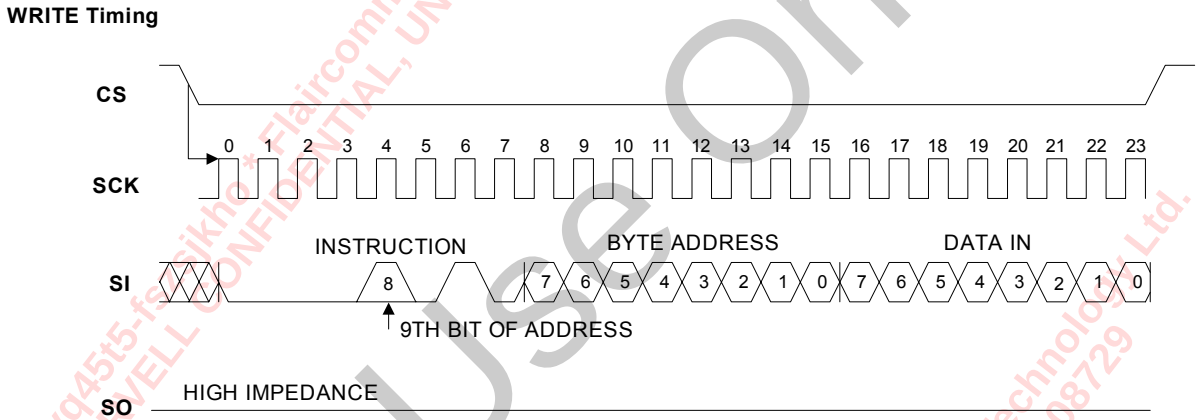
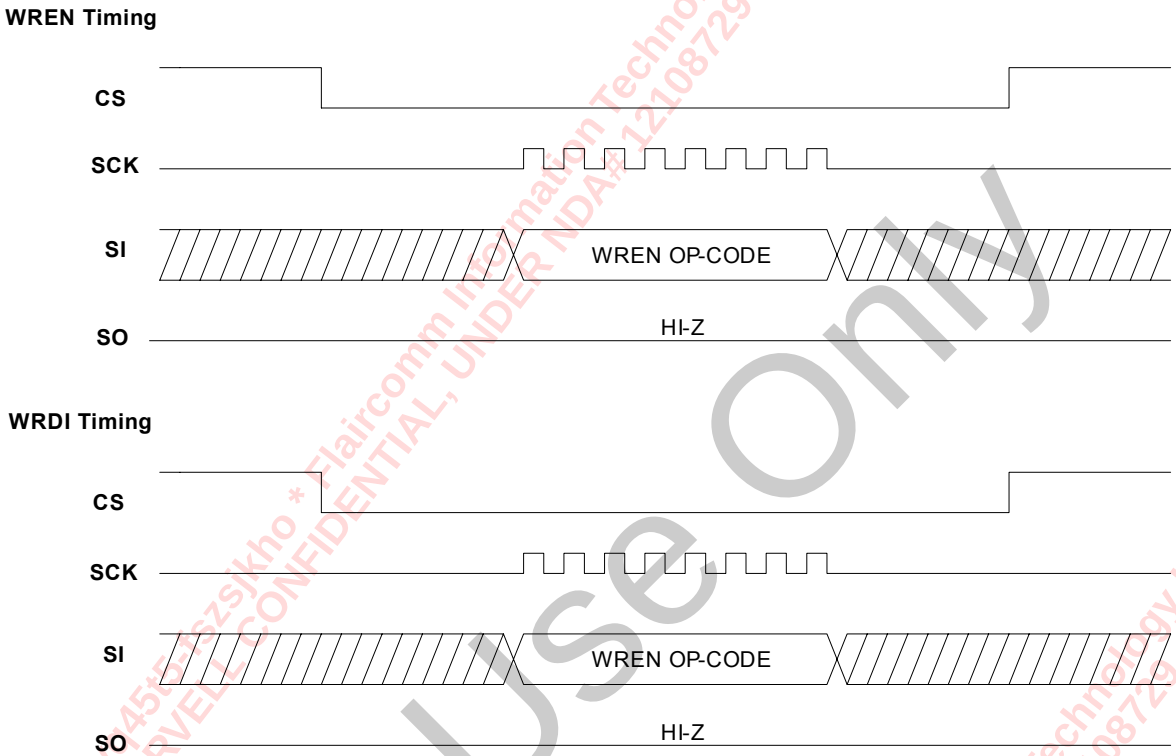


Figure 38: Write Enable and Write Disable Signal Diagrams

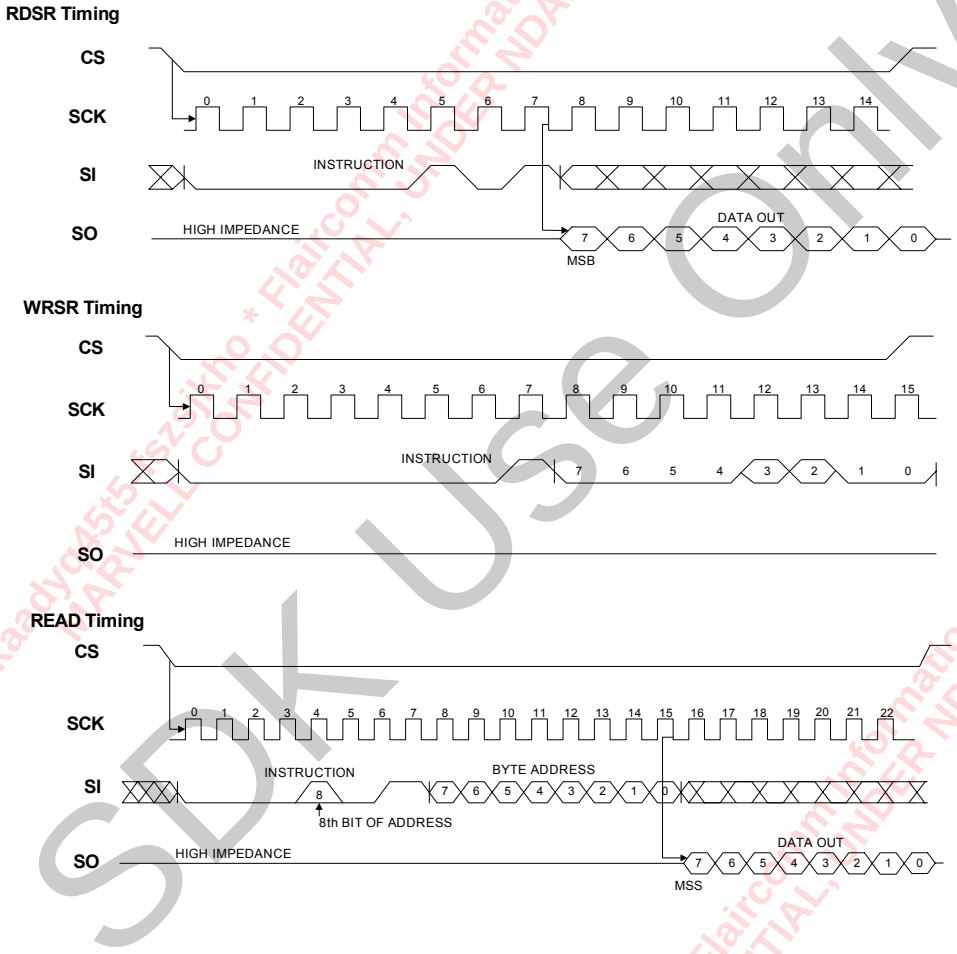


5.4.5.4.2 Byte Read

The 88W8686 supports the following read instructions.

- READ—Simple Read instruction
- RDSR—Read the EEPROM Status Register

Figure 39: Byte Read Signal Diagram



5.5 UART

The 88W8686 supports a Universal Asynchronous Receiver/Transmitter (UART) interface, compliant to the industry standard 16550 specification. The UART is connected to the PBU of the device.

The UART interface features include:

- FIFO mode permanently selected for transmit and receive operations
- Two pins for transmit and receive operations
- Additional flow controls available through the GPIO pins

The UART interface operation includes:

- Upload boot code to the internal CPU (for debug purposes)
- Support diagnostic tests
- Support data input/output operations for peripheral devices connected through a standard UART interface (runs concurrently with the WLAN function)

The clock is used by the UART controller to generate baud rates using the following equation:

baud = (clock freq) / (16 * divisor)

Table 45: UART Clock Divisor

Baud Rate	UART Divisor UART = 176/6 MHz (29.3 MHz)	% Error	UART Divisor UART = 176/3 MHz (58.7 MHz)	% Error
2400	764	0.015	1528	0.015
4800	382	0.015	764	0.015
9600	191	0.015	382	0.015
14400	127	0.248	255	0.145
19200	95	0.512	191	0.015
28800	64	0.535	127	0.248
33600	55	0.794	109	0.116
38400	48	0.535	95	0.512
56000	33	0.794	65	0.733
57600	32	0.535	64	0.535
115200	16	0.535	32	0.535

5.5.1 UART Interface Signal Description

The 88W8686 supports the UART interface through the GPIO[3:2], GPIO[6:5], TDI, and TCK pins.

Table 46 shows the standard UART signal names on the device.

Table 46: UART Pin Definitions

88W8686 Pin Name	16550 Standard Pin Name	Description
GPIO[6]	sout	The GPIO[6] signal is the serial data output to the modem, data set, or peripheral device. The GPIO[6] signal is set high when the reset is applied.
TDI	sin	The TDI signal is the serial data input from the modem, data set, or peripheral device.

5.5.2 Booting from UART

When the CON[6:5] pins are programmed to 00 at initialization or reset, the 88W8686 firmware downloads the executable boot code via the UART interface. See Table 24: "Configuration Pins" on page 52.

When booting from the UART, the 88W8686 device has the following requirements:

Table 47: UART Boot Requirements

System Requirement	Description
Number of data bits	8 bits
Stop bits	1 bit
Parity	No parity
Baud Rate	38400

5.5.3 UART as Test Port

Test diagnostic programs may be uploaded to the CPU through the EEPROM or UART interface. During execution, the diagnostic program transmits performance and status information through the UART by performing a write to the PBU address space designated to the UART.

5.6 GPIO Interface

5.6.1 Overview

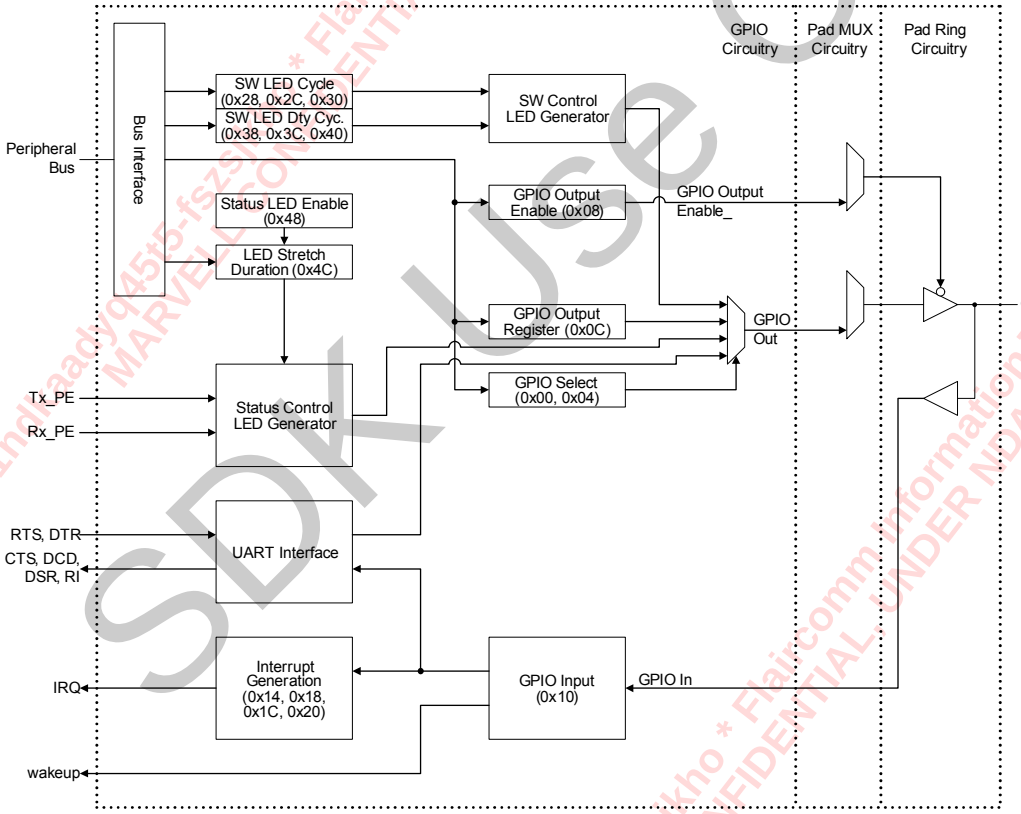
The General-Purpose I/O (GPIO) interface is used to implement user-defined input and output signals to and from the 88W8686 device, such as external interrupts, LED controlled outputs, and other user-defined I/Os.

The main features of the GPIO interface include:

- User-defined GPIOs; each I/O configured to either input or output
- Each GPIO independently controlled
- Each I/O configurable to output bit from GPIO_OUT[6:0] and GPIO_OUT[14:11].

Figure 40 shows a block diagram of the 88W8686 GPIO Unit (GPU). This circuitry exists for each of the GPIO pins, although some functions may be implemented only on certain pins.

Figure 40: GPU Block Diagram



5.6.2 GPIO Functions

Table 48 shows the functions associated with each GPIO pin.

Note

The number of GPIO pins is dependent upon the package. See Section 1. "Package and Power" on page 17 for the number of available GPIO pins on each package type.

Table 48: GPIO Functions

GPIO Function	GPIO Pin														
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
General Purpose Output	X	X	X	X	X	X	X	RESERVED	RESERVED	RESERVED	RESERVED	X	X	X	X
General Purpose Input	X	X	X	X	X	X	X					X	X	X	X
LED Status	--	X[1]	--	--	--	--	--					--	--	--	--
External Wakeup	--	--	--	--	X	--	--					--	--	--	--
External Interrupt	X	X	X	X	X	X	X					X	X	X	X
Firmware Controlled LED	--	X	--	--	--	--	--					--	--	--	--
UART Signals[2]	--	--	RTS	DSR	--	DTR	SO[3]					--	--	--	--
External Oscillator Control	X[4]	--	--	--	--	--	--					--	--	--	--

1. Indicates WLAN Tx power or Rx ready.
2. UART signals are also available on pins TCK and TDI.
3. UART Serial Out
4. During sleep mode, the external crystal oscillator is disabled, and if implemented, also powered down by GPIO[0].

5.6.3 LED Pulse Stretching

LED statuses on the GPIO pins can be pulse-stretched. Pulse stretching is necessary, because the duration of these status events may be too short to be observable on the LEDs. The pulse-stretch duration can be programmed via register.

5.6.4 Blink Rate

The software controlled LEDs can indicate events by blinking LEDs. For blink rate periods, see Software LED Cycle[3:0], Offset 0x28 in the Peripheral Bus registers document for register programming information.

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Section 6. Electrical Specifications

6.1 Absolute Maximum Ratings

Table 49: Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Units
VDD12	Power supply voltage with respect to VSS 88W8686 pins: VDD12	--	1.2	1.35	V
VDD18A	Power supply voltage with respect to VSS 88W8686 pins: VDD18A	--	1.8	2.3	V
VDD18_LDO	Power supply voltage with respect to VSS 88W8686 pins: VDD18_LDO	--	1.8	2.3	V
VDD30	Power supply voltage with respect to VSS 88W8686 pins: VDD30	--	3.0	4.2	V
VIO_X1	Power supply voltage with respect to VSS 88W8686 pins: VIO_X1	--	1.8	2.3	V
		--	3.3	4.2	V
VIO_X2	Power supply voltage with respect to VSS 88W8686 pins: VIO_X2	--	1.8	2.3	V
		--	3.3	4.2	V
$T_{STORAGE}$	Storage temperature	-55	--	+125	°C

6.2 Operating Conditions

Table 50: Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
VDD12	1.2V digital power supply	--	1.14	1.2	1.32	V
VDD18A	1.8V analog I/O power supply	--	1.7	1.8	1.9	V
VDD18_LDO	1.8V internal voltage supply	--	1.62	1.8	1.98	V
VDD30	3.0V digital I/O power supply	--	2.7	3.0	3.3	V
VIO_X1	Host Interface digital I/O power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.63	V
VIO_X2	Digital I/O power supply	--	1.62	1.8	1.98	V
		--	2.97	3.3	3.63	V
T_A	Ambient operating temperature	--	-30	--	85	°C
T_J	Maximum junction temperature	--	--	--	125	°C

6.2.1 Internal Operating Frequencies

Table 51: Internal Operating Frequencies

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SYSCLK}	CPU clock speeds See Section 6.10 "Power Consumption" on page 138.	--	--	5.5, 11, 16, 20, 22, 32, 40, 44, 64, 80, 106, 128	--	MHz

Note

Table 51 refers to the internal system and CPU clock. For information on the allowable reference clock frequencies, see Section 6.6 "Network" on page 121.

6.3 Digital Pad Ratings

See Section 1.5 "Power" on page 40 for a list of the pins operating from each voltage supply.

6.3.1 3V Pads

Table 52: DC Electricals—3V Pads (VDD30)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	1.0	--	1.2	V
V_{IL}	Input low voltage	--	0.6	--	0.8	V
V_{HYS}	Input hysteresis	--	250	--	--	mV
V_{OH}	Output high voltage	I_{OH}(max) = 13.5 mA[1]	2.3	--	--	V
V_{OL}	Output low voltage	I_{OL}(max) = 12 mA[2]	--	--	0.4	V

1. I_{OH} is the maximum current draw to maintain a mininum V_{OH} level.
2. I_{OL} is the maximum sink current to maintain a maximum V_{OL} level.

6.3.2 1.8V/3.3V Pads

Table 53: DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2)

Symbol	Parameter	Condition	Mode	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	1.8V	1.2	--	V18+0.3	V
		--	3.3V	2.0	--	V33+0.3	V
V_{IL}	Input low voltage	--	1.8V	-0.3	--	0.6	V
		--	3.3V	-0.3	--	1	V
V_{HYS}	Input hysteresis	--	1.8V	250	--	--	mV
		--	3.3V	300	--	--	mV

Table 53: DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2) (Continued)

Symbol	Parameter	Condition	Mode	Min	Typ	Max	Units
V_{OH}	Output high voltage	SR[1] = Slew Rate[2] SR: 3 — I_{OH}(max): 16 mA SR: 2 — I_{OH}(max): 16 mA SR: 1 — I_{OH}(max): 5 mA SR: 0 — I_{OH}(max): 5 mA	1.8V	1.22	--	--	V
		SR = Slew Rate SR: 3 — I_{OH}(max): 16.5 mA SR: 2 — I_{OH}(max): 16.5 mA SR: 1 — I_{OH}(max): 5.5 mA SR: 0 — I_{OH}(max): 5.5 mA	3.3V	2.57	--	--	V
V_{OL}	Output low voltage	SR = Slew Rate[3] SR: 3 — I_{OL}(max): 23 mA SR: 2 — I_{OL}(max): 15.5 mA SR: 1 — I_{OL}(max): 7.5 mA SR: 0 — I_{OL}(max): 7.5 mA	1.8V	--	--	0.4	V
		SR = Slew Rate SR: 3 — I_{OL}(max): 23.5 mA SR: 2 — I_{OL}(max): 15.5 mA SR: 1 — I_{OL}(max): 7.5 mA SR: 0 — I_{OL}(max): 7.5 mA	3.3V	--	--	0.4	V
I_pullup[4]	--	--	--	16	22	29	µA
I_pulldown	--	--	--	12	23	33	µA
I_pullup_weak	--	--	--	--	--	10	µA
I_pulldown_weak	--	--	--	--	--	10	µA

1. Slew rate that controls the output drive strength and rise/fall time of the pad.
2. I_{OH} is the maximum current draw to maintain a mininum V_{OH} level.
3. I_{OL} is the maximum sink current to maintain a maximum V_{OL} level.
4. There are two types of pull-up/pull-down pads—regular and weak. Each pad type (regular and weak) has different internal resistor values.

6.4 Package Thermal Conditions

6.4.1 68-Pin QFN Package

Table 54: Thermal Conditions—68-Pin (8x8x1 mm)

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance[1] Junction to ambient of package. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	25.6	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	22.5	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	21.4	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	20.8	°C/W
ψ_{JT}	Thermal characteristic parameter[1] Junction to top center of package. $\psi_{JT} = (T_J - T_{TOP})/P$ T_{TOP} = temperature on top center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	0.36	°C/W
ψ_{JB}	Thermal characteristic parameter[1] Junction to top center of package. $\psi_{JT} = (T_J - T_B)/P$ T_B = power dissipation from top center of package	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	12.2	°C/W
θ_{JC}	Thermal resistance[1] Junction to case of the package $\theta_{JC} = (T_J - T_C)/ P_{Top}$ P_{Top} = power dissipation from top of package	JEDEC 4-layer PCB no air flow	8.9	°C/W
θ_{JB}	Thermal resistance[1] Junction to board of package $\theta_{JB} = (T_J - T_B)/ P_{bottom}$ P_{bottom} = power dissipation from bottom of package to PCB surface	JEDEC 4-layer PCB no air flow	12.4	°C/W

1. Refer to white paper on AN-63 Thermal Calculations for more information.

6.4.2 Flip Chip

Table 55: Flip Chip Thermal Conditions—280 µm Pitch[1]

Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance Junction to ambient of device. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	50.7	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	47.1	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	45.1	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	40.8	°C/W

1. Refer to white paper on AN-63 Thermal Calculations for more information.

Table 56: Flip Chip Thermal Conditions—500 µm Pitch[1]

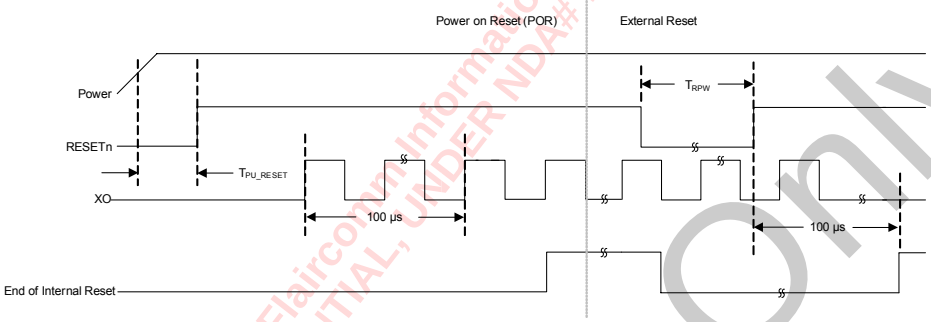
Symbol	Parameter	Condition	Typ	Units
θ_{JA}	Thermal resistance Junction to ambient of device. $\theta_{JA} = (T_J - T_A)/ P$ P = total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB no air flow	48.1	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 1 meter/sec air flow	44.6	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 2 meter/sec air flow	42.7	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB 3 meter/sec air flow	39.7	°C/W

1. Refer to white paper on AN-63 Thermal Calculations for more information.

6.5 Processor

6.5.1 Reset Specifications

Figure 41: Reset and Configuration Timing



Notes

- RESETn is not needed for proper operation due to internal power-on reset logic.
- For DC and AC specifications, see Section 6.8.3 "GPIO Specifications" .

Table 57: External Timing Requirements (RESETn Pin)
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESETn de-asserted	--	0	--	--	ms
T_{RPW}[1]	RESETn pulse width	--	10[2]	100	--	ns

1. For external reset, the device reset time is T_{RPW} + 300 µs.
2. Minimum value guaranteed for a valid reset. Smaller values may trigger the reset circuit.

Table 58: Internal Reset Timing
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
--	Negative internal reset pulse width	--	100	100	--	µs

6.5.2 Configuration Pin Specifications

For a list of configuration pins, see Section 2.5.4 "Configuration Pins" on page 52.

6.5.2.1 Pull-Up Resistance

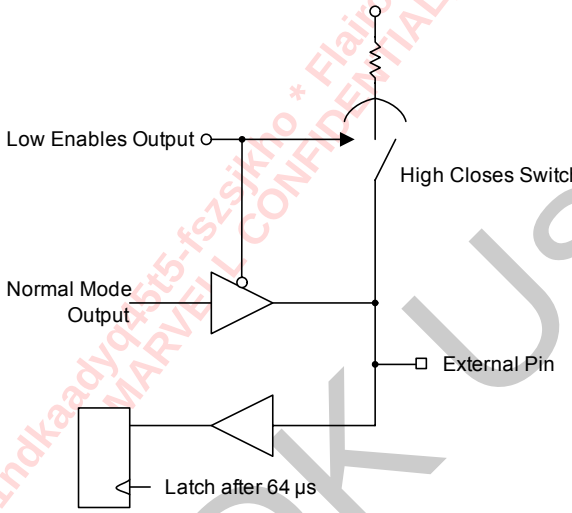
Table 59: Configuration Pin Serial Interface[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{PUP_RESET}	Internal pull-up resistance	0-64 µs following any reset	--	800	--	kΩ

1. After 64 µs, the configuration pins become functional output pins where the internal pull-up will be disabled.

Figure 42: Configuration Pin Diagram



6.6 Network

6.6.1 Wireless LAN

6.6.1.1 Input Clock Modes

Table 60: DC Coupled Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high voltage	--	VDD18A - 0.5	--	VDD18A + 0.5	V
V_{IL}	Input low voltage	--	0	--	0.4	V

Table 61: AC Coupled Mode

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{PP}	Peak to Peak input voltage	--	0.4	--	1.8	Vpk-pk

Table 62: Phase Noise

Parameter	Test Conditions	Temp (°C)	Min	Typ	Max	Units
Reference Clock Phase Noise Requirement	Offset = 1 kHz	Full	--	--	-135	dBc/Hz
	Offset = 10 kHz	Full	--	--	-145	dBc/Hz
	Offset = 100 kHz	Full	--	--	-145	dBc/Hz
	Offset > 1 MHz	Full	--	--	-150	dBc/Hz

Note

For DC and AC coupled modes, typical input capacitance is approximately 2 pF and input resistance is >20 kΩ. For AC coupled mode, the Duty Cycle is 50% ±5%.

6.6.1.2 Input Clock Specifications

Table 63: 19.2 MHz Clock Timing
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_XO19\_2}$	XO19_2 period	--	52.083 - 20 ppm	52.083	52.083 + 20 ppm	ns
$T_{H\_XO19\_2}$	XO19_2 high time	--	20.8332	26.0415	31.2498	ns
$T_{L\_XO19\_2}$	XO19_2 low time	--	20.8332	26.0415	31.2498	ns
$T_{R\_XO19\_2}$	XO19_2 rise time	--	--	--	5	ns
$T_{F\_XO19\_2}$	XO19_2 fall time	--	--	--	5	ns

Table 64: 20 MHz Clock Timing
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XO20}	XO20 period	--	50.000 - 20 ppm	50.000	50.000 + 20 ppm	ns
T_{H_XO20}	XO20 high time	--	20.000	25.000	30.000	ns
T_{L_XO20}	XO20 low time	--	20.000	25.000	30.000	ns
T_{R_XO20}	XO20 rise time	--	--	--	5	ns
T_{F_XO20}	XO20 fall time	--	--	--	5	ns

Table 65: 24 MHz Clock Timing
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XO24}	XO24 period	--	41.6667 - 20 ppm	41.6667	41.6667 + 20 ppm	ns
T_{H_XO24}	XO24 high time	--	16.6667	20.8333	25.000	ns
T_{L_XO24}	XO24 low time	--	16.6667	20.8333	25.000	ns
T_{R_XO24}	XO24 rise time	--	--	--	5	ns
T_{F_XO24}	XO240 fall time	--	--	--	5	ns

Table 66: 26 MHz Clock Timing
NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XO26}	XO26 period	--	38.462 - 20 ppm	38.462	38.462 + 20 ppm	ns
T_{H_XO26}	XO26 high time	--	15.3848	19.231	23.0772	ns
T_{L_XO26}	XO26 low time	--	15.3848	19.231	23.0772	ns
T_{R_XO26}	XO26 rise time	--	--	--	5	ns
T_{F_XO26}	XO26 fall time	--	--	--	5	ns

Table 67: 38.4 MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P\_XO38\_4}$	XO38_4 period	--	26.042 - 20 ppm	26.042	26.042 + 20 ppm	ns
$T_{H\_XO38\_4}$	XO38_4 high time	--	10.4168	13.021	15.6252	ns
$T_{L\_XO38\_4}$	XO38_4 low time	--	10.4168	13.021	15.6252	ns
$T_{R\_XO38\_4}$	XO38_4 rise time	--	--	--	5	ns
$T_{F\_XO38\_4}$	XO38_4 fall time	--	--	--	5	ns

Table 68: 40 MHz Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_XO40}	XO40 period	--	25.000 - 20 ppm	25.000	25.000 + 20 ppm	ns
T_{H_XO40}	XO40 high time	--	10.000	12.500	15.000	ns
T_{L_XO40}	XO40 low time	--	10.000	12.500	15.000	ns
T_{R_XO40}	XO40 rise time	--	--	--	5	ns
T_{F_XO40}	XO40 fall time	--	--	--	5	ns

6.6.1.3 External Sleep Clock Specifications

The 88W8686 external sleep clock pin is powered from the VIO_X1 voltage supply.

See Table 53, “DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2),” on page 115 for DC specifications.

6.6.1.3.1 Protocol Timing

Table 69: Sleep Clock Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
CLK	Clock Frequency Range	--	10	100	1000	kHz
T_{HIGH}	Clock high time	--	40	--	--	ns
T_{LOW}	Clock low time	--	40	--	--	ns
T_{RISE}	Clock rise time	--	--	--	5	ns
T_{FALL}	Clock fall time	--	--	--	5	ns

6.6.1.4 Crystal

Table 70: Crystal Specifications

Parameter	Condition	Typical	Units
Fundamental Frequency	--	19.2, 20, 24, 26, 38.4, 40	MHz
Frequency Tolerance	Over operating temperature	< ±10	ppm
	Over process at 25ºC	< ±10	ppm
SMD and AT Cut Height	--	<1.2	mm
Load Capacitor	Across	10	pF
Maximum Series Resistance	--	60	ohm
Resonance Mode	--	A1, Fundamental	--

6.6.1.5 WLAN RF

6.6.1.5.1 Receive Mode Specifications

Table 71: 802.11g/b LNA and Rx RF Mixer

Parameter	Condition	Min	Typ	Max	Units
RF Frequency Range	IEEE 802.11g/b	2400	--	2500	MHz
Total Rx Gain	Total Rx gain when LNA in high gain mode	--	87	--	dB
Rx NF at RF High Gain	Rx RF when LNA in high gain mode	--	--	5	dB
Rx Input IP3 at RF High Gain (In-Band)	Rx input IP3 when LNA in high gain mode	--	-21	--	dBm
Total Rx Gain When LNA in Low Gain 1	Total Rx gain when LNA in low gain mode 1	--	83	--	dB
Total Rx Gain When LNA in Low Gain 2	Total Rx gain when LNA in low gain mode 2	--	78	--	dB
Total Rx Gain When LNA in Low Gain 3	Total Rx gain when LNA in low gain mode 3	--	55	--	dB
RF Gain Range	--	--	32	--	dB
LNA High Gain/Low Gain Threshold	Input signal power to switch LNA from high gain to low gain	--	-30	--	dBm
Rx Input P1 dB at RF Low Gain	Transceiver 1 dB compression point when LNA in low gain mode	--	0	--	dBm
Adjacent Channel Rejection (802.11b, 11 Mbps)	Measured when the desired channel is 3 dB above sensitivity	--	48	--	dBc
Adjacent Channel Rejection (802.11g, 54 Mbps)	Measured when the desired channel is 3 dB above sensitivity	--	16	--	dBc
LO Leakage at LNA Input	2400 MHz < fleak < 2500 MHz	--	--	-90	dBm

Table 72: 802.11g/b RBB

Parameter	Condition	Min	Typ	Max	Units
Total Rx Gain When RBB at Maximum Gain	Total Rx gain when LNA in low gain mode	--	55	--	dB
Total Rx Gain When RBB at Minimum Gain	Total Rx gain when LNA in low gain mode	--	0	--	dB
RBB Gain Range	--	--	55	--	dB
Baseband I/Q Gain Mismatch	Gain mismatch between inphase and quadrature signal paths	--	--	0.3	dB
Baseband I/Q Phase Mismatch	Phase mismatch between inphase and quadrature signal paths	--	1	3	degrees
I/Q Differential Output Level	Differential output signal swing	--	0.5	--	Vop
Baseband Output Common Mode Voltage	802.11g mode	0.75	0.8	0.85	V
Baseband Output DC Offset	After DC offset calibration	--	200	--	mV
Maximum Baseband Output	Differential output swing	1	--	--	Vop
Baseband Filter 3 dB Corner Frequency	Baseband channel select filter corner frequency	8.2	8.6	9	MHz
Baseband Filter Passband Ripple	Baseband channel select filter passband ripple	--	0.5	1	dB

Table 73: 802.11a LNA and Rx RF Mixer

Parameter	Condition	Min	Typ	Max	Units
RF Frequency Range[1]	IEEE 802.11a	4900	--	5825	MHz
Total Rx Gain	Total Rx gain when LNA in high gain mode	--	68	--	dB
Rx NF at RF High Gain	Rx RF when LNA in high gain mode	--	--	7	dB
Rx Input IP3 at RF High Gain (In-Band)	Rx Input IP3 when LNA in high gain mode	--	-10	--	dBm
Total Rx Gain When LNA In Low Gain[1]	Total Rx gain when LNA in low gain mode	--	45	--	dB
RF Gain Range	--	--	23	--	dB
LNA High Gain/Low Gain Threshold	Input signal power to switch LNA from high gain to low gain	--	-23	--	dBm
Rx Input P1 dB at RF Low Gain	Transceiver 1 dB compression point when LNA in low gain mode	--	11	--	dBm
Adjacent Channel Rejection (802.11a, 54 Mbps)	Measured when the desired channel is 3 dB above sensitivity	--	15	--	dBc
LO Leakage at LNA Input	4900 MHz < fleak < 5825 MHz	--	--	-81	dBm

1. Excludes an external LNA nominal gain of 16 dB. Gain can be extended if external LNA is not used.

Table 74: 802.11a RBB

Parameter	Condition	Min	Typ	Max	Units
Total Rx Gain When RBB at Maximum Gain[1]	Total Rx gain when LNA in low gain mode	--	45	--	dB
Total Rx Gain When RBB at Minimum Gain[1]	Total Rx gain when LNA in low gain mode	--	-5	--	dB
RBB Gain Range	--	--	50	--	dB
Baseband I/Q Gain Mismatch	Gain mismatch between inphase and quadrature signal paths	--	--	0.5	dB
Baseband I/Q Phase Mismatch	Phase mismatch between inphase and quadrature signal paths	--	1	3	degrees
I/Q Differential Output Level	Differential output signal swing	--	0.5	--	Vop
Baseband Output Common Mode Voltage	802.11g mode	0.75	0.8	0.85	V
Baseband Output DC Offset	After DC offset calibration	--	200	--	mV
Maximum Baseband Output	Differential output swing	1	--	--	Vop
Baseband Filter 3 dB Corner Frequency	Baseband channel select filter corner frequency	8.2	8.6	9	MHz
Baseband Filter Passband Ripple	Baseband channel select filter passband ripple	--	0.5	1	dB

1. Excludes an external LNA nominal gain of 16 dB. Gain can be extended if external LNA is not used.

6.6.1.5.2 Transmit Mode Specifications

Table 75: Tx Mode

Parameter	Condition	Min	Typ	Max	Units
RF Frequency Range	IEEE 802.11g/b	2400	--	2500	MHz
	IEEE 802.11a	4900	--	5825	MHz
Tx Output 1 dB Compression Point	IEEE 802.11g/b	--	11	--	dBm
	IEEE 802.11a	--	7	--	dBm
Tx Carrier Suppression	Carrier suppression @ PA output	-35	--	--	dBc
Tx I/Q Suppression	I/Q suppression @ PA Output	-40	--	--	dBc
Baseband Filter 3 dB Corner Frequency	Baseband channel select filter corner frequency	10.8	11.3	11.8	MHz
Baseband Filter Passband Ripple	Baseband channel select filter passband ripple	--	0.1	0.3	dB
Tx I/Q Gain Mismatch	Gain mismatch between inphase and quadrature signal paths	--	0.1	0.2	dB
Tx I/Q Phase Mismatch	Phase mismatch between inphase and quadrature signal paths	--	1	2	degrees

6.6.1.5.3 Local Oscillator

Table 76: Local Oscillator

Parameter	Condition	Min	Typ	Max	Units
Phase Noise	Measured at 2.438 GHz at 100 kHz offset	--	--	-95	dBc/Hz
	Measured at 5.501 GHz at 100 kHz offset	--	--	-90	dBc/Hz
Integrated RMS Phase Noise at RF Output[1]	Reference clock frequency = 40 MHz 802.11a	--	1	1.2	degrees
	Reference clock frequency = 40 MHz 802.11g/b	--	0.6	0.7	degrees
Frequency Resolution	--	--	--	1	kHz

1. RMS phase noise is integrated from 1 kHz to 10 MHz.

6.6.2 Networking Coexistence

The 88W8686 Bluetooth coexistence pins are powered from the VDD18_LDO voltage supply.

Contact Marvell Field Applications Engineers for further details regarding Bluetooth coexistence protocol timing.

6.7 Host Interfaces

6.7.1 G-SPI Host Interface Specifications

The 88W8686 G-SPI host interface pins are powered from the VIO_X1 voltage supply.

See Table 53, “DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2),” on page 115 for DC specifications.

6.7.1.1 G-SPI Host Interface Protocol Timing

Figure 43: G-SPI Host Interface Transaction Timing

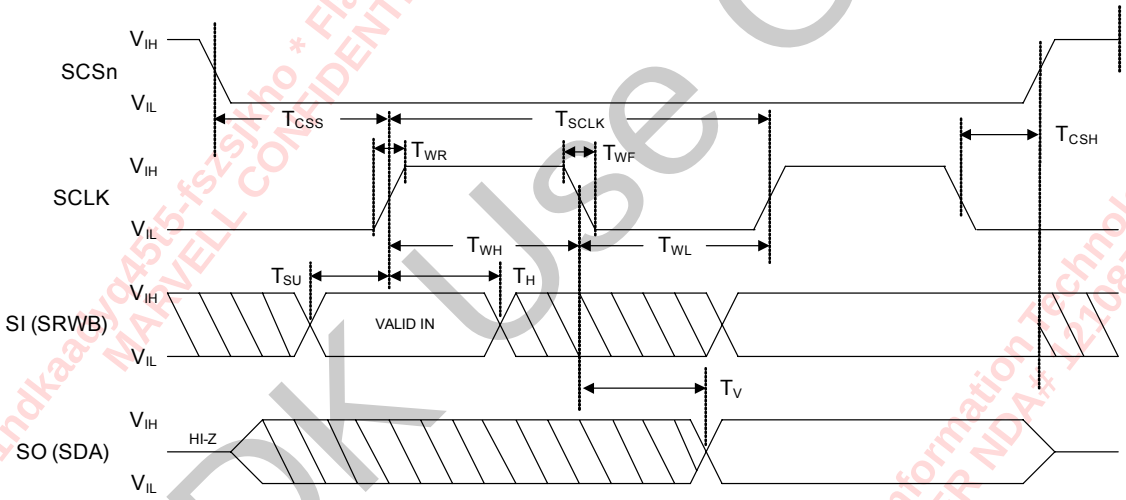


Figure 44: G-SPI Host Interface Inter-Transaction Timing

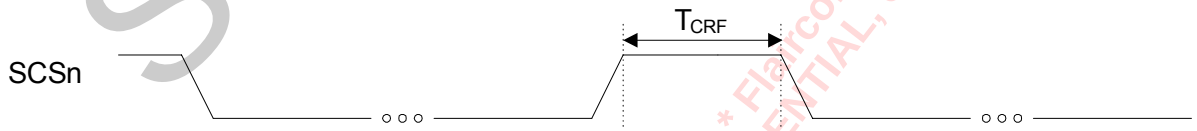


Table 77: SPI Host Interface Timing Data

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units
T_{SCLK}	Clock Period	20	--	--	ns
T_{WH}	Clock High	5	--	--	ns
T_{WL}	Clock Low	9	--	--	ns
T_{WR}	Clock Rise Time	--	--	1	ns
T_{WF}	Clock Fall Time	--	--	1	ns
T_{H}	SDI Hold Time	2.5	--	--	ns
T_{SU}	SDI Setup Time	2.5	--	--	ns
T_{V}	SDO Hold Time	5	--	--	ns
T_{CSS}	SCSn Fall to Clock	5	--	--	ns
T_{CSH}	Clock to SCSn Rise	0	--	--	ns
T_{CRF}	SCSn Rise to SCSn Fall	400	--	--	ns

6.7.2 SDIO Specifications

The 88W8686 SDIO host interface pins are powered from the VIO_X1 voltage supply.

See Table 53, “DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2),” on page 115 for DC specifications.

The SDIO electrical specifications are identical for the 1-bit SDIO, 4-bit SDIO, and SPI modes.

6.7.2.1 SDIO Protocol Timing

Figure 45: SDIO Protocol Timing Diagram

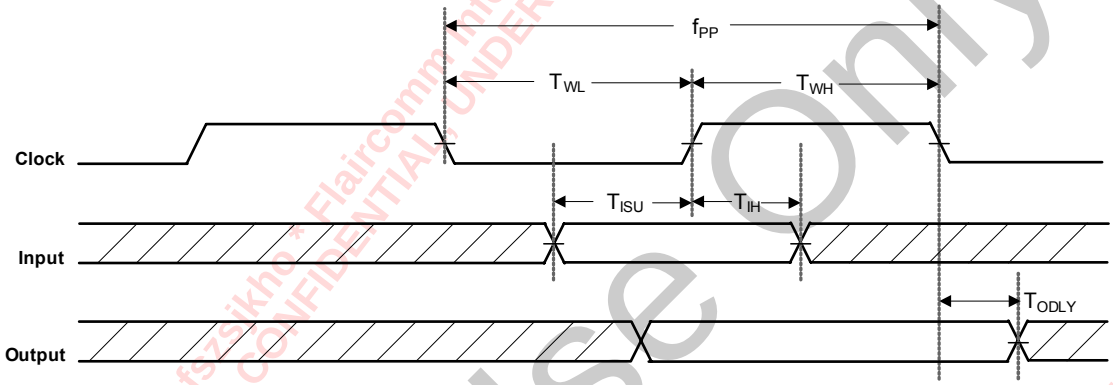
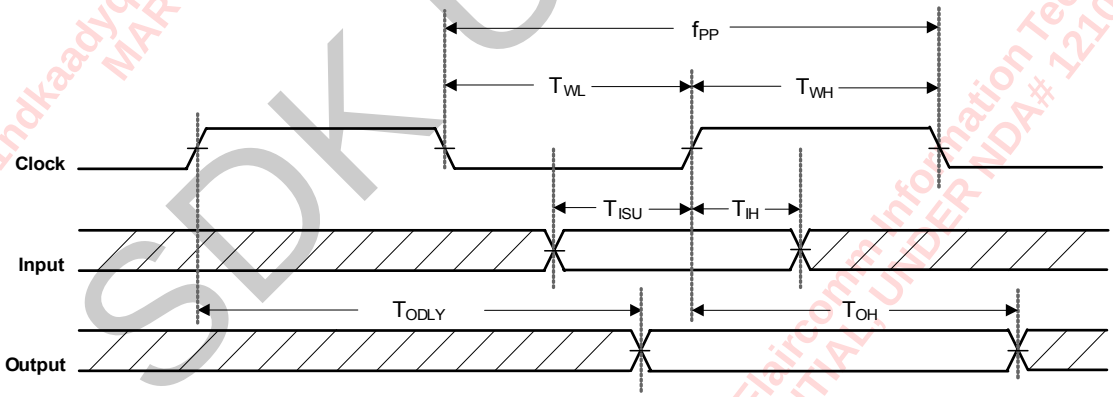


Figure 46: SDIO Protocol Timing Diagram—High Speed Mode



Note

The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

Table 78: SDIO Timing Data

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{PP}	Clock Frequency	Normal	0	--	25	MHz
		High Speed	0	--	50	MHz
T_{WL}	Clock Low Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{WH}	Clock High Time	Normal	10	--	--	ns
		High Speed	7	--	--	ns
T_{ISU}	Input Setup Time	Normal	5	--	--	ns
		High Speed	6	--	--	
T_{IH}	Input Hold Time	Normal	5	--	--	ns
		High Speed	2	--	--	
T_{ODLY}	Output Delay Time	--	0	--	14	ns
T_{OH}	Output Hold Time	High Speed	2.5	--	--	ns

6.8 Peripheral Bus Interface

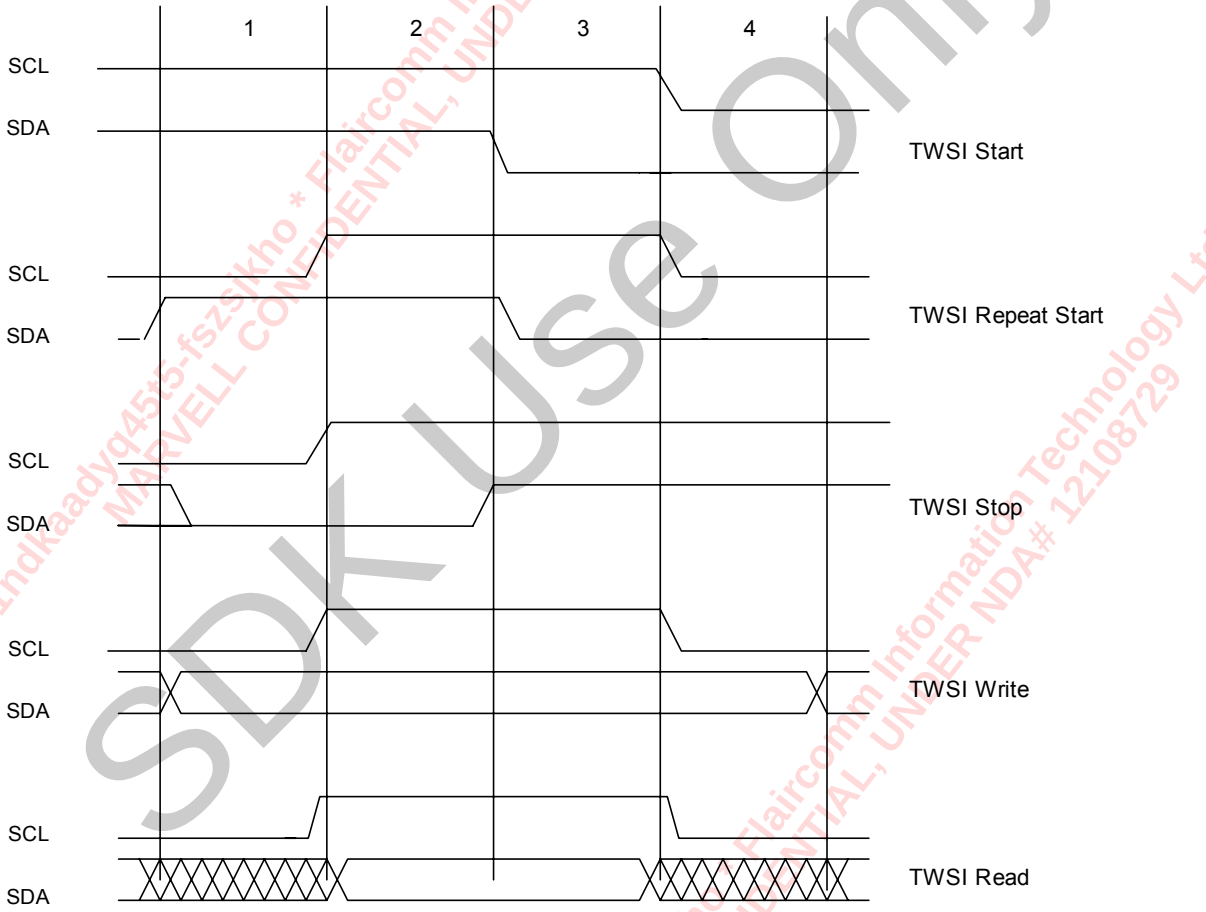
6.8.1 Clocked Serial Unit

The 88W8686 CSU pins are powered from the VIO_X2 voltage supply.

See Table 53, “DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2),” on page 115 for DC specifications.

6.8.1.1 TWSI Protocol Timing

Figure 47: TWSI Signalling



6.8.1.2 SPI Serial Interface Protocol Timing

Figure 48: SPI Serial Interface Timing Diagram

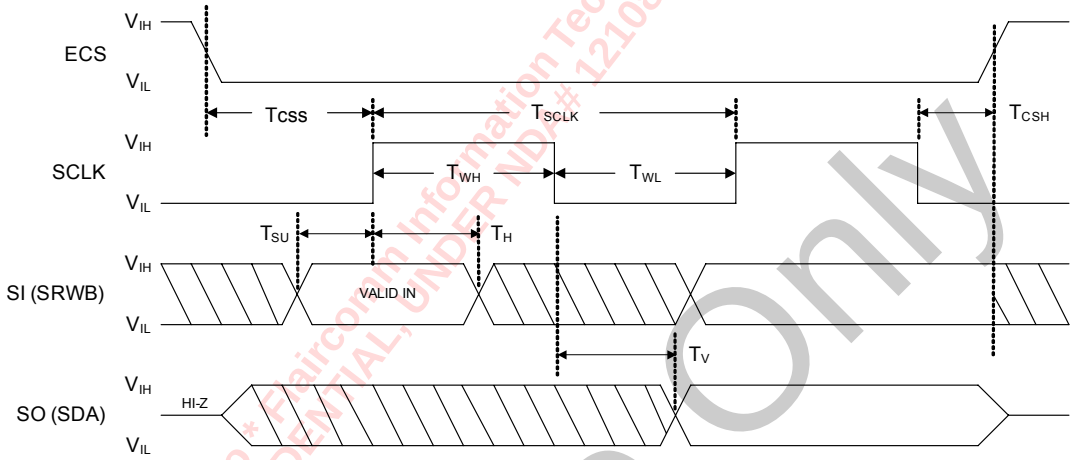


Table 79: Serial Interface Timing Data[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CSS}	Chip select setup time	--	--	1/(2*SCLK)	--	ns
T_{CSH}	Chip select hold time	--	--	1/(2*SCLK)	--	ns
T_{SCLK}	SCLK period[2]	--	$2/f_{SYSCLK}$	--	$2^{17}/f_{SYSCLK}$	ns
T_{WH}	SCLK width high	--	$1/f_{SYSCLK}$	--	$2^{16}/f_{SYSCLK}$	ns
T_{WL}	SCLK width low	--	$1/f_{SYSCLK}$	--	$2^{16}/f_{SYSCLK}$	ns
T_{SU}	Setup time (SRWB to SCLK)	--	15	--	--	ns
T_H	Hold time (SRWB from SCLK)	--	0	--	--	ns
T_V	SDA output delay (from SCLK)	--	--	--	80	ns

1. f_{SYSCLK} = system clock frequency (see Table 51, “Internal Operating Frequencies,” on page 114).
2. Internal pullup only. No external pullup. Maximum serial clock frequency limited to 5 MHz (for transceiver).

6.8.2 UART Specifications

The 88W8686 UART Tx and Rx pins are powered from the VIO_X2 voltage supply.

See Table 53, "DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2)," on page 115 for DC specifications.

6.8.3 GPIO Specifications

The 88W8686 GPIO[6:0] pins are powered from the VIO_X1 voltage supply.

The 88W8686 GPIO[14:11] pins are powered from the VIO_X2 voltage supply.

See Table 53, "DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2)," on page 115 for DC specifications.

6.8.3.1 LED Mode

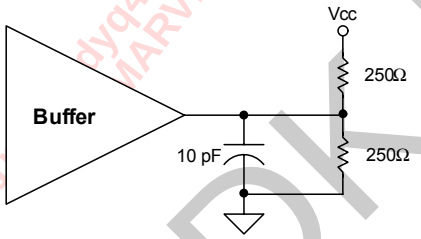
Table 80: LED Mode[1]

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Typ	Units
I_{OH}	Switching current high	Tristate on pad (requires pull-up on board)	Tristate when driving high	mA
I_{OL}	Switching current low	@ 0.4V	10	mA

1. LED Mode is independently selectable for the GPIO[1].

Figure 49: Slew Rate Measurement



6.9 Test Interface Specifications

The 88W8686 test interface pins are powered from the VIO_X2 voltage supply.

See Table 53, "DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2)," on page 115 for DC specifications.

6.9.1 Test Interface Protocol Timing

Figure 50: JTAG Timing Diagram

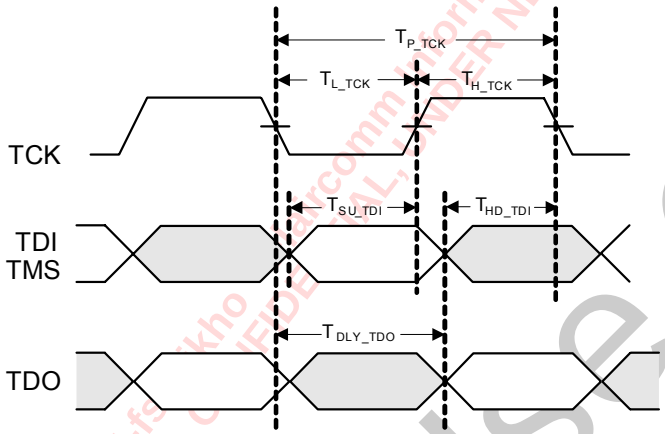


Table 81: JTAG Timing

NOTE: Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period	--	40	--	--	ns
T_{H_TCK}	TCK High	--	12	--	--	ns
T_{L_TCK}	TCK Low	--	12	--	--	ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time	--	10	--	--	ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time	--	10	--	--	ns
T_{DLY_TDO}	TCK to TDO Delay	--	0	--	15	ns

Note

Does not apply to CPU JTAG enabled by the TMS_CPU pin.

6.10 Power Consumption

Table 82: VDD12 Current Consumption
NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
$VDD12_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	35	47	mA
		Rx mode—waiting for data (802.11a)	--	40	48	mA
$VDD12_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	40	48	mA
$VDD12_{Rx11}$		Rx mode—receiving 11 Mbps data	--	41	51	mA
$VDD12_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	60	75	mA
$VDD12_{Rx54}$		Rx mode—receiving 54 Mbps data	--	65	81	mA
$VDD12_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	60	74	mA
$VDD12_{Rx54}$		Rx mode—receiving 54 Mbps data	--	70	87	mA
$VDD12_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	35	42	mA
$VDD12_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	30	37	mA
$VDD12_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	40	48	mA
$VDD12_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	40	50	mA
$VDD12_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	40	53	mA
$VDD12_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	40	53	mA

NOTE: Values based on an outside 1.2V supply and a disabled internal LDO.
If the internal LDO is used, VDD12 can be left floating.

Table 83: VDD18A Current Consumption
NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
$VDD18_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	88	101	mA
		Rx mode—waiting for data (802.11a)	--	88	101	mA
$VDD18_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	122	140	mA
$VDD18_{Rx11}$		Rx mode—receiving 11 Mbps data	--	123	141	mA
$VDD18_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	125	143	mA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	125	143	mA
$VDD18_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	132	152	mA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	133	153	mA
$VDD18_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	110	127	mA
$VDD18_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	115	133	mA
$VDD18_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	115	133	mA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	115	133	mA
$VDD18_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	121	139	mA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	119	137	mA

Table 84: VDD18_LDO Current Consumption
NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
$VDD18_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	35	47	mA
		Rx mode—waiting for data (802.11a)	--	40	48	mA
$VDD18_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	40	48	mA
$VDD18_{Rx11}$		Rx mode—receiving 11 Mbps data	--	45	57	mA
$VDD18_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	60	75	mA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	65	80	mA
$VDD18_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	60	74	mA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	70	87	mA
$VDD18_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	30	42	mA
$VDD18_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	30	42	mA
$VDD18_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	45	58	mA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	50	59	mA
$VDD18_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	45	53	mA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	45	53	mA

NOTE: The VDD18_LDO supply powers both the internal LDO (if enabled) and the Bluetooth coexistence pins. Even if the internal LDO is disabled, the VDD18_LDO supply must be present when using the Bluetooth coexistence pins. This table shows the VDD18_LDO supply current with the internal LDO enabled. The Bluetooth coexistence pins consume a very small amount of current due to a very slow toggling rate.

Table 85: VDD30 Current Consumption
NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
$VDD30_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	45	56	µA
		Rx mode—waiting for data (802.11a)	--	24	30	µA
$VDD30_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	45	56	µA
$VDD30_{Rx11}$		Rx mode—receiving 11 Mbps data	--	45	56	µA
$VDD30_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	45	56	µA
$VDD30_{Rx54}$		Rx mode—receiving 54 Mbps data	--	45	56	µA
$VDD30_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	25	30	µA
$VDD30_{Rx54}$		Rx mode—receiving 54 Mbps data	--	25	30	µA
$VDD30_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	1480	1850	µA
$VDD30_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	1410	1762	µA
$VDD30_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	526	657	µA
$VDD30_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	293	366	µA
$VDD30_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	53	66	µA
$VDD30_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	39	48	µA

Table 86: VIO_X1 Current Consumption
NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
Used as 1.8V Supply						
$VIO\_X1_{CLK\_Data}$	SDIO Host Interface Clock/ Data Toggling	16 MHz clock frequency	--	1.5	1.9	mA
		25 MHz clock frequency	--	2.1	2.6	mA
		50 MHz clock frequency	--	4.2	5.3	mA
Used as 3.3V Supply						
$VIO\_X1_{CLK\_Data}$	SDIO Host Interface Clock/ Data Toggling	16 MHz clock frequency	--	3	3.8	mA
		25 MHz clock frequency	--	4.2	5.2	mA
		50 MHz clock frequency	--	8.4	10	mA

Table 87: VIO_X2 Current Consumption

NOTE: System clock = 40 MHz, 802.11 MAC clock = 40 MHz CPU clock = 40 MHz
No pin toggling activity on VIO_X2 supply during measurement.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Used as 1.8V Supply						
$VDD18_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	47	58	µA
		Rx mode—waiting for data (802.11a)	--	50	62	µA
$VDD18_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	47	58	µA
$VDD18_{Rx11}$		Rx mode—receiving 11 Mbps data	--	47	58	µA
$VDD18_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	47	58	µA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	47	58	µA
$VDD18_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	50	62	µA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	50	62	µA
$VDD18_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	47	58	µA
$VDD18_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	47	58	µA
$VDD18_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	47	58	µA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	47	58	µA
$VDD18_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	50	62	µA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	50	62	µA
Used as 3.3V Supply						
$VDD18_{RxI}$	Rx Idle	Rx mode—waiting for data (802.11g/b)	--	80	100	µA
		Rx mode—waiting for data (802.11a)	--	80	100	µA
$VDD18_{Rx1}$	802.11b	Rx mode—receiving 1 Mbps data	--	80	100	µA
$VDD18_{Rx11}$		Rx mode—receiving 11 Mbps data	--	80	100	µA
$VDD18_{Rx24}$	802.11g	Rx mode—receiving 24 Mbps data	--	80	100	µA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	80	100	µA
$VDD18_{Rx24}$	802.11a	Rx mode—receiving 24 Mbps data	--	80	100	µA
$VDD18_{Rx54}$		Rx mode—receiving 54 Mbps data	--	80	100	µA
$VDD18_{Tx1}$	802.11b	Tx mode—transmitting 1 Mbps data	--	80	100	µA
$VDD18_{Tx11}$		Tx mode—transmitting 11 Mbps data	--	80	100	µA
$VDD18_{Tx24}$	802.11g	Tx mode—transmitting 24 Mbps data	--	80	100	µA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	80	100	µA
$VDD18_{Tx24}$	802.11a	Tx mode—transmitting 24 Mbps data	--	80	100	µA
$VDD18_{Tx54}$		Tx mode—transmitting 54 Mbps data	--	80	100	µA

Section 7. Part Order Numbering/Package Marking

7.1 Part Order Numbering

Figure 51 shows the part order numbering scheme for the device. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 51: Sample Part Number

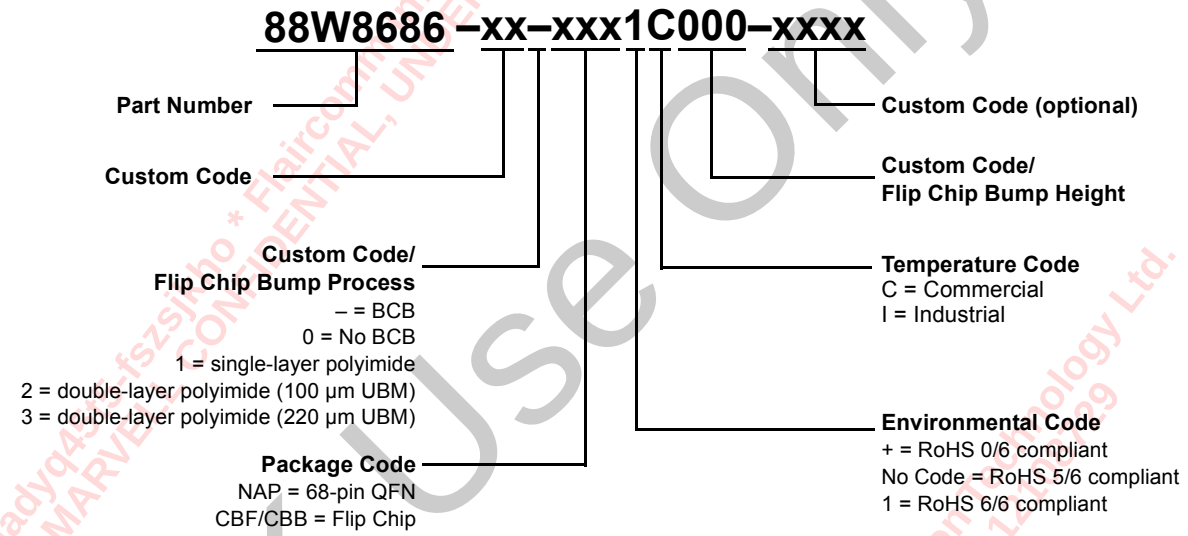


Table 88: Part Order Options

Package Type	Part Order Number
68-pin QFN 8x8 mm Tray	88W8686-xx-NAP1C000
68-pin QFN 8x8 mm Tape-and-Reel	88W8686-xx-NAP1C000-P123
280 µm Pitch Flip Chip Tape-and-Reel	88W8686-xx2CBF1-B115-T
500 µm Pitch Flip Chip Tape-and-Reel (100 µm UBM)	88W8686-xx2CBB1-B115-T
500 µm Pitch Flip Chip Tape-and-Reel (220 µm UBM)	88W8686-xx3CBB1-B115-T

Note

Part ordering options are for 2.4 GHz operation. 5 GHz is currently not supported in production.

7.2 Package Marking

Figure 52 shows a sample commercial package marking and pin 1 location for the device.

Figure 52: Sample Package Marking and Pin 1 Location

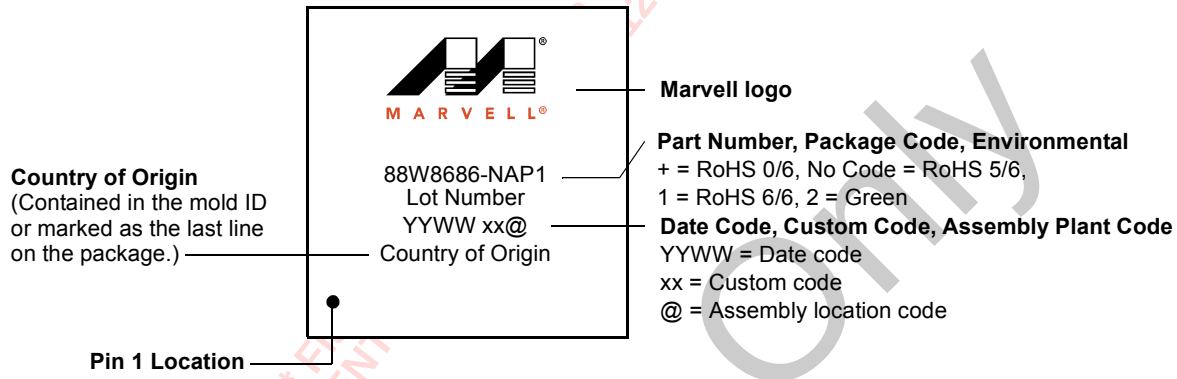
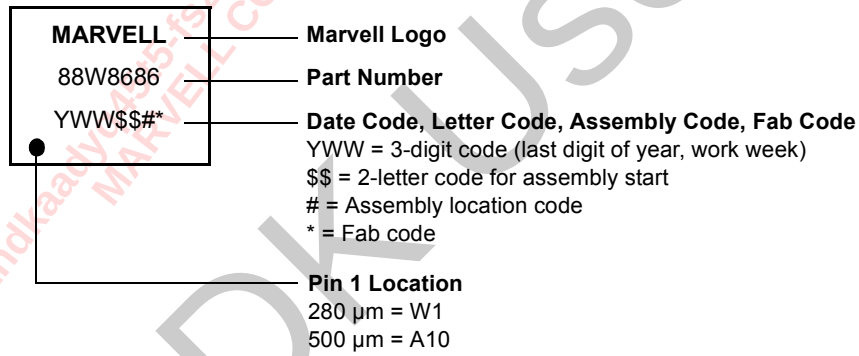


Figure 53: Flip Chip Package Marking and Pin 1 Location—View from Non-Bump Side



Note

Above drawings are not drawn to scale. Marking locations are approximate.

Appendix A. Flip Chip Underfill Requirement

A.1 Overview

This section provides packaging compatibility information for flip chip packaging used with Marvell 88W8686 embedded WLAN single-chip devices.

A.2 Bump Composition

Figure 54 shows a diagram of the solder bump composition. The composition of the solder bump is lead-free. Table 89 shows the values for 280 µm and 500 µm pitch bumps.

Figure 54: Solder Bump Composition

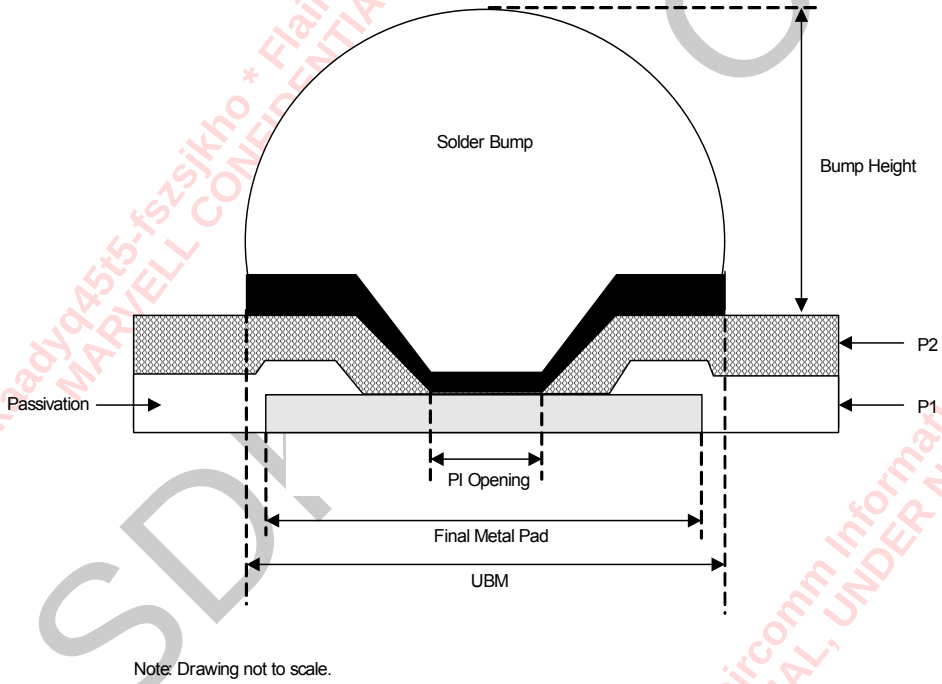


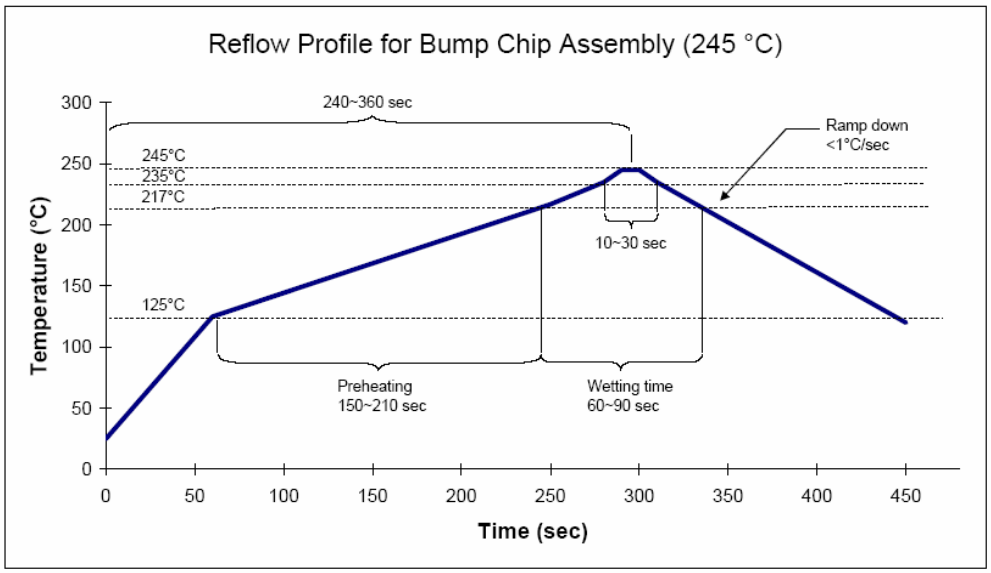
Table 89: Solder Bump Composition Values

Parameter	Pitch	
	280 µm	**500 µm**
Bump Height	115 ±15 µm	115 ±15 µm
PI Opening	70 µm	70 µm
Final Metal Pad	145 µm	194.5 µm
UBM	115 µm	220 µm

A.3 Reflow Profile

The composition of the flip chip packaging is lead-free. Use a lead-free heating profile with a peak of 245°C. Figure 55 shows the recommended reflow profile.

Figure 55: Reflow Profile



Preheat Ramp-up Rate	125°C to 217°C < 1°C / sec
Time at T > 217°C	60 sec to 90 sec
Peak Temperature	245°C
Cooling Ramp-down Rate	< 1°C / sec
Time From 25°C to peak	240s to 360 sec

A.4 Additional Assembly Recommendations

Marvell recommends that customers use 13-Zone Reflow Oven for flip chip mounting—10 zones for heating up and 3 zones for cooling down. The cooling ramp down rate is less than 1°C per second from peak temperature to 25°C. Mount the flip chip as the last component on the PCB/motherboard. After the flip chip is mounted on PCB/motherboard, proceed with the tasks in the following order:

1. Perform electrical test for the flip chip without underfill material.
2. Proceed with any rework needed on the flip chip.
3. After flip chip passing electrical testing, apply underfill material to the flip chip.

A.5 Footprint on Datasheet

The flip chip footprint shown in the 88W8686 datasheet is "pad up". In the description, this is a pad location relative to die center. This is from the perspective of looking at the device from the same side as the bumps. This will cause the footprint to be inverted on the Y-axis for proper placement.

A.6 Flux Requirements

"No Clean" flux is required for assembly of these parts, as it is not possible to clean the area under the parts after assembly. This flux should also be "tacky" to hold the parts in place during heating.

A.7 Underfill Recommendations

Customers with flip chip or bare-die assembly experience must select an underfill for their production assembly. Underfill must be selected based on the PCB/resin/substrate type, and the selection of underfill will vary from customer-to-customer.

Marvell has qualified the 88W8686 WLCPS package with Non Solder Mask Define substrates (made with BT or FR4 material) and underfilled with Nagase ChemteX Corp R3434iHX-2 advanced underfill encapsulant. Reliability studies show that proper use of this combination results in a reliable assembly. Therefore, Marvell recommends this for use with the 88W8686 WLCSP.

Marvell has no data on other combinations and recommends that customers perform their own due diligence in establishing the reliability risk of their chosen combination. For application of Nagase underfill type R3434iHX-2, contact the Sales department at Nagase ChemteX Corp or visit Nagase ChemteX website at http://www.nagasechemtex.co.jp/english/.

Recommended underfill material:

- Brand—Nagase ChemteX Corporation
- Product Number—Nagase UF TDS-R3434iHX-2

A.8 Pad/Solder Mask Guidelines

Figure 56 and shows the spacing required for pad and solder mask for (Non Solder Mask Design) board layout. Table 90 shows the values for 280 µm and 500 µm pitch bumps.

Figure 56: Pad Guidelines—NSMD PCB Design

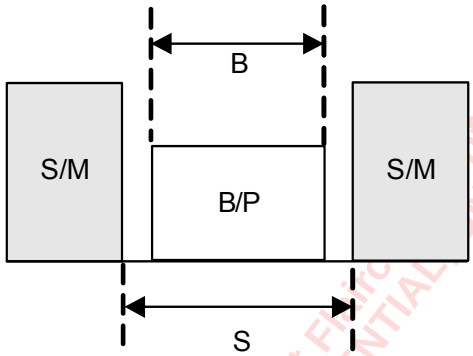


Table 90: Pad Guideline Values[1]

Parameter	Recommendation	
	280 µm	500 µm
"B" Bump Pad Diameter on NSMD PCB	115 µm	220 µm
"S" Solder Mask Opening	175 µm	280 µm

1. NSMD = Non Solder Mask Define. S/M = Solder Mask.

Appendix B. Acronyms and Abbreviations

Table 91: Acronyms and Abbreviations

Acronym	Definition
ABR	Automatic Baud Rate
ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AFC	Automatic Frequency Correction
AFH	Adaptive Frequency Hopping
AGC	Automatic Gain Control
AIFS	Arbitration Interframe Space
AP	Access Point
API	Application Program Interface
ARM	Advanced RISC Machine
ATIM	Announcement Traffic Indication Message
BAMR	Base Address Mask Register
BAR	Base Address Register
BBU	Baseband Processor Unit
BCB	Benzocyclobutene (flip chip bump process)
BOM	Bill of Materials
BSS	Basic Service Set
BSSID	Basic Service Set ID
BTU	Bluetooth Baseband Unit
BRF	Bluetooth RF Unit
BWQ	Bandwidth Queue
CBP	Contention-Based Period
CCA	Clear Channel Assessment
CCK	Complementary Code Keying
CCMP	Counter Mode CBC-MAC Protocol
CDE	Close Descriptor Enable

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
CFP	Contention-Free Period
CFQ	Contention-Free Queue
CID	Connection Identifier
CIS	Card Information Structure
CIU	CPU Interface Unit
CMD	Command
CMQ	Control Management Queue
CRC	Cyclic Redundancy Check
CS	Card Select
CSMA/CA	Carrier Sense Multiple Access / Collision Avoidance
CSMA/CD	Carrier Sense Multiple Access / Collision Detection (802.3 MAC)
CSU	Clocked Serial Unit
CTS	Clear to Send
DAC	Digital to Analog Converter
DBPSK	Differential Binary Phase Shift Keying
DCD	Device Controller Driver
DCE	Data Communication Equipment
DCF	Distributed Coordination Function
DCLA	Direct Current Level Adjustment
DCU	DMA Controller Unit
DFS	Dynamic Frequency Selection
DIFS	Distributed Interframe Space
DMA	Direct Memory Access
dQH	Device Queue Head
DQPSK	Differential Quadrature Phase Shift Keying
DSM	Distribution System Medium
DSP	Digital Signal Processor
dTD	Linked List Transfer Descriptors
DTIM	Delivery Traffic Indication Map
ED	Energy Detect
EDCA	Enhanced Distributed Channel Access

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
EEPROM	Electrically Erasable Programmable Read Only Memory
EFU	eFuse Unit
EIFS	Extended Interframe Space
ERP-OFDM	Extended Rate PHY-Orthogonal Frequency Division Multiplexing
FAE	Field Application Engineer
FIFO	First In First Out
FIPS	Federal Information Processing Standards
FIQ	Fast Interrupt Request
FM	Frequency Modulation
FMU	Frequency Modulation Unit
FMR	Frequency Modulation Decoder/RF
FW	Firmware
GI	Guard Interval
GPIO	General Purpose Input Output
GPL	GNU General Public License
GPU	General Purpose Input Output Unit
HIU	Host Interface Unit
HT	High Throughput
HW	Hardware
I/Q	Inphase/Quadrature
IB	InBand
IBSS	Independent Basic Service Set
ICE	In-Circuit Emulator (or Emulation)
ICR	Interrupt Cause Register
ICU	Interrupt Controller Unit
ICV	Integrity Check Value
IE	Information Element
IEEE	Institute of Electrical and Electronics Engineers
IEMR	Interrupt Event Mask Register
IF	Interface
IFS	Interframe Space

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
IMR	Interrupt Mask Register
IPG	Inter Packet Gap
IR	Infrared
IRQ	Interrupt Request
ISA	Instruction Set Architecture
ISDN	Integrated Services Digital Network
ISM	Industrial Scientific and Medical
ISMR	Interrupt Status Mask Register
ISR	Interrupt Status Register
JEDEC	Joint Electronic Device Engineering Council
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LME	Layer Management Entity
LQFN	Low Quad Flat Non-leaded
LSB	Least Significant Bit
LSP	Low Speed Peripheral
MAC	Medium Access Controller
MC	Memory Controller
MCU	WLAN MAC Control Unit
MDI	Modem Data Interface
MIB	Management Information Base
MIC	Message Integrity Code
MII	Media Independent Interface
MIMO	Multiple Input Multiple Output
MIPS	Million Instructions Per Second
MLME	MAC Sublayer Management Entity
MMI	Modem Management Interface
MMPDU	MAC Management Protocol Data Unit
MMU	Memory Management Unit
MPDU	MAC Protocol Data Unit
MSB	Most Significant Bit

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
MSDU	MAC Service Data Unit
Multi-ICE	JTAG emulator for ARM-based SoC devices
NAV	Network Allocation Vector
NL	No load
NPTR	Next Descriptor Pointer
OFDM	Orthogonal Frequency Division Multiplexing
OID	Object Identifier
OOB	OutofBand
PA	Power Amplifier
PAD	Packet Assembler/Disassembler
PBU	Peripheral Bus Unit
PC	Point Coordinator
PCB	Printed Circuit Board
PCF	Point Coordination Function
PCIe	PCI Express
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PEAP	Protected EAP
PHY	Physical Layer
PIFS	Priority Interframe Space
PLL	Phase-Locked Loop
PLME	Physical Layer Management Entity
PMU	Power Management Unit
POST	Power On Self Test
PPK	Per-Packet Key
PPM	Pulse Position Modulation
PSK	Pre-Shared Keys
PTA	Packet Traffic Arbitration
PWK	Pair Wise Key
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat Non Leaded Package

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
QoS	Quality of Service
RA	Receiver Address
RBDS	Radio Broadcast Data System
RDS	Radio Data System
RF	Radio Frequency
RIFS	Reduced Interframe Space
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RSSI	Receiver Signal Strength Indicator
RTS	Request To Send
RTU	General Purpose Timer Unit
SA	Source Address
SAP	Service Access Point
SCLK	Serial Interface Clock
SDA	Serial Interface Data
SFD	Start of Frame Delimiter
SIFS	Short Interframe Space
SIU	Serial Interface Unit (UART)
SJU	System/Software JTAG Controller Unit
SM	Switch Module
SMI	Serial Management Interface
SNR	Signal To Noise Ratio
SO	Serial Out
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SQU	Internal SRAM Unit
SRWB	Serial Interface Read Write
SSID	Service Set Identifier
TA	Transmitter Address
TBG	Time Base Generator
TBTT	Target Beacon Transmission Time

Table 91: Acronyms and Abbreviations (Continued)

Acronym	Definition
TCM	Tightly Coupled Memory
TCP/IP	Transmission Control Protocol/Internet Protocol
TDM	Time Division Multiplexing
TDU	Time Division Multiplexing Unit
TIM	Traffic Indication Map
TKIP	Temporal Key Integrity Protocol
TQFP	Thin Quad Flat Pack
TRPC	Transmit Rate-based Power Control
TSC	TKIP Sequence Counter
TSF	Timing Synchronization Function
UART	Universal Asynchronous Receiver/Transmitter
UBM	Under Bump Metal
VCO	Voltage Controlled Oscillator
WAP	Wireless Application Protocol
WEP	Wired Equivalent Privacy
Wi-Fi	Wireless Fidelity (IEEE 802.11)
WLAN	Wireless Local Area Network
WMM	Wi-Fi Multimedia
WPA	Wi-Fi Protected Access
WPA2	Wi-Fi Protected Access 2
WPA2-PSK	Wi-Fi Protected Access 2-Pre-shared Keys
WPA-PSK	Wi-Fi Protect Access-Pre-shared Keys
WSE	Wireless Interconnection System Engine
XFQFN	Extra-Fine Quad Flat Non-leaded
XOSC	Crystal Oscillator

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Appendix C. Revision History

Table 92: Revision History

Document Type	Document Revision
Release	Rev. D

Package
- Updated coexistence signal descriptions
- Figure 4, “QFN Mechanical Drawing—68-Pin,” on page 19: updated drawing: added option1 note
- Table 2, “Flip Chip Locations—500 µm Pitch,” on page 26: removed BT_FREQ pin locations from VSS section

Processor
- DMA—updated description

Peripheral Bus
- Section 5.5.2 "Booting from UART" on page 109: updated description

Electricals
- Table 53, “DC Electricals—1.8V/3.3V (VIO_X1/VIO_X2),” on page 115: reorganized; rounded pullup/pulldown values/updated weak pull-up/pull-down values to 10µA maximum
- Table 59, “Configuration Pin Serial Interface,” on page 120: removed Rpup_Normal; added note
- Table 61, “AC Coupled Mode,” on page 121: updated minimum value from 0.2V to 0.4V
- Table 70, “Crystal Specifications,” on page 124: changed Frequency Tolerance Condition to “Over operating temperature”

Part Ordering
- Added note for 2.4 GHz operation (5 GHz not supported in production).

Appendix
- Appendix Appendix A. "Flip Chip Underfill Requirement" on page 145: added

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