

16-bit Proprietary Microcontroller

CMOS

F²MC-16LX MB90378 Series

MB90F378/V378

■ DESCRIPTION

The MB90378 series is a line of general-purpose, 16-bit microcontrollers designed for those applications which require high-speed real-time processing. The instruction set is designed to be optimized for controller applications which inheriting the AT architecture of F²MC-16LX family and allow a wide range of control tasks to be processed efficiently at high speed.

A built-in LPC interface, serial IRQ and PS/2 interface simplifies communication with host CPU and PS/2 devices in computer system. Moreover, SMBus compliant I²C*² and A/D converter implements the smart battery control. With these features, the MB90378 series matches itself as keyboard controller with smart battery control.

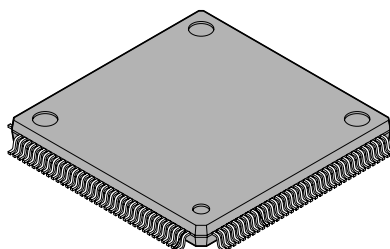
While inheriting the AT architecture of the F²MC*¹ family, the instruction set for the F²MC-16LX CPU core of the MB90378 series incorporates additional instructions for high-level languages, supports extended addressing modes, and contains enhanced multiplication and division instructions as well as a substantial collection of improved bit manipulation instructions. In addition, the MB90378 series has an on-chip 32-bit accumulator which enables processing of long-word data.

*1 : F²MC stands for FUJITSU Flexible Microcontroller, a registered trademark of FUJITSU LIMITED.

*2 : Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use, these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

■ PACKAGE

144-pin plastic LQFP



(FPT-144P-M12)

MB90378 Series

■ FEATURES

• Clock

- Embedded PLL clock multiplication circuit
- Operating clock (PLL clock) can be selected from divided-by-2 of oscillation or one to four times the oscillation (at oscillation of 4 MHz to 20 MHz)
- Minimum instruction execution time of 50 ns (at oscillation of 5 MHz, four times the PLL clock, operation at V_{CC} of 3.3 V)

• CPU addressing space of 16 Mbytes

Internal 24-bit addressing

• Instruction set optimized for controller applications

- Rich data types (bit, byte, word, long word)
- Rich addressing mode (23 types)
- High code efficiency
- Enhanced precision calculation realized by the 32-bit accumulator

• Instruction set designed for high level language (C) and multi-task operations

- Adoption of system stack pointer
- Enhanced pointer indirect instructions
- Barrel shift instructions

• Program patch function (2 address pointer)

• Improved execution speed

4-byte instruction queue

• Powerful interrupt function

- Priority level programmable : 8 levels
- 32 factors of stronger interrupt function

• Automatic data transmission function independent of CPU operation

- Extended intelligent I/O service function (EI²OS)
- Maximum 16 channels

• Low-power consumption (standby) mode

- Sleep mode (mode in which CPU operating clock is stopped)
- Timebase timer mode (mode in which operations other than timebase timer and watch timer are stopped)
- Stop mode (mode in which all oscillations are stopped)
- CPU intermittent operation mode
- Watch mode

• Dual operation flash

Upper and lower banks of flash memory can be used to execute erase/program and read operation concurrently (MB90F378)

• Package

LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)

• Process

CMOS technology

■ PRODUCT LINEUP

Parameter \ Part number	MB90F378	MB90V378
Classification	Flash type ROM	—
ROM size	128 Kbytes (112 Kbytes + 16 Kbytes) Dual operation	—
RAM size	6 Kbytes	15.6 Kbytes
CPU function	Number of instruction : 351 Minimum execution time : 50 ns/5 MHz (PLL x 4) Addressing mode : 23 Data bit length : 1, 8, 16 bits Maximum memory space : 16 Mbytes	
I/O port	I/O port (Nch) : 25 I/O port (CMOS) : 68 I/O port (CMOS with pull-up control) : 32 Total : 125	
16-bit reload timer	Reload timer : 6 channels Reload mode, single-shot mode or event count mode selectable	
8/16-bit PPG timer	PPG timer : 2 channels (8-bit mode, 4 channels)	
16-bit PPG timer	PPG timer : 3 channels PWM mode or single-shot mode selectable	
Bit decoder	Bit decoder : 1 channel	
Parity generator	Parity generator : 1 channel Selectable odd/even parity	
PS/2 interface	PS/2 interface : 3 channels 4 selectable sampling clocks	
LPC interface	LPC bus interface : 1 channel Universal peripheral Interface : 4 channels GA20 output control : for UPI ch 0 only Data buffer array : 80 bytes	
Serial IRQ controller	Serial IRQ request : 6 channels LPC clock monitor/control	
UART	With full-duplex double buffer (variable data length) Clock asynchronous or clock synchronized transmission (with start and stop bits) can be selectively used	
I ² C	I ² C (SMbus compliant) : 1 channel Support I ² C bus of PHILIPS and the SMbus proposed by Intel I ² C bus Selectable packet error check Timeout detection function	
Multi-address I ² C	Multi-address I ² C (SMbus compliant) : 1 channel Support I ² C bus of PHILIPS and the SMbus proposed by Intel I ² C bus Selectable packet error check Timeout detection function 6 addresses support ALERT function	

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MB90378 Series

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Parameter	Part number	MB90F378	MB90V378
Bridge circuit		Three bus connection routes can be switched by I ² C/multi-address I ² C	
DTP/external interrupt		8 independent channels Selectable causes : Rise/fall edge, fall edge, "L" level or "H" level	
Extended external interrupt		8 multiplex channels × 2 set Selectable causes : Rise/fall edge, fall edge, rise edge or "L" level	
Key-on wake-up interrupt		8 independent channels Causes : "L" level	
8/10-bit A/D converter		8/10-bit resolution : 12 channels Conversion time : Less than 4.2 μs (20 MHz internal clock)	
8-bit D/A converter		8-bit resolution : 2 channels	
LCD controller/driver		Up to 9 SEG × 4 COM Selectable LCD output or CMOS I/O port	
Low-power consumption		Stop mode/Sleep mode/CPU intermittent operation mode/Watch mode	
Process		CMOS	
Package		LQFP-144 (FPT-144P-M12 : 0.4 mm pitch)	PGA299
Operating voltage		2.7 V to 3.6 V at 20 MHz*	

* : Varies with conditions such as the operating frequency (see "■ ELECTRICAL CHARACTERISTICS"). Assurance for the MB90V378 is given only for operation with a tool at power supply voltage of 2.7 V to 3.6 V, an operating temperature of 0 °C to +25 °C, and an operating frequency of 1 MHz to 20 MHz.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB90F378	MB90V378
FPT-144P-M12	○	X
PGA299	X	○

○ : Available
X : Not available

Note : For more information about each package, see "■ PACKAGE DIMENSIONS".

■ DIFFERENCES AMONG PRODUCTS

Memory size

In evaluation with an evaluation product, note the difference between the evaluation product and the product actually used. The following items must be taken into consideration.

- The MB90V378 does not have an internal ROM, however, operations equivalent to chips with an internal ROM can be evaluated by using a dedicated development tool, enabling selection of ROM size by settings of the development tool.
- In the MB90V378, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FF0000_H to FF3FFF_H are mapped to bank FF only. (This setting can be changed by the development tool configuration.)
- In the MB90F378, images from FF4000_H to FFFFFFF_H are mapped to bank 00, and FF0000_H to FF3FFF_H are mapped to bank FF only.

MB90378 Series

■ PIN DESCRIPTION

Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
128,129	X0,X1	A	Oscillating	Main oscillation I/O pins.
20,21	X0A,X1A	A	Oscillating	Sub-clock oscillation I/O pins.
17	$\overline{\text{RST}}$	B	Reset input	External reset input pin.
58, 57, 56	MD0 to MD2	C	Mode input	Input pin for operation mode specification. Connect this pin directly to Vcc or Vss.
109 to 116	P00 to P07	D	Port input	General-purpose I/O ports.
	KSI0 to KSI7			Can be used as key-on wake-up interrupt input ch 0 to 7. Input is enabled when 1 is set in EICR : EN0 to 7 in standby mode.
117 to 124	P10 to P17	E		General-purpose I/O ports.
125, 130 to 136	P20 to P27	E		General-purpose I/O ports.
137, 138	P30, P31	E		General-purpose I/O ports.
	PG00, PG01			8/16-bit PPG timer output pins. 8-bit x 2 channels mode use : Event output from PG00/PG01 16-bit x 1 channel mode use : Event output from PG00
139, 140	P32, P33	E		General-purpose I/O ports.
	PG10, PG11			8/16-bit PPG timer output pins. 8-bit x 2 channels mode use : Event output from PG10/PG11. 16-bit x 1 channel mode use : Event output from PG10.
141 to 143	P34 to P36	E		General-purpose I/O ports.
144	P37	E		General-purpose I/O port.
	ADTG			External trigger input pin (ADTG) for the A/D converter.
1	P40	F		General-purpose Nch open-drain I/O port.
	PSCK0			Serial clock I/O pin for PS/2 interface ch 0. This function is selected when PS/2 interface ch 0 is enabled.
2	P41	F		General-purpose Nch open-drain I/O port.
	PSDA0			Serial data I/O pin for PS/2 interface ch 0. This function is selected when PS/2 interface ch 0 is enabled.
3	P42	F		General-purpose Nch open-drain I/O port.
	PSCK1		Serial clock I/O pin for PS/2 interface ch 1. This function is selected when PS/2 interface ch 1 is enabled.	
4	P43	F	General-purpose Nch open-drain I/O port.	
	PSDA1		Serial data I/O pin for PS/2 interface ch 1. This function is selected when PS/2 interface ch 1 is enabled.	

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MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
5	P44	F	Port input	General-purpose Nch open-drain I/O port.
	PSCK2			Serial clock I/O pin for PS/2 interface ch 2. This function is selected when PS/2 interface ch 2 is enabled.
6	P45	F		General-purpose Nch open-drain I/O port.
	PSDA2			Serial data I/O pin for PS/2 interface ch 2. This function is selected when PS/2 interface ch 2 is enabled.
7	P46	G		General-purpose Nch open-drain I/O port.
	$\overline{\text{CLKRUN}}$			LPC clock status / restart request I/O pin for serial IRQ controller. This function is selected when serial IRQ and LPC clock restart request is enabled.
8	P47	H		General-purpose I/O port.
	SERIRQ			Serial IRQ data I/O pin for serial IRQ controller. This function is selected when serial IRQ is enabled.
9	P50	J		General-purpose Nch open-drain I/O port.
	GA20			GA20 output for LPC interface. This function is selected when GA20 function is enabled.
10	P51	H		General-purpose I/O port.
	$\overline{\text{LFRAME}}$			LFRAME input for LPC interface. This function is selected when LPC interface is enabled.
11	P52	H		General-purpose I/O port.
	$\overline{\text{LRESET}}$			Reset input for LPC interface. This function is selected when LPC interface is enabled.
12	P53	H		General-purpose I/O port.
	LCK			Clock input for LPC interface. This function is selected when LPC interface is enabled.
13 to 16	P54 to P57	H	General-purpose I/O ports.	
	LAD0 to LAD3		Address/Data I/O for LPC interface. This function is selected when LPC interface is enabled.	
93 to 98	P60 to P65	I	General-purpose I/O ports.	
	INT0 to INT5		Can be used as DTP/external interrupt request input ch 0 to 5. Input is enabled when 1 is set in ENIR: EN0 to 5 in standby mode.	
99	P66	I	General-purpose I/O port.	
	UCK1		Serial clock I/O pin for UART ch 1. This function is enabled when UART ch 1 enables clock output.	

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MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
100	P67	I	Port input	General-purpose I/O port.
	UO1			Serial data output pin for UART ch 1. This function is enabled when UART ch 1 enables data output.
101	P70	I		General-purpose I/O port.
	UI1			Serial data input pin for UART ch 1. While UART ch 1 is operating for input, the input of this pin is used as required and must not be used for any other input.
102	P71	I		General-purpose I/O port.
	UCK2			Serial clock I/O pin for UART ch 2. This function is enabled when UART ch 2 enables clock output.
103	P72	I		General-purpose I/O port.
	UO2			Serial data output pin for UART ch 2. This function is enabled when UART ch 2 enables data output.
104	P73	I		General-purpose I/O port.
	UI2			Serial data input pin for UART ch 2. While UART ch 2 is operating for input, the input of this pin is used as required and must not be used for any other input.
105	P74	I		General-purpose I/O port.
	UCK3			Serial clock I/O pin for UART ch 3. This function is enabled when UART ch 3 enables clock output.
106	P75	I		General-purpose I/O port.
	UO3			Serial data output pin for UART ch 3. This function is enabled when UART ch 3 enables data output.
107	P76	I		General-purpose I/O port.
	UI3			Serial data input pin for UART ch 3. While UART ch 3 is operating for input, the input of this pin is used as required and must not be used for any other input.
108	P77	I	General-purpose I/O port.	
	PPG1		Output pin for PPG ch 1. This function is enabled when PPG ch 1 output is enabled.	
71	P80	T	General-purpose Nch open-drain I/O port.	
	SCL1		Serial clock I/O pin for multi-address I ² C.	
72	P81	T	General-purpose Nch open-drain I/O port.	
	SDA1		Serial data I/O pin for multi-address I ² C.	

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Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
73	P82	J	Port input	General-purpose Nch open-drain I/O port.
	ALERT			ALERT output pin for multi-address I ² C.
30, 31	P83, P84	I		General-purpose I/O ports.
	INT6, INT7			Can be used as DTP/external interrupt request input ch6, 7. Input is enabled when 1 is set in ENIR: EN6, 7 in standby mode.
32	P85	I		General-purpose I/O port.
33	P86	I		General-purpose I/O port.
65	P90	T		General-purpose Nch open-drain I/O port.
	SCL2			Serial clock I/O pin for bridge circuit.
66	P91	T		General-purpose Nch open-drain I/O port.
	SDA2			Serial data I/O pin for bridge circuit.
67	P92	T		General-purpose Nch open-drain I/O port.
	SCL3			Serial clock I/O pin for bridge circuit.
68	P93	T		General-purpose Nch open-drain I/O port.
	SDA3			Serial data I/O pin for bridge circuit.
69	P94	T		General-purpose Nch open-drain I/O port.
	SCL4			Serial clock I/O pin for bridge circuit.
70	P95	T		General-purpose Nch open-drain I/O port.
	SDA4			Serial data I/O pin for bridge circuit.
22 to 29	PA0 to PA7	I		General-purpose I/O ports.
	EEI0 to EEI7			External IRQ input pin for Extend External Interrupt request ch0 to 7. When IRQ detect, prepare to the CPU Interrupt. (Multiplex)
34 to 41	PB0 to PB7	I	General-purpose I/O ports.	
	EEI8 to EEI15		External IRQ input pin for Extend External Interrupt request ch8 to 15. When IRQ detect, prepare to the CPU Interrupt. (Multiplex)	
45 to 52	PC0 to PC7	M	A/D input	General-purpose I/O ports.
	AN0 to AN7			A/D converter analog input pin 0 to 7. This function is enabled when the analog input specification is enabled (ADER1).
53, 59 to 61	PD0 to PD3	M		General-purpose I/O ports.
	AN8 to AN11			A/D converter analog input pin 8 to 11. This function is enabled when the analog input specification is enabled (ADER2).

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MB90378 Series

Pin no.	Pin name	I/O circuit	Pin status during reset	Function
LQFP-144				
62, 63	PD4, PD5	N	Port input	General-purpose I/O ports.
	DA1, DA2			D/A converter analog output 1, 2. This function is selected when D/A converted is enabled.
64, 92	PD6, PD7	H		General-purpose I/O ports.
	PPG2, PPG3			Output pin for PPG ch 2, 3. This function is selected when PPG ch 2, 3 output is enabled.
74	PE0	O		General-purpose I/O port.
	SEG0			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN1			External clock input pin for reload timer 1.
75	PE1	O		General-purpose I/O port.
	SEG1			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO1			Event output pin for reload timer 1.
76	PE2	O		General-purpose I/O port.
	SEG2			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN2			External clock input pin for reload timer 2.
77	PE3	O		General-purpose I/O port.
	SEG3			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO2			Event output pin for reload timer 2.
78	PE4	O	General-purpose I/O port.	
	SEG4		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN3		External clock input pin for reload timer 3.	
79	PE5	O	General-purpose I/O port.	
	SEG5		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TO3		Event output pin for reload timer 3.	
80	PE6	O	General-purpose I/O port.	
	SEG6		Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.	
	TIN4		External clock input pin for reload timer 4.	

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Pin no. LQFP-144	Pin name	I/O circuit	Pin status during reset	Function
81	PE7	O	Port input	General-purpose I/O port.
	SEG7			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TO4			Event output pin for reload timer 4.
82	PF0	P		General-purpose Nch Open-drain I/O port.
	SEG8			Segment output pin for LCD controller/driver. This function is selected when LCD segment output is enabled.
	TIN5			External clock input pin for reload timer 5.
83	PF1	P		General-purpose Nch Open-drain I/O port.
	COM0			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
	TO5			Event output pin for reload timer 5.
84	PF2	P		General-purpose Nch Open-drain I/O port.
	COM1			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
	TIN6			External clock input pin for reload timer 6.
85	PF3	P		General-purpose Nch Open-drain I/O port.
	COM2			COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.
	TO6			Event output pin for reload timer 6.
86	PF4	P	General-purpose Nch Open-drain I/O port.	
	COM3		COM output pin for LCD controller/driver. This function is selected when LCD COM output is enabled.	
87 to 89	PF5 to PF7	Q	Power input	General-purpose Nch Open-drain I/O ports.
	V1 to V3			Power input pin for LCD controller/driver. This function is selected when external voltage divider is enabled.
42	AV _{cc}	R	Power input	V _{cc} power input pin for analog circuits.
43	AV _R	S		V _{ref+} input pin for the A/D converter. This voltage must not exceed V _{cc} . V _{ref-} is fixed to AV _{ss} .
44	AV _{ss}	R		V _{ss} power input pin for analog circuits.
19,55,91,127	V _{ss}	–	Source Power input	Power (0 V) input pin.
18,54,90,126	V _{cc}	–		Power (3.3 V) input pin.

MB90378 Series

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<p>Main/Sub clock (main/sub clock crystal oscillator)</p> <ul style="list-style-type: none"> At an oscillation feedback resistor of approximately 1 MΩ
B		<ul style="list-style-type: none"> CMOS hysteresis input Pull-up resistor approximately 50 kΩ
C		<ul style="list-style-type: none"> CMOS hysteresis input
D		<ul style="list-style-type: none"> CMOS output CMOS hysteresis input Selectable pull-up resistor approximately 50 kΩ I_{OL} = 4 mA
E		<ul style="list-style-type: none"> CMOS output CMOS input Selectable pull-up resistor approximately 50 kΩ I_{OL} = 4 mA
F		<ul style="list-style-type: none"> Nch open-drain output CMOS hysteresis input I_{OL} = 4 mA 5 V tolerant

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Type	Circuit	Remarks
G		<ul style="list-style-type: none"> • Nch open-drain output • CMOS input • $I_{OL} = 4 \text{ mA}$
H		<ul style="list-style-type: none"> • CMOS output • CMOS input • $I_{OL} = 4 \text{ mA}$
I		<ul style="list-style-type: none"> • CMOS output • CMOS hysteresis input • $I_{OL} = 4 \text{ mA}$
J		<ul style="list-style-type: none"> • Nch open-drain output • CMOS input • $I_{OL} = 4 \text{ mA}$ • 5 V tolerant
M		<ul style="list-style-type: none"> • CMOS output • CMOS input • A/D analog input • $I_{OL} = 4 \text{ mA}$

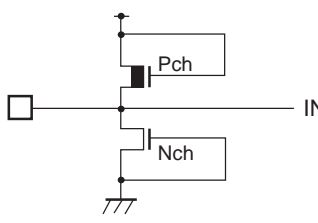
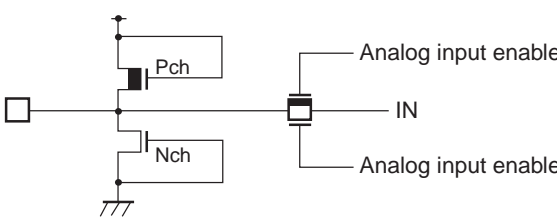
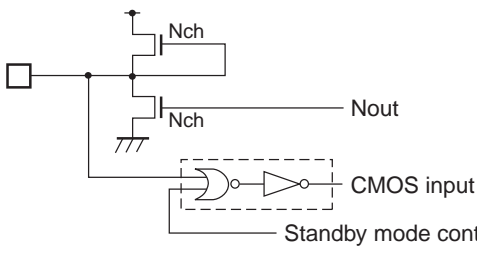
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MB90378 Series

Type	Circuit	Remarks
N		<ul style="list-style-type: none"> • CMOS output • CMOS input • D/A analog output • $I_{OL} = 4 \text{ mA}$
O		<ul style="list-style-type: none"> • CMOS output • CMOS hysteresis input • Segment output • $I_{OL} = 4 \text{ mA}$
P		<ul style="list-style-type: none"> • Nch open-drain output • CMOS hysteresis input • Segment output • $I_{OL} = 12 \text{ mA}$
Q		<ul style="list-style-type: none"> • Nch open-drain output • CMOS hysteresis input • LCD driving power supply • $I_{OL} = 12 \text{ mA}$

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Type	Circuit	Remarks
R		<ul style="list-style-type: none"> • Power supply input protection circuit
S		<ul style="list-style-type: none"> • A/D converter reference voltage (AVR) input pin with protection circuit
T		<ul style="list-style-type: none"> • Nch open-drain output • CMOS input • $I_{OL} = 4 \text{ mA}$ • 5 V tolerant

MB90378 Series

■ HANDLING DEVICES

1. Be sure that the maximum rated voltage is not exceeded (latch-up prevention).

A latch-up may occur on a CMOS IC if a voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin other than medium-to-high voltage pins. A latch-up may also occur if a voltage higher than the rating is applied between V_{CC} pin and V_{SS} pin. A latch-up causes a rapid increase in the power supply current, which can result in thermal damage to an element. Take utmost care that the maximum rated voltage is not exceeded.

When turning the power on or off to analog circuits, be sure that the analog supply voltages (AV_{CC} , AVR) and analog input voltage do not exceed the digital supply voltage (V_{CC}).

2. Stabilize the supply voltages

Even within the operation guarantee range of the V_{CC} supply voltage, a malfunction can be caused if the supply voltage undergoes a rapid change. For voltage stabilization guidelines, the V_{CC} ripple fluctuations (P-P value) at commercial frequencies (50 Hz to 60 Hz) should be suppressed to "10%" or less of the reference V_{CC} value. During a momentary change such as when switching a supply voltage, voltage fluctuations should also be suppressed so that the "transient fluctuation rate" is 0.1 V/ms or less.

3. Power-on

To prevent a malfunction in the built-in voltage drop circuit, secure "50 μ s (between 0.2 V and 1.8 V)" or more for the voltage rise time during power-on.

4. Treatment of unused input pins

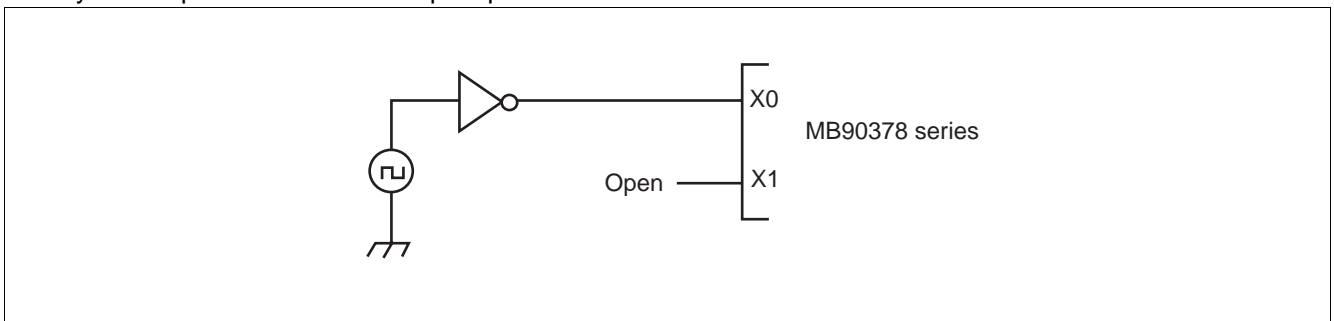
An unused input pin may cause a malfunction if it is left open. Every unused input pin should be pulled up or down.

5. Treatment of A/D converter, and D/A converter power pin

When the A/D converter, D/A converter and comparator is not used, connect the pins as follows: $AV_{CC} = V_{CC}$, $AV_{SS} = AVR = V_{SS}$.

6. Notes on external clock

When an external clock is used, the oscillation stabilization wait time is required at power-on reset or at cancellation of sub-clock mode or stop mode. As shown in diagram below, when an external clock is used, connect only the X0 pin and leave the X1 pin open.



7. Power supply pins

When a device has two or more V_{CC} or V_{SS} pins, the pins that should have equal potential are connected within the device in order to prevent a latch-up or other malfunction. To reduce extraneous emission, to prevent a malfunction of the strobe signal due to an increase in the group level, and to maintain the local output current rating, connect all these power supply pins to an external power supply and ground them.

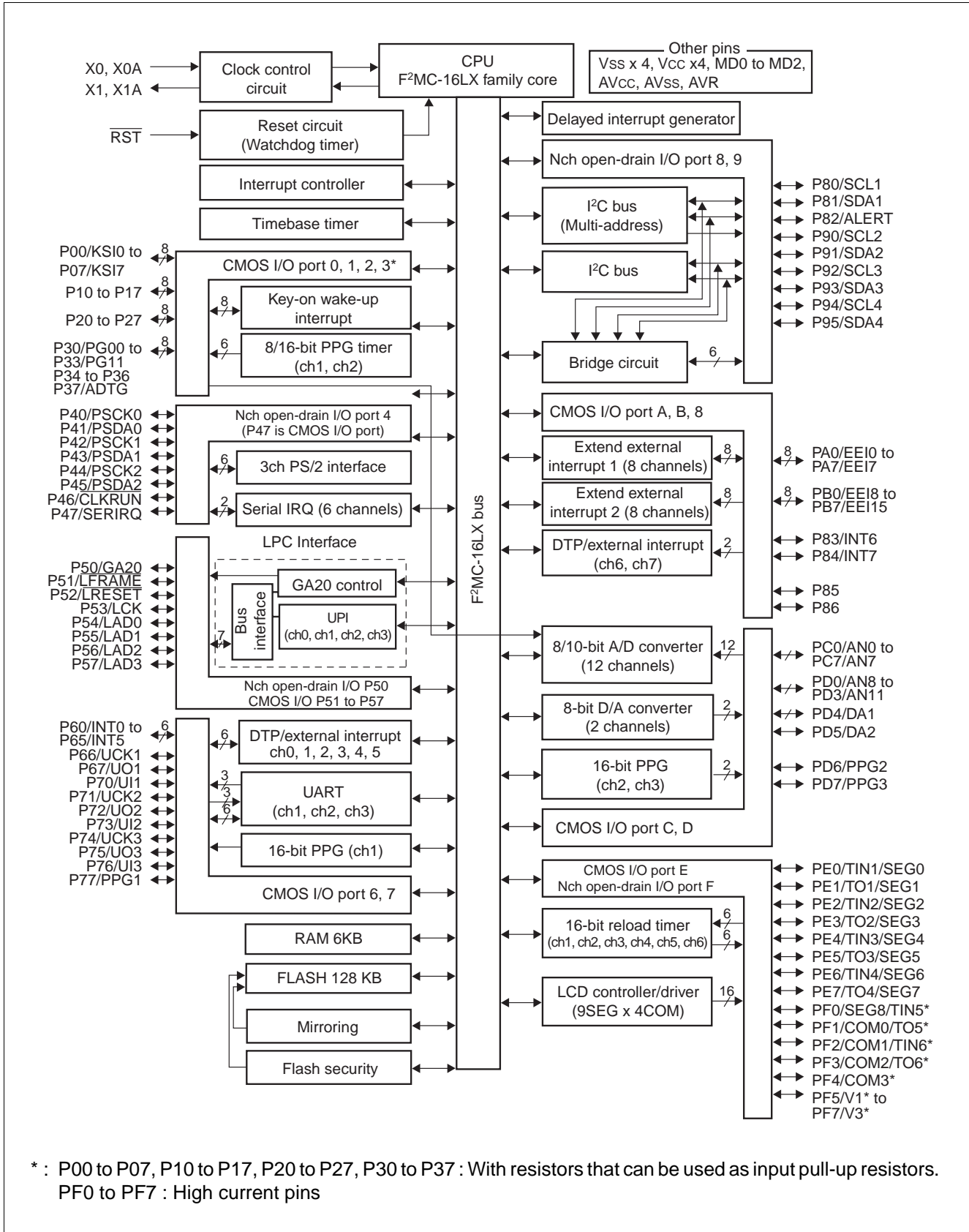
The current source should be connected to the V_{CC} and V_{SS} pins of the device with minimum impedance. It is recommended that a bypass capacitor of about 0.1 μF be connected near the terminals between V_{CC} and V_{SS} .

8. Analog power-on sequence of A/D converter and D/A converter

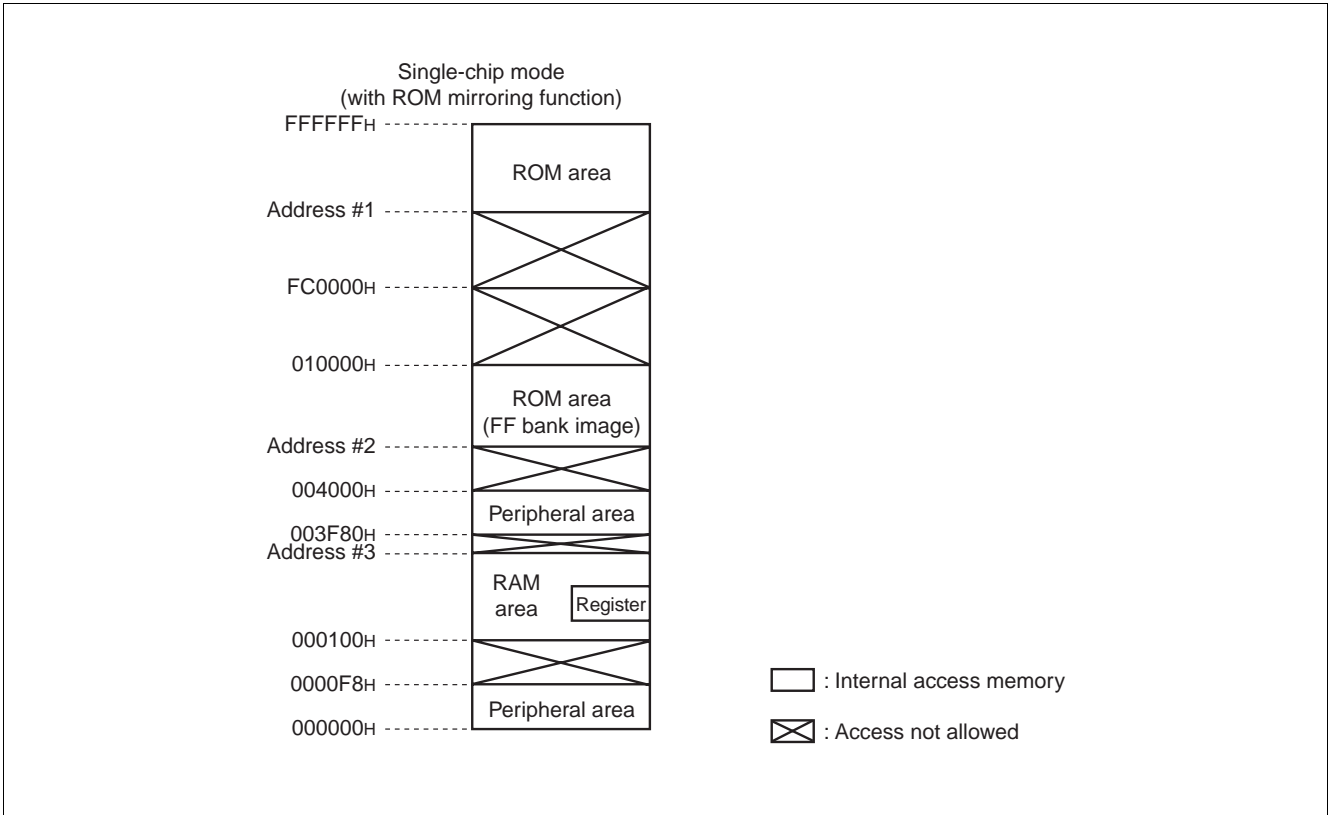
The power to the A/D converter and D/A converter (AV_{CC} , AVR) and analog inputs (AN0 to AN11) must be turned on after the power to the digital circuits (V_{CC}) is turned on. When turning off the power, turn off the power to the digital circuits (V_{CC}) after turning off the power to the A/D converter, D/A converter and analog inputs. When the power is turned on or off, AVR should not exceed AV_{CC} . Also, when a pin that is used for A/D analog input is also used as an input port, the input voltage should not exceed AV_{CC} . (The power to the analog circuits and the power to the digital circuits can be simultaneously turned on or off.)

MB90378 Series

■ BLOCK DIAGRAM



MEMORY MAP



Model	Address #1	Address #2	Address #3
MB90F378	FE0000 _H	004000 _H	001900 _H
MB90V378	FE0000 _H *	004000 _H *	003F80 _H

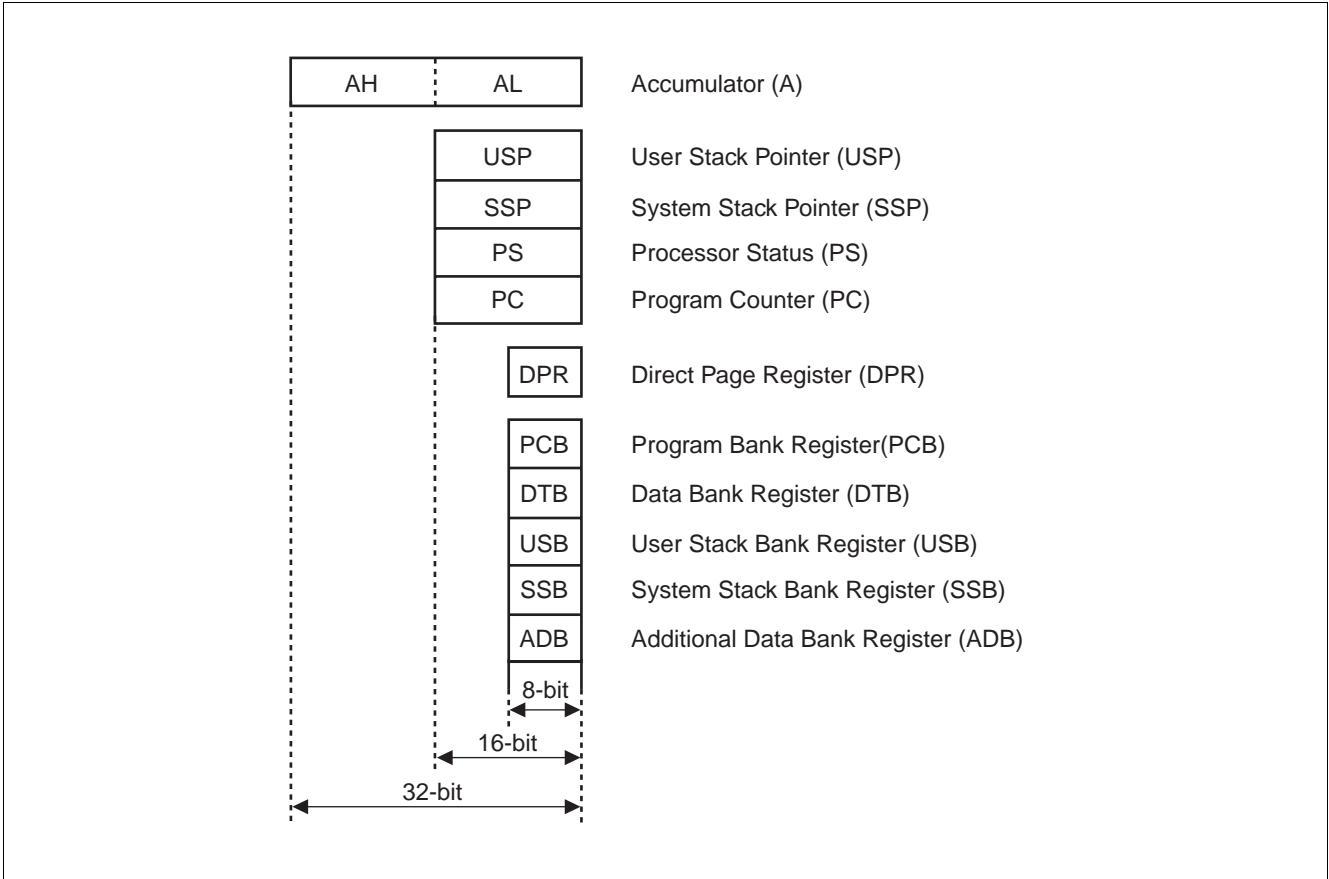
* : The MB90V378 does not contain ROM. Assume that the development tool uses these area for its ROM decode areas.

- Notes :
- If single-chip mode (without ROM mirroring function) is selected, see Chapter 32, "ROM Mirroring Function Selection Module" of the MB90378 series H/W manual.
 - ROM data in the FF bank can be seen as an image in the higher 00 bank to validate the small model C compiler. Because addresses of the 16 low-order bits in the FF bank are the same, the table in ROM can be referenced without the "far" specification. For example, when 00C000_H is accessed, the contents of ROM at FFC000_H are actually accessed. The ROM area in the FF bank exceeds 48 Kbytes, and all areas cannot be seen as images in the 00 bank. Because ROM data from FF4000_H to FFFFFFF_H is seen as an image at 004000_H to 00FFFF_H, the ROM data table should be stored in the area from FF4000_H to FFFFFFF_H.

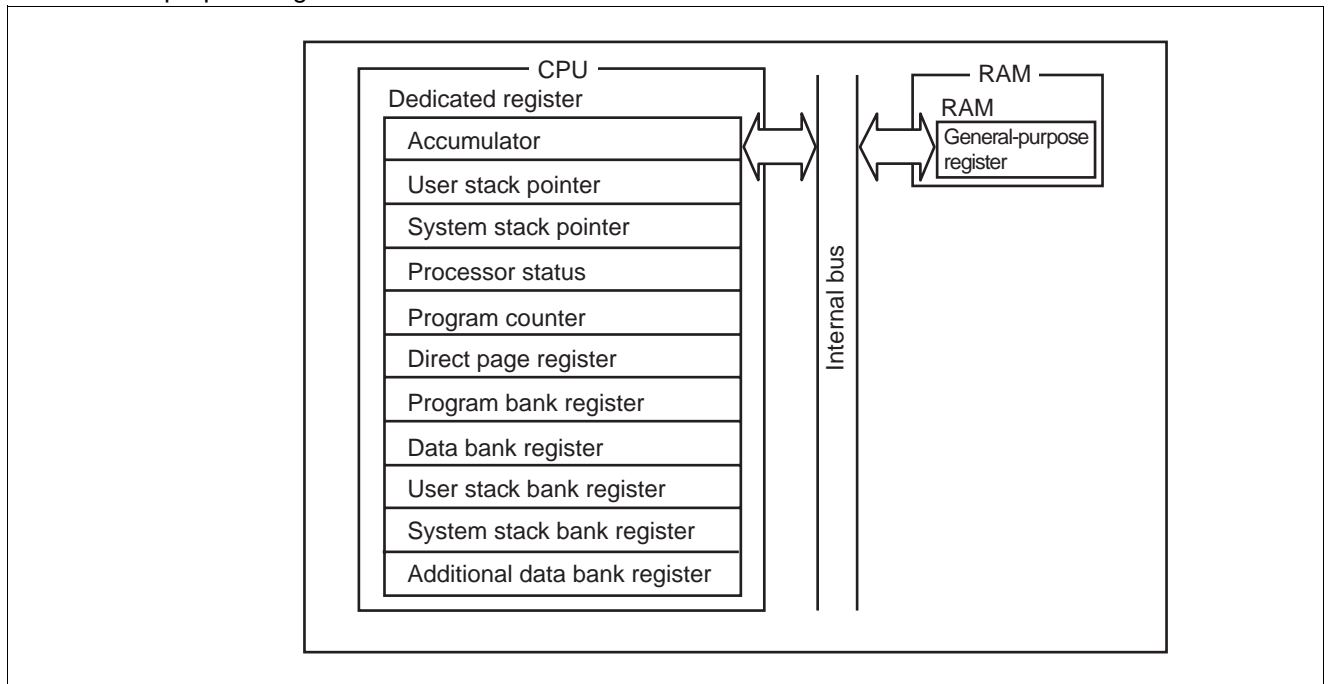
MB90378 Series

■ F²MC-16LX CPU PROGRAMMING MODEL

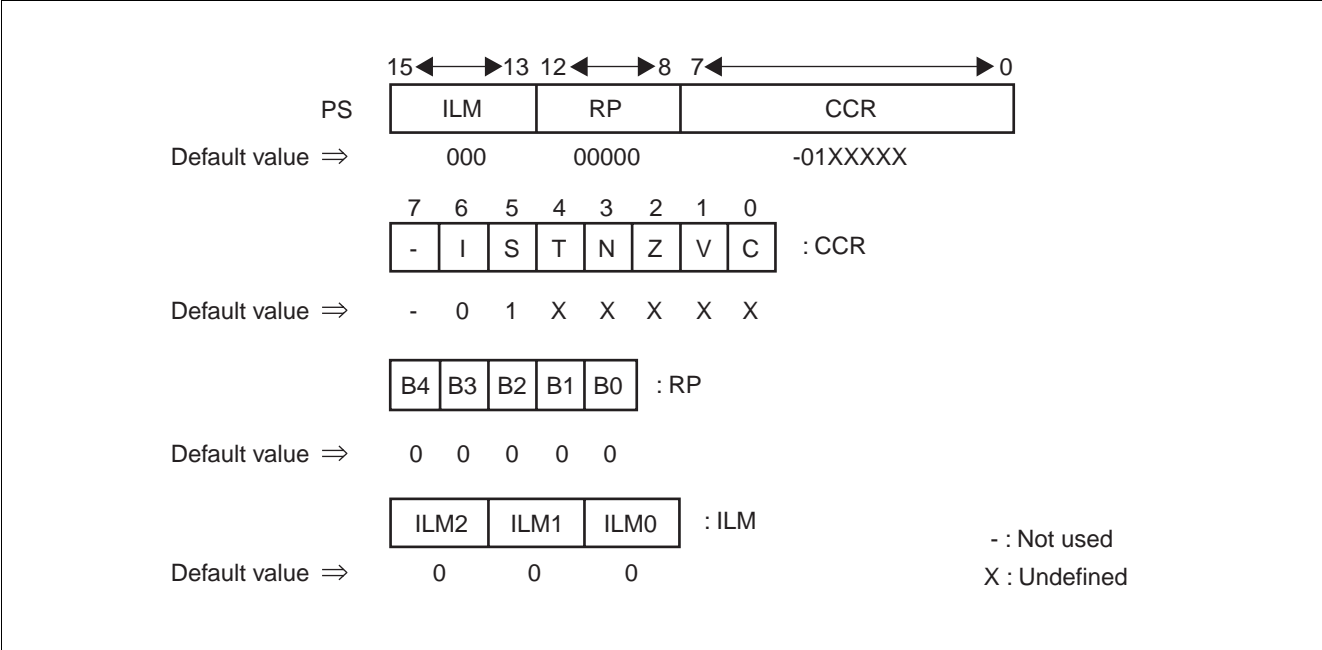
- Dedicated registers



- General-purpose registers



• Processor status (PS)



MB90378 Series

■ I/O MAP

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000000 _H	PDR0	Port 0 data register	R/W	R/W	Port 0	XXXXXXXX _B
000001 _H	PDR1	Port 1 data register	R/W	R/W	Port 1	XXXXXXXX _B
000002 _H	PDR2	Port 2 data register	R/W	R/W	Port 2	XXXXXXXX _B
000003 _H	PDR3	Port 3 data register	R/W	R/W	Port 3	XXXXXXXX _B
000004 _H	PDR4	Port 4 data register	R/W	R/W	Port 4	X1111111 _B
000005 _H	PDR5	Port 5 data register	R/W	R/W	Port 5	XXXXXXXX1 _B
000006 _H	PDR6	Port 6 data register	R/W	R/W	Port 6	XXXXXXXX _B
000007 _H	PDR7	Port 7 data register	R/W	R/W	Port 7	XXXXXXXX _B
000008 _H	PDR8	Port 8 data register	R/W	R/W	Port 8	-XXXX111 _B
000009 _H	PDR9	Port 9 data register	R/W	R/W	Port 9	--111111 _B
00000A _H	PDRA	Port A data register	R/W	R/W	Port A	XXXXXXXX _B
00000B _H	PDRB	Port B data register	R/W	R/W	Port B	XXXXXXXX _B
00000C _H	PDRC	Port C data register	R/W	R/W	Port C	XXXXXXXX _B
00000D _H	PDRD	Port D data register	R/W	R/W	Port D	XXXXXXXX _B
00000E _H	PDRE	Port E data register	R/W	R/W	Port E	XXXXXXXX _B
00000F _H	PDRF	Port F data register	R/W	R/W	Port F	11111111 _B
000010 _H	DDR0	Port 0 direction register	R/W	R/W	Port 0	00000000 _B
000011 _H	DDR1	Port 1 direction register	R/W	R/W	Port 1	00000000 _B
000012 _H	DDR2	Port 2 direction register	R/W	R/W	Port 2	00000000 _B
000013 _H	DDR3	Port 3 direction register	R/W	R/W	Port 3	00000000 _B
000014 _H	DDR4	Port 4 direction register	R/W	R/W	Port 4	0----- _B
000015 _H	DDR5	Port 5 direction register	R/W	R/W	Port 5	0000000- _B
000016 _H	DDR6	Port 6 direction register	R/W	R/W	Port 6	00000000 _B
000017 _H	DDR7	Port 7 direction register	R/W	R/W	Port 7	00000000 _B
000018 _H	PGDR	Parity generator data register	R/W	R/W	Parity generator	XXXXXXXX _B
000019 _H	PGCSR	Parity generator control status register	R/W	R/W		X-----0 _B
00001A _H	DDRA	Port A direction register	R/W	R/W	Port A	00000000 _B
00001B _H	DDRB	Port B direction register	R/W	R/W	Port B	00000000 _B
00001C _H	DDRC	Port C direction register	R/W	R/W	Port C	00000000 _B
00001D _H	DDRD	Port D direction register	R/W	R/W	Port D	00000000 _B
00001E _H	DDRE	Port E direction register	R/W	R/W	Port E	00000000 _B
00001F _H	DDR8	Port 8 direction register	R/W	R/W	Port 8	-0000--- _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000020 _H	SMR1	Serial mode register 1	R/W	R/W	UART1	00000-00 _B
000021 _H	SCR1	Serial control register 1	R/W	R/W		00000100 _B
000022 _H	SIDR1/ SODR1	Input data register 1/ Output data register 1	R/W	R/W		XXXXXXXX _B
000023 _H	SSR1	Serial status register 1	R/W	R/W		00001000 _B
000024 _H	M2CR1	Mode 2 control register 1	R/W	R/W		----1000 _B
000025 _H	CDCR1	Clock division control register 1	R/W	R/W	Communication prescaler 1	00--0000 _B
000026 _H	ENIR	Interrupt/DTP enable register	R/W	R/W	DTP/external interrupt	00000000 _B
000027 _H	EIRR	Interrupt/DTP cause register	R/W	R/W		XXXXXXXX _B
000028 _H	ELVR	Request level setting register	R/W	R/W		00000000 _B
000029 _H			R/W	R/W		00000000 _B
00002A _H	ADER1	Analog input enable register 1	R/W	R/W	Port C, A/D	11111111 _B
00002B _H	ADER2	Analog input enable register 2	R/W	R/W	Port D, A/D	----1111 _B
00002C _H	BRSR	Bridge circuit selection register	R/W	R/W	Bridge circuit	--000000 _B
00002D _H	ADC0	A/D control register	R/W	R/W	8/10-bit A/D converter	00000000 _B
00002E _H	ADCR0	A/D data register	R	R		XXXXXXXX _B
00002F _H	ADCR1		R/W	R/W		00000-XX _B
000030 _H	ADCS0	A/D control status register	R/W	R/W		00----- _B
000031 _H	ADCS1		R/W	R/W		00000000 _B
000032 _H	SICRL	Serial interrupt request register	R/W	R/W	Serial IRQ	00000000 _B
000033 _H	SICRH	Serial interrupt control register	R/W	R/W		00000000 _B
000034 _H	SIFR1	Serial interrupt frame number register 1	R/W	R/W		--000000 _B
000035 _H	SIFR2	Serial interrupt frame number register 2	R/W	R/W		--000000 _B
000036 _H	SIFR3	Serial interrupt frame number register 3	R/W	R/W		--000000 _B
000037 _H	SIFR4	Serial interrupt frame number register 4	R/W	R/W	--000000 _B	
000038 _H	PDCRL1	PPG1 down counter register	—	R	16-bit PPG timer (ch1)	11111111 _B
000039 _H	PDCRH1		—	R		11111111 _B
00003A _H	PCSRL1	PPG1 period setting register	—	W		XXXXXXXX _B
00003B _H	PCSRH1		—	W		XXXXXXXX _B
00003C _H	PDUTL1	PPG1 duty setting register	—	W		XXXXXXXX _B
00003D _H	PDUTH1		—	W		XXXXXXXX _B
00003E _H	PCNTL1	PPG1 control status register	R/W	R/W		--000000 _B
00003F _H	PCNTH1		R/W	R/W		00000000 _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
000040 _H	PDCRL2	PPG2 down counter register	—	R	16-bit PPG timer (ch2)	11111111 _B
000041 _H	PDCRH2		—	R		11111111 _B
000042 _H	PCSRL2	PPG2 period setting register	—	W		XXXXXXXX _B
000043 _H	PCSRH2		—	W		XXXXXXXX _B
000044 _H	PDUTL2	PPG2 duty setting register	—	W		XXXXXXXX _B
000045 _H	PDUTH2		—	W		XXXXXXXX _B
000046 _H	PCNTL2	PPG2 control status register	R/W	R/W		--000000 _B
000047 _H	PCNTH2		R/W	R/W	00000000 _B	
000048 _H	PDCRL3	PPG3 down counter register	—	R	16-bit PPG timer (ch3)	11111111 _B
000049 _H	PDCRH3		—	R		11111111 _B
00004A _H	PCSRL3	PPG3 period setting register	—	W		XXXXXXXX _B
00004B _H	PCSRH3		—	W		XXXXXXXX _B
00004C _H	PDUTL3	PPG3 duty setting register	—	W		XXXXXXXX _B
00004D _H	PDUTH3		—	W		XXXXXXXX _B
00004E _H	PCNTL3	PPG3 control status register	R/W	R/W		--000000 _B
00004F _H	PCNTH3		R/W	R/W	00000000 _B	
000050 _H	PSCR0	PS/2 interface control register 0	R/W	R/W	3-channel PS/2 interface	0--00000 _B
000051 _H	PSSR0	PS/2 interface status register 0	R/W	R/W		00000000 _B
000052 _H	PSCR1	PS/2 interface control register 1	R/W	R/W		0--00000 _B
000053 _H	PSSR1	PS/2 interface status register 1	R/W	R/W		00000000 _B
000054 _H	PSCR2	PS/2 interface control register 2	R/W	R/W		0--00000 _B
000055 _H	PSSR2	PS/2 interface status register 2	R/W	R/W		00000000 _B
000056 _H	PSDR0	PS/2 interface data register 0	R/W	R/W		00000000 _B
000057 _H	PSDR1	PS/2 interface data register 1	R/W	R/W		00000000 _B
000058 _H	PSDR2	PS/2 interface data register 2	R/W	R/W		00000000 _B
000059 _H	PSMR	PS/2 interface mode register	R/W	R/W		----0000 _B
00005A _H	DAT0	D/A converter data register 0	R/W	R/W	8-bit D/A converter	XXXXXXXX _B
00005B _H	DAT1	D/A converter data register 1	R/W	R/W		XXXXXXXX _B
00005C _H	DACR0	D/A control register 0	R/W	R/W		-----0 _B
00005D _H	DACR1	D/A control register 1	R/W	R/W		-----0 _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
00005E _H	UPAL1	UPI1 address register (lower)	R/W	R/W	LPC interface	XXXXXXXX _B
00005F _H	UPAH1	UPI1 address register (upper)	R/W	R/W		XXXXXXXX _B
000060 _H	UPAL2	UPI2 address register (lower)	R/W	R/W		XXXXXXXX _B
000061 _H	UPAH2	UPI2 address register (upper)	R/W	R/W		XXXXXXXX _B
000062 _H	UPAL3	UPI3 address register (lower)	R/W	R/W		XXXXXXXX _B
000063 _H	UPAH3	UPI3 address register (upper)	R/W	R/W		XXXXXXXX _B
000064 _H	UPCL	UPI control register (lower)	R/W	R/W		00000000 _B
000065 _H	UPCH	UPI control register (upper)	R/W	R/W		-000-000 _B
000066 _H	UPDI0/ UPDO0	UPI0 data input register/ data output register	R/W	R/W		XXXXXXXX _B
000067 _H	UPS0	UPI0 status register	R/W	R/W		00000000 _B
000068 _H	UPDI1/ UPDO1	UPI1 data input register/ data output register	R/W	R/W		XXXXXXXX _B
000069 _H	UPS1	UPI1 status register	R/W	R/W		00000000 _B
00006A _H	UPDI2/ UPDO2	UPI2 data input register/ data output register	R/W	R/W		XXXXXXXX _B
00006B _H	UPS2	UPI2 status register	R/W	R/W		00000000 _B
00006C _H	UPDI3/ UPDO3	UPI3 data input register/ data output register	R/W	R/W		XXXXXXXX _B
00006D _H	UPS3	UPI3 status register	R/W	R/W		00000000 _B
00006E _H	LCR	LPC control register	R/W	R/W	----000 _B	
00006F _H	ROMM	ROM mirroring function selection register	W	W	ROM mirroring function	-----1 _B
000070 _H	TMCSRL1	Timer control status register CH1 (lower)	R/W	R/W	16-bit reload timer (ch1)	00000000 _B
000071 _H	TMCSRH1	Timer control status register CH1 (upper)	R/W	R/W		----0000 _B
000072 _H	TMR1/ TMRD1	16-bit timer/reload register CH1	—	R/W		XXXXXXXX _B
000073 _H			—	R/W		XXXXXXXX _B
000074 _H	TMCSRL2	Timer control status register CH2 (lower)	R/W	R/W	16-bit reload timer (ch2)	00000000 _B
000075 _H	TMCSRH2	Timer control status register CH2 (upper)	R/W	R/W		----0000 _B
000076 _H	TMR2/ TMRD2	16-bit timer/reload register CH2	—	R/W		XXXXXXXX _B
000077 _H			—	R/W		XXXXXXXX _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value	
000078 _H	TMCSRL3	Timer control status register CH3 (lower)	R/W	R/W	16-bit reload timer (ch3)	00000000 _B	
000079 _H	TMCSRH3	Timer control status register CH3 (upper)	R/W	R/W		----0000 _B	
00007A _H	TMR3/ TMRD3	16-bit timer/reload register CH3	—	R/W		XXXXXXXX _B	
00007B _H			—	R/W		XXXXXXXX _B	
00007C _H	TMCSRL4	Timer control status register CH4 (lower)	R/W	R/W	16-bit reload timer (ch4)	00000000 _B	
00007D _H	TMCSRH4	Timer control status register CH4 (upper)	R/W	R/W		----0000 _B	
00007E _H	TMR4/ TMRD4	16-bit timer/reload register CH4	—	R/W		XXXXXXXX _B	
00007F _H			—	R/W		XXXXXXXX _B	
000080 _H	IBCRL	I ² C bus control register (lower)	R/W	R/W	I ² C	----0000 _B	
000081 _H	IBCRH	I ² C bus control register (upper)	R/W	R/W		00000000 _B	
000082 _H	IBSRL	I ² C bus status register (lower)	R	R		00000000 _B	
000083 _H	IBSRH	I ² C bus status register (upper)	R/W	R/W		--000000 _B	
000084 _H	IDAR	I ² C data register	R/W	R/W		XXXXXXXX _B	
000085 _H	IADR	I ² C address register	R/W	R/W		-XXXXXXXX _B	
000086 _H	ICCR	I ² C clock control register	R/W	R/W		0-000000 _B	
000087 _H	ITCR	I ² C timeout control register	R/W	R/W		-0-00000 _B	
000088 _H	ITOC	I ² C timeout clock register	R/W	R/W		00000000 _B	
000089 _H	ITOD	I ² C timeout data register	R/W	R/W		00000000 _B	
00008A _H	ISTO	I ² C slave timeout register	R/W	R/W		00000000 _B	
00008B _H	IMTO	I ² C master timeout register	R/W	R/W		00000000 _B	
00008C _H	RDR0	Port 0 pull-up resistor setting register	R/W	R/W		Port 0	00000000 _B
00008D _H	RDR1	Port 1 pull-up resistor setting register	R/W	R/W		Port 1	00000000 _B
00008E _H	RDR2	Port 2 pull-up resistor setting register	R/W	R/W	Port 2	00000000 _B	
00008F _H	RDR3	Port 3 pull-up resistor setting register	R/W	R/W	Port 3	00000000 _B	
000090 _H to 00009D _H	Prohibited area						
00009E _H	PACSR	Program address detect control status register	R/W	R/W	Address match detection	00000000 _B	
00009F _H	DIRR	Delayed interrupt cause/clear register	R/W	R/W	Delayed interrupt	-----0 _B	

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000A0 _H	LPMCR	Low-power consumption mode register	R/W	R/W	Low-power consumption control register	00011000 _B
0000A1 _H	CKSCR	Clock selection register	R/W	R/W		11111100 _B
0000A2 _H , 0000A3 _H	Prohibited area					
0000A4 _H	CKMC	Clock modulation control register	R/W	R/W	Clock modulation	-----0 _B
0000A5 _H to 0000A7 _H	Prohibited area					
0000A8 _H	WDTC	Watchdog control register	R/W	R/W	Watchdog timer	X-XXX111 _B
0000A9 _H	TBTC	Timebase timer control register	R/W	R/W	Timebase timer	1--00100 _B
0000AA _H	WTC	Watch timer control register	R/W	R/W	Watch timer	10001000 _B
0000AB _H	Prohibited area					
0000AC _H	EICR	Wake-up interrupt control register	R/W	R/W	Key-on wake-up interrupt	00000000 _B
0000AD _H	EIFR	Wake-up interrupt flag register	R/W	R/W		-----0 _B
0000AE _H	FMCS	Flash memory control status register	R/W	R/W	Flash memory interface circuit	000X0000 _B
0000AF _H	Prohibited area					
0000B0 _H	ICR00	Interrupt control register 00	R/W	R/W	Interrupt controller	00000111 _B
0000B1 _H	ICR01	Interrupt control register 01	R/W	R/W		00000111 _B
0000B2 _H	ICR02	Interrupt control register 02	R/W	R/W		00000111 _B
0000B3 _H	ICR03	Interrupt control register 03	R/W	R/W		00000111 _B
0000B4 _H	ICR04	Interrupt control register 04	R/W	R/W		00000111 _B
0000B5 _H	ICR05	Interrupt control register 05	R/W	R/W		00000111 _B
0000B6 _H	ICR06	Interrupt control register 06	R/W	R/W		00000111 _B
0000B7 _H	ICR07	Interrupt control register 07	R/W	R/W		00000111 _B
0000B8 _H	ICR08	Interrupt control register 08	R/W	R/W		00000111 _B
0000B9 _H	ICR09	Interrupt control register 09	R/W	R/W		00000111 _B
0000BA _H	ICR10	Interrupt control register 10	R/W	R/W		00000111 _B
0000BB _H	ICR11	Interrupt control register 11	R/W	R/W		00000111 _B
0000BC _H	ICR12	Interrupt control register 12	R/W	R/W		00000111 _B
0000BD _H	ICR13	Interrupt control register 13	R/W	R/W		00000111 _B
0000BE _H	ICR14	Interrupt control register 14	R/W	R/W		00000111 _B
0000BF _H	ICR15	Interrupt control register 15	R/W	R/W		00000111 _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000C0 _H	MBCRL	MI ² C bus control register (lower)	R/W	R/W	Multi-address I ² C	----0000 _B
0000C1 _H	MBCRH	MI ² C bus control register (upper)	R/W	R/W		00000000 _B
0000C2 _H	MBSRL	MI ² C bus status register (lower)	R	R		00000000 _B
0000C3 _H	MBSRH	MI ² C bus status register (upper)	R/W	R/W		--000000 _B
0000C4 _H	MDAR	MI ² C data register	R/W	R/W		XXXXXXXX _B
0000C5 _H	MALR	MI ² C alert register	R/W	R/W		----0000 _B
0000C6 _H	MADR1	MI ² C address register 1	R/W	R/W		-XXXXXXXX _B
0000C7 _H	MADR2	MI ² C address register 2	R/W	R/W		-XXXXXXXX _B
0000C8 _H	MADR3	MI ² C address register 3	R/W	R/W		-XXXXXXXX _B
0000C9 _H	MADR4	MI ² C address register 4	R/W	R/W		-XXXXXXXX _B
0000CA _H	MADR5	MI ² C address register 5	R/W	R/W		-XXXXXXXX _B
0000CB _H	MADR6	MI ² C address register 6	R/W	R/W		-XXXXXXXX _B
0000CC _H	MCCR	MI ² C clock control register	R/W	R/W		0-000000 _B
0000CD _H	MTCR	MI ² C timeout control register	R/W	R/W		-0-00000 _B
0000CE _H	MTOC	MI ² C timeout clock register	R/W	R/W		00000000 _B
0000CF _H	MTOD	MI ² C timeout data register	R/W	R/W		00000000 _B
0000D0 _H	MSTO	MI ² C slave timeout register	R/W	R/W		00000000 _B
0000D1 _H	MMTO	MI ² C master timeout register	R/W	R/W		00000000 _B
0000D2 _H	SMR2	Serial mode register 2	R/W	R/W	UART2	00000-00 _B
0000D3 _H	SCR2	Serial control register 2	R/W	R/W		00000100 _B
0000D4 _H	SIDR2/ SODR2	Input data register 2/ output data register 2	R/W	R/W		XXXXXXXX _B
0000D5 _H	SSR2	Status register 2	R/W	R/W		00001000 _B
0000D6 _H	M2CR2	Mode 2 control register 2	R/W	R/W		----1000 _B
0000D7 _H	CDCR2	Clock division control register 2	R/W	R/W	Communication prescaler 2	00--0000 _B
0000D8 _H	EENR1	Interrupt enable register	R/W	R/W	Extend External Interrupt 1	00000000 _B
0000D9 _H	EERR1	Interrupt cause register	R/W	R/W		XXXXXXXX _B
0000DA _H 0000DB _H	EELR1	Request level setting register	R/W R/W	R/W R/W		00000000 _B 00000000 _B
0000DC _H	EENR2	Interrupt enable register	R/W	R/W	Extend External Interrupt 2	00000000 _B
0000DD _H	EERR2	Interrupt cause register	R/W	R/W		XXXXXXXX _B
0000DE _H 0000DF _H	EELR2	Request level setting register	R/W R/W	R/W R/W		00000000 _B 00000000 _B
0000E0 _H	PDL3	Port 3 data latch register	R/W	R/W		Port 3 data latch

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
0000E1 _H	BDR	Bit data register	R/W	R/W	Bit decoder	----XXXX _B
0000E2 _H	BRRL	Bit result register (lower)	R	R		XXXXXXXX _B
0000E3 _H	BRRH	Bit result register (upper)	R	R		XXXXXXXX _B
0000E4 _H	SMR3	Serial mode register 3	R/W	R/W	UART3	00000-00 _B
0000E5 _H	SCR3	Serial control register 3	R/W	R/W		00000100 _B
0000E6 _H	SIDR3 / SODR3	Input data register 3/ output data register 3	R/W	R/W		XXXXXXXX _B
0000E7 _H	SSR3	Status register 3	R/W	R/W		00001000 _B
0000E8 _H	M2CR3	Mode 2 control register 3	R/W	R/W		----1000 _B
0000E9 _H	CDCR3	Clock division control register 3	R/W	R/W	Communication prescaler 3	00--0000 _B
0000EA _H	TMCSRL5	Timer control status register CH5 (lower)	R/W	R/W	16-bit reload timer (ch5)	00000000 _B
0000EB _H	TMCSRH5	Timer control status register CH5 (upper)	R/W	R/W		----0000 _B
0000EC _H	TMR5/ TMRD5	16-bit timer/reload register CH5	—	R/W		XXXXXXXX _B
0000ED _H			—	R/W		XXXXXXXX _B
0000EE _H	LCRL	LCD control register 0	R/W	R/W	LCD controller/driver	00010000 _B
0000EF _H	LCRH	LCD control register 1	R/W	R/W		00000000 _B
0000F0 _H to 0000F4 _H	VRAM	LCD display RAM	R/W	-		XXXXXXXX _B
0000F5 _H to 0000F7 _H	Prohibited area					
0000F8 _H to 0000FF _H	External area					
000100 _H to 0018FF _H	Prohibited area (RAM area)					
001FF0 _H	PADR0	Program address detection register 0	R/W	R/W	Address match detection	XXXXXXXX _B
001FF1 _H		Program address detection register 1	R/W	R/W		XXXXXXXX _B
001FF2 _H		Program address detection register 2	R/W	R/W		XXXXXXXX _B

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
001FF3 _H	PADR1	Program address detection register 3	R/W	R/W	Address match detection	XXXXXXXX _B
001FF4 _H		Program address detection register 4	R/W	R/W		XXXXXXXX _B
001FF5 _H		Program address detection register 5	R/W	R/W		XXXXXXXX _B
001FF6 _H to 003F7F _H	Prohibited area					
003F80 _H	UDRL10	UP data register 10 (lower)	R/W	R/W	LPC data buffer array-Extend	XXXXXXXX _B
003F81 _H	UDRH10	UP data register 10 (upper)	R/W	R/W		XXXXXXXX _B
003F82 _H	UDRL11	UP data register 11 (lower)	R/W	R/W		XXXXXXXX _B
003F83 _H	UDRH11	UP data register 11 (upper)	R/W	R/W		XXXXXXXX _B
003F84 _H	UDRL12	UP data register 12 (lower)	R/W	R/W		XXXXXXXX _B
003F85 _H	UDRH12	UP data register 12 (upper)	R/W	R/W		XXXXXXXX _B
003F86 _H	UDRL13	UP data register 13 (lower)	R/W	R/W		XXXXXXXX _B
003F87 _H	UDRH13	UP data register 13 (upper)	R/W	R/W		XXXXXXXX _B
003F88 _H	UDRL14	UP data register 14 (lower)	R/W	R/W		XXXXXXXX _B
003F89 _H	UDRH14	UP data register 14 (upper)	R/W	R/W		XXXXXXXX _B
003F8A _H	UDRL15	UP data register 15 (lower)	R/W	R/W		XXXXXXXX _B
003F8B _H	UDRH15	UP data register 15 (upper)	R/W	R/W		XXXXXXXX _B
003F8C _H	UDRL16	UP data register 16 (lower)	R/W	R/W		XXXXXXXX _B
003F8D _H	UDRH16	UP data register 16 (upper)	R/W	R/W		XXXXXXXX _B
003F8E _H	UDRL17	UP data register 17 (lower)	R/W	R/W		XXXXXXXX _B
003F8F _H	UDRH17	UP data register 17 (upper)	R/W	R/W		XXXXXXXX _B
003F90 _H	UDRL18	UP data register 18 (lower)	R/W	R/W		XXXXXXXX _B
003F91 _H	UDRH18	UP data register 18 (upper)	R/W	R/W		XXXXXXXX _B
003F92 _H	UDRL19	UP data register 19 (lower)	R/W	R/W		XXXXXXXX _B
003F93 _H	UDRH19	UP data register 19 (upper)	R/W	R/W		XXXXXXXX _B
003F94 _H	UDRL1A	UP data register 1A (lower)	R/W	R/W		XXXXXXXX _B
003F95 _H	UDRH1A	UP data register 1A (upper)	R/W	R/W		XXXXXXXX _B
003F96 _H	UDRL1B	UP data register 1B (lower)	R/W	R/W		XXXXXXXX _B
003F97 _H	UDRH1B	UP data register 1B (upper)	R/W	R/W		XXXXXXXX _B
003F98 _H	UDRL1C	UP data register 1C (lower)	R/W	R/W		XXXXXXXX _B
003F99 _H	UDRH1C	UP data register 1C (upper)	R/W	R/W		XXXXXXXX _B
003F9A _H	UDRL1D	UP data register 1D (lower)	R/W	R/W		XXXXXXXX _B
003F9B _H	UDRH1D	UP data register 1D (upper)	R/W	R/W	XXXXXXXX _B	

(Continued)

MB90378 Series

Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003F9C _H	UDRL1E	UP data register 1E (lower)	R/W	R/W	LPC data buffer array-Extend	XXXXXXXX _B
003F9D _H	UDRH1E	UP data register 1E (upper)	R/W	R/W		XXXXXXXX _B
003F9E _H	UDRL1F	UP data register 1F (lower)	R/W	R/W		XXXXXXXX _B
003F9F _H	UDRH1F	UP data register 1F (upper)	R/W	R/W		XXXXXXXX _B
003FA0 _H	DBACLR	Data buffer array clear register	R/W	R/W	LPC data buffer array	----000 _B
003FA1 _H	Prohibited area					
003FA2 _H	FWR0	FLASH programming control register 0	R/W	R/W	Dual operating FLASH	00000000 _B
003FA3 _H	FWR1	FLASH programming control register 1	R/W	R/W		00000000 _B
003FA4 _H	SSR0	Sector switching register	R/W	R/W		00XXXXX0 _B
003FA5 _H to 003FAE _H	Prohibited area					
003FAF _H	PCKCR	PLL clock control register	W	W	PLL	XXXX0000 _B
003FB0 _H	PRL2	PPG reload register (lower)	R/W	R/W	8/16-bit PPG timer 2	XXXXXXXX _B
003FB1 _H	PRLH2	PPG reload register (upper)	R/W	R/W		XXXXXXXX _B
003FB2 _H	PRL3	PPG reload register (lower)	R/W	R/W		XXXXXXXX _B
003FB3 _H	PRLH3	PPG reload register (upper)	R/W	R/W		XXXXXXXX _B
003FB4 _H	PPGC2	PPG control register ch2	R/W	R/W		00000001 _B
003FB5 _H	PPGC3	PPG control register ch3	R/W	R/W		00000001 _B
003FB6 _H	PCS23	PPG clock control register	R/W	R/W		000000XX _B
003FB7 _H to 003FBF _H	Prohibited area					
003FC0 _H	UDRL0	UP data register 0 (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX _B
003FC1 _H	UDRH0	UP data register 0 (upper)	R/W	R/W		XXXXXXXX _B
003FC2 _H	UDRL1	UP data register 1 (lower)	R/W	R/W		XXXXXXXX _B
003FC3 _H	UDRH1	UP data register 1 (upper)	R/W	R/W		XXXXXXXX _B
003FC4 _H	UDRL2	UP data register 2 (lower)	R/W	R/W		XXXXXXXX _B
003FC5 _H	UDRH2	UP data register 2 (upper)	R/W	R/W		XXXXXXXX _B
003FC6 _H	UDRL3	UP data register 3 (lower)	R/W	R/W		XXXXXXXX _B
003FC7 _H	UDRH3	UP data register 3 (upper)	R/W	R/W		XXXXXXXX _B
003FC8 _H	UDRL4	UP data register 4 (lower)	R/W	R/W		XXXXXXXX _B
003FC9 _H	UDRH4	UP data register 4 (upper)	R/W	R/W		XXXXXXXX _B

(Continued)

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003FCA _H	UDRL5	UP data register 5 (lower)	R/W	R/W	LPC data buffer array	XXXXXXXX _B
003FCB _H	UDRH5	UP data register 5 (upper)	R/W	R/W		XXXXXXXX _B
003FCC _H	UDRL6	UP data register 6 (lower)	R/W	R/W		XXXXXXXX _B
003FCD _H	UDRH6	UP data register 6 (upper)	R/W	R/W		XXXXXXXX _B
003FCE _H	UDRL7	UP data register 7 (lower)	R/W	R/W		XXXXXXXX _B
003FCF _H	UDRH7	UP data register 7 (upper)	R/W	R/W		XXXXXXXX _B
003FD0 _H	UDRL8	UP data register 8 (lower)	R/W	R/W		XXXXXXXX _B
003FD1 _H	UDRH8	UP data register 8 (upper)	R/W	R/W		XXXXXXXX _B
003FD2 _H	UDRL9	UP data register 9 (lower)	R/W	R/W		XXXXXXXX _B
003FD3 _H	UDRH9	UP data register 9 (upper)	R/W	R/W		XXXXXXXX _B
003FD4 _H	UDRLA	UP data register A (lower)	R/W	R/W		XXXXXXXX _B
003FD5 _H	UDRHA	UP data register A (upper)	R/W	R/W		XXXXXXXX _B
003FD6 _H	UDRLB	UP data register B (lower)	R/W	R/W		XXXXXXXX _B
003FD7 _H	UDRHB	UP data register B (upper)	R/W	R/W		XXXXXXXX _B
003FD8 _H	UDRLC	UP data register C (lower)	R/W	R/W		XXXXXXXX _B
003FD9 _H	UDRHC	UP data register C (upper)	R/W	R/W		XXXXXXXX _B
003FDA _H	UDRLD	UP data register D (lower)	R/W	R/W		XXXXXXXX _B
003FDB _H	UDRHD	UP data register D (upper)	R/W	R/W		XXXXXXXX _B
003FDC _H	UDRLE	UP data register E (lower)	R/W	R/W		XXXXXXXX _B
003FDD _H	UDRHE	UP data register E (upper)	R/W	R/W		XXXXXXXX _B
003FDE _H	UDRLF	UP data register F (lower)	R/W	R/W		XXXXXXXX _B
003FDF _H	UDRHF	UP data register F (upper)	R/W	R/W		XXXXXXXX _B
003FE0 _H	DNDL0	DOWN data register 0 (lower)	R	R		XXXXXXXX _B
003FE1 _H	DNDH0	DOWN data register 0 (upper)	R	R		XXXXXXXX _B
003FE2 _H	DNDL1	DOWN data register 1 (lower)	R	R		XXXXXXXX _B
003FE3 _H	DNDH1	DOWN data register 1 (upper)	R	R		XXXXXXXX _B
003FE4 _H	DNDL2	DOWN data register 2 (lower)	R	R		XXXXXXXX _B
003FE5 _H	DNDH2	DOWN data register 2 (upper)	R	R		XXXXXXXX _B
003FE6 _H	DNDL3	DOWN data register 3 (lower)	R	R		XXXXXXXX _B
003FE7 _H	DNDH3	DOWN data register 3 (upper)	R	R		XXXXXXXX _B
003FE8 _H	DNDL4	DOWN data register 4 (lower)	R	R		XXXXXXXX _B
003FE9 _H	DNDH4	DOWN data register 4 (upper)	R	R		XXXXXXXX _B
003FEA _H	DNDL5	DOWN data register 5 (lower)	R	R	XXXXXXXX _B	
003FEB _H	DNDH5	DOWN data register 5 (upper)	R	R	XXXXXXXX _B	
003FEC _H	DNDL6	DOWN data register 6 (lower)	R	R	XXXXXXXX _B	
003FED _H	DNDH6	DOWN data register 6 (upper)	R	R	XXXXXXXX _B	

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Address	Abbreviation	Register	Byte access	Word access	Resource name	Initial value
003FEE _H	DNDL7	DOWN data register 7 (lower)	R	R	LPC data buffer array	XXXXXXXX _B
003FEF _H	DNDH7	DOWN data register 7 (upper)	R	R		XXXXXXXX _B
003FF0 _H	DBAAL	Data buffer array address register (lower)	R/W	R/W		XXXXXXXX _B
003FF1 _H	DBAAH	Data buffer array address register (upper)	R/W	R/W		XXXXXXXX _B
003FF2 _H , 003FF3 _H	Prohibited area					
003FF4 _H	TMCSRL6	Timer control status register CH6 (lower)	R/W	R/W	16-bit reload timer (ch6)	0000000 _B
003FF5 _H	TMCSRH6	Timer control status register CH6 (upper)	R/W	R/W		----0000 _B
003FF6 _H	TMR6/ TMRD6	16-bit timer/reload register CH6	—	R/W		XXXXXXXX _B
003FF7 _H			—	R/W		XXXXXXXX _B
003FF8 _H	PRLLO	PPG reload register (lower)	R/W	R/W	8/16-bit PPG timer 1	XXXXXXXX _B
003FF9 _H	PRLH0	PPG reload register (upper)	R/W	R/W		XXXXXXXX _B
003FFA _H	PRLLO	PPG reload register (lower)	R/W	R/W		XXXXXXXX _B
003FFB _H	PRLH1	PPG reload register (upper)	R/W	R/W		XXXXXXXX _B
003FFC _H	PPGC0	PPG control register ch0	R/W	R/W		00000001 _B
003FFD _H	PPGC1	PPG control register ch1	R/W	R/W		00000001 _B
003FFE _H	PCS01	PPG clock control register	R/W	R/W		000000XX _B
003FFF _H	Prohibited area					

- Meaning of abbreviations used for reading and writing

R/W : Readable and writable

R : Read-only

W : Write-only

- Explanation of initial values

0 : The bit is initialized to 0.

1 : The bit is initialized to 1.

X : The initial value of the bit is undefined.

- : The bit is not used. Its initial value is undefined.

- Instruction using IO addressing e.g. MOV A, io, is not supported for registers area 003F80_H to 003FFF_H.

MB90378 Series

■ INTERRUPT FACTORS, INTERRUPT VECTORS, INTERRUPT CONTROL REGISTER

Interrupt cause	EI ² OS support	Interrupt vector		Interrupt control register		Priority*2
		Number	Address	ICR	Address	
Reset	×	#08	08H	FFFFDC _H	—	High ↑
INT9 instruction	×	#09	09H	FFFFD8 _H	—	
Exception processing	×	#10	0AH	FFFFD4 _H	—	
A/D converter conversion termination	○	#11	0BH	FFFFD0 _H	ICR00	0000B0 _H *1
Timebase timer	△	#12	0CH	FFFFCC _H		
UPI0 IBF/LPC reset	△	#13	0DH	FFFFC8 _H	ICR01	0000B1 _H *1
UPI1 IBF	△	#14	0EH	FFFFC4 _H		
UPI2 IBF	△	#15	0FH	FFFFC0 _H	ICR02	0000B2 _H *1
UPI3 IBF	△	#16	10H	FFFFBC _H		
DTP/ext. interrupt channels 0/1 detection	○	#17	11H	FFFFB8 _H	ICR03	0000B3 _H *1
DTP/ext. interrupt channels 2/3 detection	○	#18	12H	FFFFB4 _H		
DTP/ext. interrupt channels 4/5 detection	○	#19	13H	FFFFB0 _H	ICR04	0000B4 _H *1
Key-on wake-up interrupt detection	△	#20	14H	FFFFAC _H		
UPI0/1/2/3 OBE	△	#21	15H	FFFFA8 _H	ICR05	0000B5 _H *2
16-bit PPG timer 1 / 8/16-bit PPG timer 0/1	△	#22	16H	FFFFA4 _H		
PS/2 interface 0/1	△	#23	17H	FFFFA0 _H	ICR06	0000B6 _H *1
PS/2 interface 2	△	#24	18H	FFFF9C _H		
Watch timer	△	#25	19H	FFFF98 _H	ICR07	0000B7 _H *1
I ² C transfer complete / bus error	△	#26	1AH	FFFF94 _H		
16-bit PPG timer 2/3	○	#27	1BH	FFFF90 _H	ICR08	0000B8 _H *1
DTP/ext. interrupt channels 6/7 detection	○	#28	1CH	FFFF8C _H		
Multi-address I ² C transfer complete / bus error	△	#29	1DH	FFFF88 _H	ICR09	0000B9 _H *1
Extend External Interrupt 00 to 07/08 to 15	○	#30	1EH	FFFF84 _H		
I ² C timeout / standby wake-up	△	#31	1FH	FFFF80 _H	ICR10	0000BA _H *1
16-bit reload timer 1/2/5 underflow	○	#32	20H	FFFF7C _H		
Multi-address I ² C timeout / standby wake-up	△	#33	21H	FFFF78 _H	ICR11	0000BB _H *1
16-bit reload timer 3/4/6 underflow	○	#34	22H	FFFF74 _H		
UART1 receive	◎	#35	23H	FFFF70 _H	ICR12	0000BC _H *1
UART1 send	△	#36	24H	FFFF6C _H		
UART2 receive	◎	#37	25H	FFFF68 _H	ICR13	0000BD _H *1
UART2 send	△	#38	26H	FFFF64 _H		
UART3 receive	◎	#39	27H	FFFF60 _H	ICR14	0000BE _H *1
UART3 send	△	#40	28H	FFFF5C _H		
Flash memory status	△	#41	29H	FFFF58 _H	ICR15	0000BF _H *1
Delayed interrupt generator module	△	#42	2AH	FFFF54 _H		

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- : Can be used and interrupt request flag is cleared by EI²OS interrupt clear signal.
- × : Cannot be used.
- ◎ : Can be used and support the EI²OS stop request.
- △ : Can be used.

- *1 :
- For peripheral functions that share the ICR register, the interrupt level will be the same.
 - If the extended intelligent I/O service is to be used with a peripheral function that shares the ICR register with another peripheral function, the service can be started by either of the function. And if EI²OS clear is supported, both interrupt request flags for the two interrupt causes are cleared by EI²OS interrupt clear signal. It is recommended to mask either of the interrupt request during the use of EI²OS.
 - EI²OS service cannot be started multiple times simultaneously. Interrupt other than the operating interrupt is masked during EI²OS operation. It is recommended to mask either of the interrupt requests during the use of EI²OS.

*2 : This priority is applied when interrupts of the same level occur simultaneously.

MB90378 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Rating

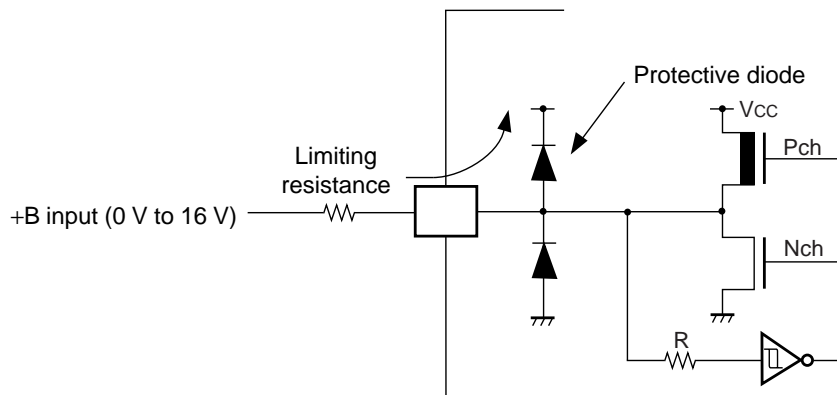
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$V_{CC} \geq AV_{CC}$ *2
A/D converter reference input voltage*1	AVR	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$AV_{CC} \geq AVR$, $AVR \geq AV_{SS}$
LCD power supply voltage*1	V1 to V3	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	V1 to V3 must not exceed V_{CC}
Input voltage*1	V_{I1}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	All pins except P40 to P45, P80 to P82, P90 to P95 *3
	V_{I2}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	P40 to P45, P80 to P82, P90 to P95
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*3
Maximum clamp current	I_{CLAMP}	- 2.0	+ 2.0	mA	*5
Total maximum clamp current	$\sum I_{CLAMP} $	—	20	mA	*5
“L” level maximum output current	I_{OL1}	—	10	mA	All pins except PF0 to PF7 *4
	I_{OL2}	—	20	mA	PF0 to PF7 *4
“L” level average output current	I_{OLAV1}	—	4	mA	All pins except PF0 to PF7 Average output current = operating current × operating efficiency
	I_{OLAV2}	—	12	mA	PF0 to PF7 Average output current = operating current × operating efficiency
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	50	mA	Average output current = operating current × operating efficiency
“H” level maximum output current	I_{OH}	—	- 10	mA	*4
“H” level average output current	I_{OHAV}	—	- 3	mA	Average output current = operating current × operating efficiency
“H” level total maximum output current	$\sum I_{OH}$	—	- 100	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	- 50	mA	Average output current = operating current × operating efficiency
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	- 40	+ 85	°C	
Storage temperature	T_{stg}	- 55	+ 150	°C	

(Continued)

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- *1 : This parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.
- *2 : Set AV_{CC} and V_{CC} at the same voltage. Take care so that AVR does not exceed $V_{CC} + 0.3$ V when the power is turned on.
- *3 : V_I and V_O shall never exceed $V_{CC} + 0.3$ V.
- *4 : The maximum output current is a peak value for a corresponding pin.
- *5 :
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to poerate the power-on reset.
 - Care must be taken not to leave the +B input pin open.
 - Note that analog system input/output pins other than the A/D input pins (LCD drive pins, etc.) cannot accept +B signal input.
 - Sample recommended circuits :

• Input/output equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

MB90378 Series

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage *2	V_{CC}	2.7 *1	3.6	V	Normal operation assurance range
	V_{CC}	1.8	3.6	V	Retains the RAM state in stop mode
A/D converter reference input voltage *3	AVR	0	AV_{CC}	V	Normal operation assurance range
LCD power supply voltage	V1 to V3	V_{SS}	V_{CC}	V	V1 to V3 pins (The optimum value is dependent on the LCD element in use.)
Operating temperature	T_A	- 40	+ 85	°C	

*1 : The operating voltage varies with the operation frequency.

*2 : Set AV_{CC} and V_{CC} at the same voltage.

*3 : Take care so that AVR does not exceed $V_{CC} + 0.3\text{ V}$ when power is turned on.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P10 to P17, P20 to P27, P30 to P37, P46, P47, P51 to P57, PC0 to PC7, PD0 to PD7	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input pins
	V_{IHS}	P00 to P07, P60 to P67, P70 to P77, P83 to P86, PA0 to PA7, PB0 to PB7, PE0 to PE7, PF0 to PF7, RST		$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS hysteresis input pins
	V_{IHS5}	P40 to P45		$0.8 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS hysteresis input pins
	V_{IH5}	P50, P82		$0.7 V_{CC}$	—	$V_{SS} + 5.5$	V	5 V tolerant CMOS input pins
	V_{IHSM}	P80, P81, P90 to P95		2.1	—	$V_{SS} + 5.5$	V	SMbus input pins
	V_{IHM}	MD0 to MD2		$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	Mode pins
"L" level input voltage	V_{IL}	P10 to P17, P20 to P27, P30 to P37, P46, P47, P50 to P57, P82, PC0 to PC7, PD0 to PD7	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	CMOS input pins
	V_{ILS}	P00 to P07, P40 to P45, P60 to P67, P70 to P77, P83 to P86, PA0 to PA7, PB0 to PB7, PE0 to PE7, PF0 to PF7, RST		$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	CMOS hysteresis input pins
	V_{ILSM}	P80, P81, P90 to P95		$V_{SS} - 0.3$	—	0.8	V	SMbus input pins
	V_{ILM}	MD0 to MD2		$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode pins
Open-drain output pin application voltage	V_{D5}	P40 to P45, P50, P80 to P82, P90 to P95	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
	V_D	P46, PF0 to PF7		$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	
"H" level output voltage	V_{OH1}	All port pins except P40 to P46, P50, P80 to P82, P90 to P95, PF0 to PF7	$V_{CC} = 3.0\text{ V}$ $I_{OH1} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	V_{OL1}	All port pins except PF0 to PF7	$I_{OL1} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OL2}	PF0 to PF7	$I_{OL2} = 12.0\text{ mA}$	—	—	0.4	V	

(Continued)

MB90378 Series

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current (Hi-Z output leakage current)	I_{IL}	All input pins	$V_{CC} = 3.3\text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	—	5	μA	
Open-drain output leakage current	I_{LEAK}	P40 to P46, P50, P80 to P82, P90 to P95, PF0 to PF7	—	—	—	5	μA	
Power supply current*	I_{CC}	V_{CC}	$V_{CC} = 3.3\text{ V}$, Internal operation at 20 MHz	—	56	68	mA	
	I_{CCS}		$V_{CC} = 3.3\text{ V}$, Internal operation at 20 MHz, In sleep mode	—	23	30	mA	
	I_{CCL}		$V_{CC} = 3.3\text{ V}$, External 32 kHz, Internal operation at 8 kHz, In sub-clock mode, $T_A = +25\text{ }^\circ\text{C}$	—	23	80	μA	
	I_{CCLS}		$V_{CC} = 3.3\text{ V}$, External 32 kHz, Internal operation at 8 kHz, In sub-clock sleep mode, $T_A = +25\text{ }^\circ\text{C}$	—	10	50	μA	
	I_{CCWAT}		$V_{CC} = 3.3\text{ V}$, External 32 kHz, Internal operation at 8 kHz, In watch mode, $T_A = +25\text{ }^\circ\text{C}$	—	1.5	30	μA	
Power supply current*	I_{CCT}	V_{CC}	$V_{CC} = 3.3\text{ V}$, Internal operation at 20 MHz, In timebase timer mode	—	2.0	3	mA	
	I_{CCH}		$V_{CC} = 3.3\text{ V}$, In stop mode, $T_A = +25\text{ }^\circ\text{C}$	—	1	20	μA	
Input capacitance	C_{IN}	All input pins except V_{CC} , AV_{CC} , V_{SS} , AV_{SS}	—	—	10	80	pF	

(Continued)

(Continued)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCD divided resistance	R _{LCD}	—	Between V _{CC} and V3 at V _{CC} = 3.3 V	100	200	400	kΩ	
			Between V3 and V2 Between V2 and V1 Between V1 and V _{SS} at V _{CC} = 3.3 V	50	100	200		
COM0 to COM3 output impedance	R _{VCOM}	COM0 to COM3	V1 to V3 = 3.3 V	—	—	5	kΩ	
SEG0 to SEG8 output impedance	R _{VSEG}	SEG0 to SEG8		—	—	5	kΩ	
LCD leakage current	L _{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG8	—	—	±1	μA		
Pull-up resistance	R _{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, RST	—	25	50	100	kΩ	
Pull-down resistance	R _{DOWN}	MD2	—	25	50	100	kΩ	MB90V378 only

* : The current value is preliminary value and may be subject to change for enhanced characteristics without previous notice. The power supply current is measured with an external clock.

MB90378 Series

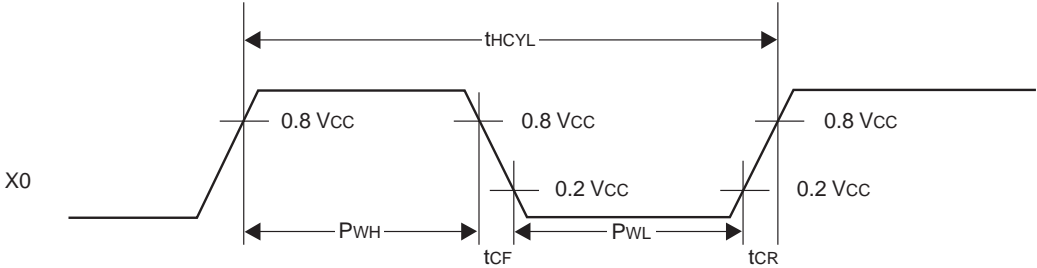
4. AC Characteristics

(1) Clock Timings

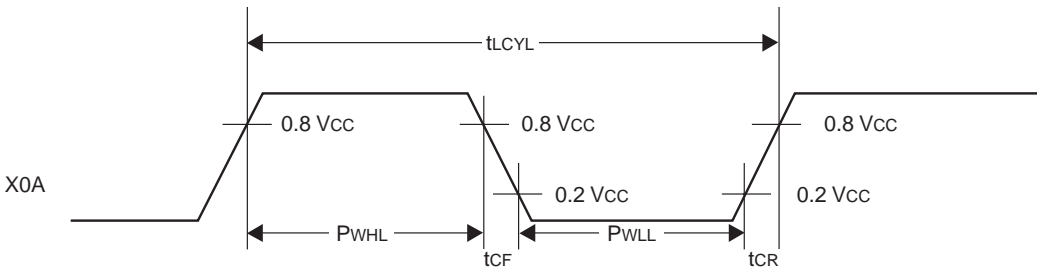
($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_{CH}	X0, X1	—	3	—	16	MHz	$\times 1/2$ (When PLL stops) When using an oscillation circuit
				4	—	16	MHz	PLL $\times 1$ When using an oscillation circuit
				4	—	10	MHz	PLL $\times 2$ When using an oscillation circuit
				4	—	6.67	MHz	PLL $\times 3$ When using an oscillation circuit
				4	—	5	MHz	PLL $\times 4$ When using an oscillation circuit
				3	—	32	MHz	$\times 1/2$ (When PLL stops) When using an external clock
				4	—	20	MHz	PLL $\times 1$ When using an external clock
				4	—	10	MHz	PLL $\times 2$ When using an external clock
				4	—	6.67	MHz	PLL $\times 3$ When using an external clock
				4	—	5	MHz	PLL $\times 4$ When using an external clock
	f_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	$t_{H_{CYL}}$	X0, X1	—	31.25	—	333	ns	
	$t_{L_{CYL}}$	X0A, X1A	—	—	30.5	—	μs	
Frequency fluctuation rate locked*	Δf	—	—	—	—	5	%	
Input clock pulse width	P_{WH} P_{WL}	X0	—	5	—	—	ns	Recommend duty ratio of 30% to 70%
	P_{WHL} P_{WLL}	X0A	—	—	15.2	—	μs	Recommend duty ratio of 30% to 70%
Input clock rise/fall time	t_{CR} t_{CF}	X0	—	—	—	5	ns	External clock operation
Internal operating clock frequency	f_{CP}	—	—	1.5	—	20	MHz	Main clock operation
	f_{LCP}	—	—	—	8.192	—	kHz	Sub-clock operation
Internal operating clock cycle time	t_{CP}	—	—	50	—	666	ns	Main clock operation
	t_{LCP}	—	—	—	122.1	—	μs	Sub-clock operation

- X0, X1 clock timing



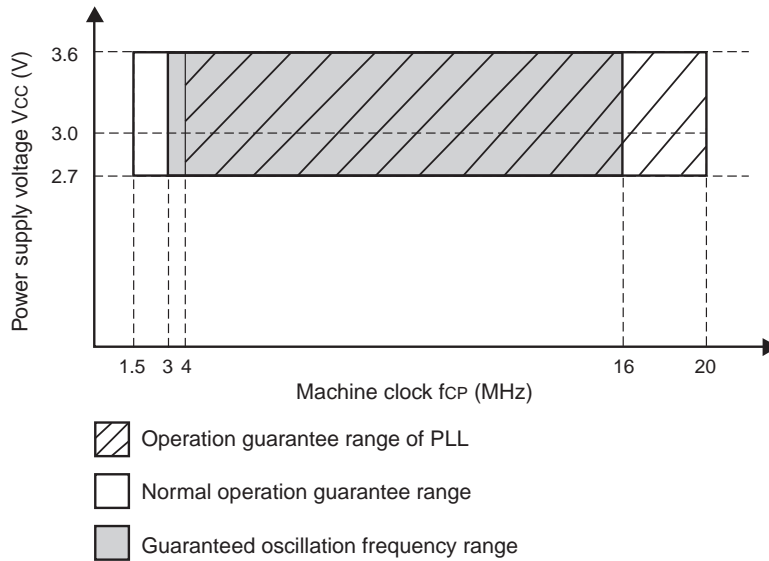
- X0A, X1A clock timing



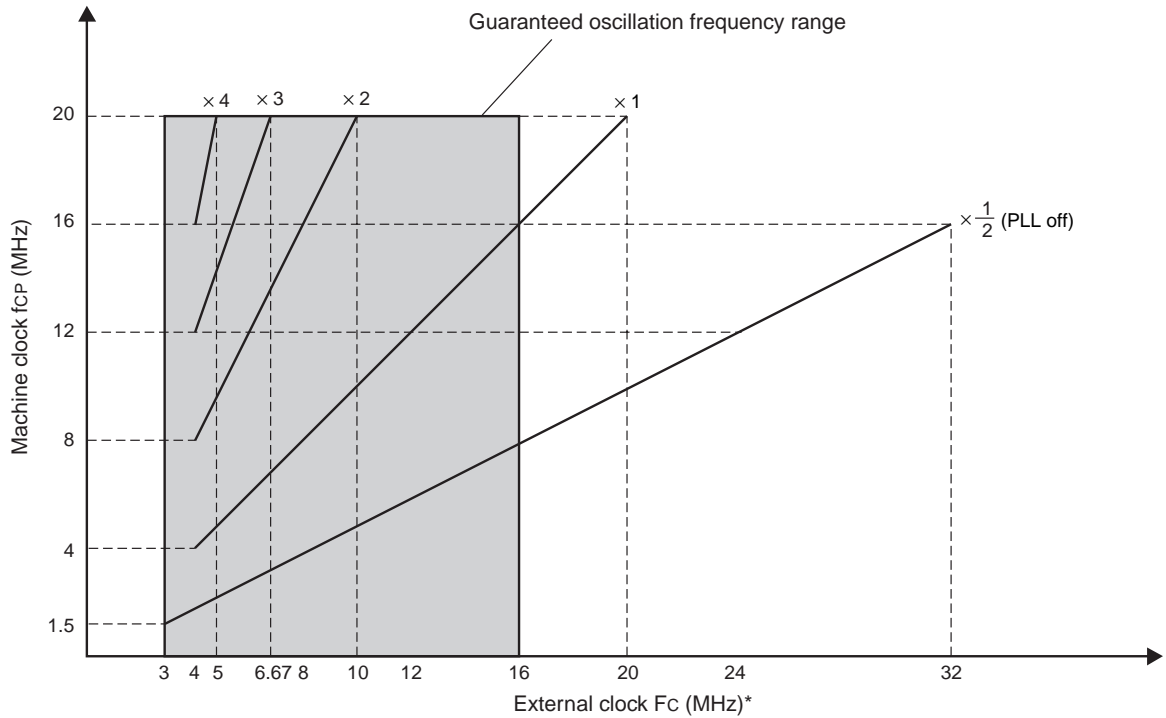
MB90378 Series

- PLL operation guarantee range

Relationship between machine clock frequency and power supply voltage

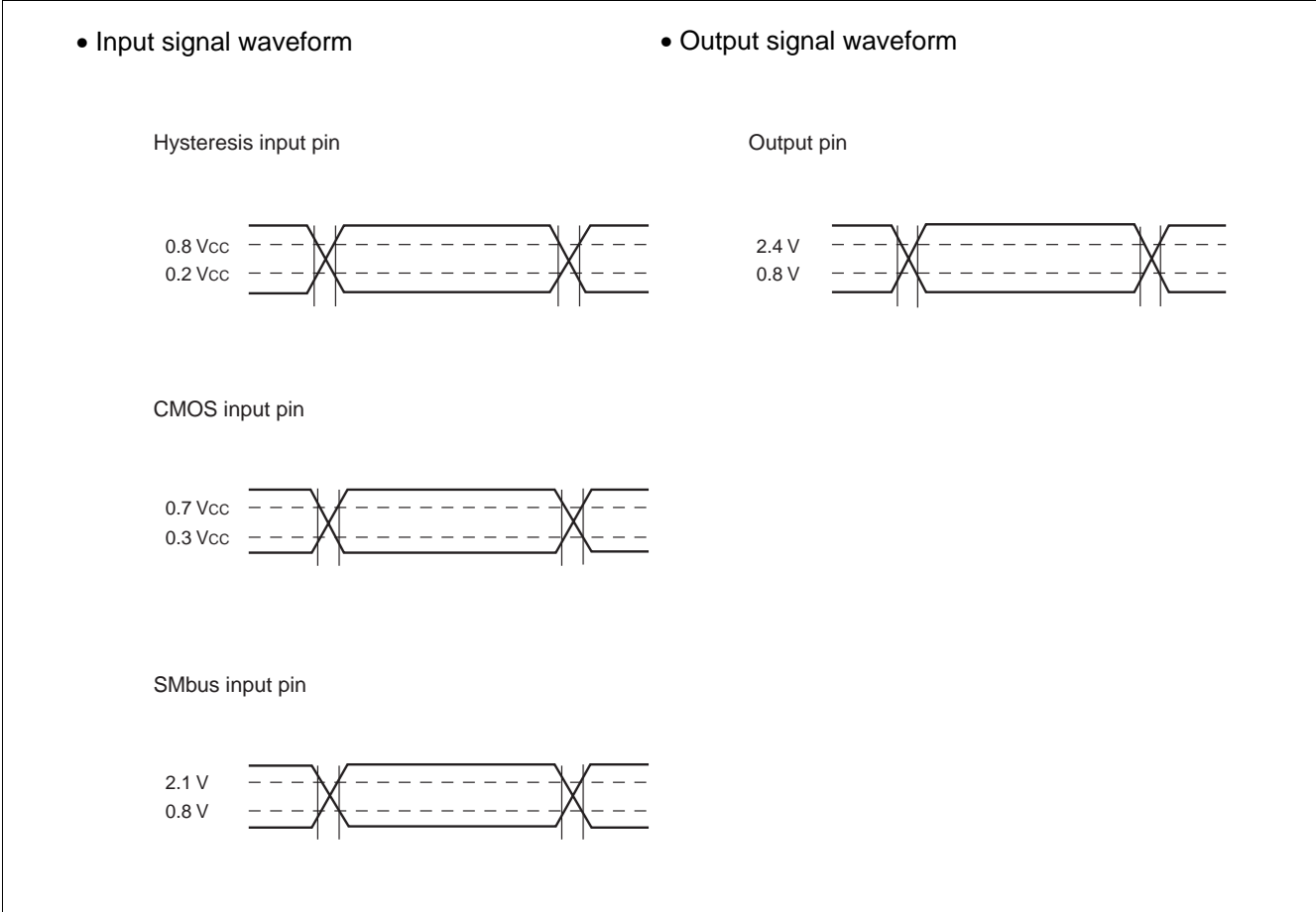


Relationship between external clock frequency and machine clock frequency



* : When using a crystal oscillator or a ceramic oscillator, the maximum oscillation clock frequency is 16 MHz.

The AC ratings are measured for the following measurement reference voltages :



MB90378 Series

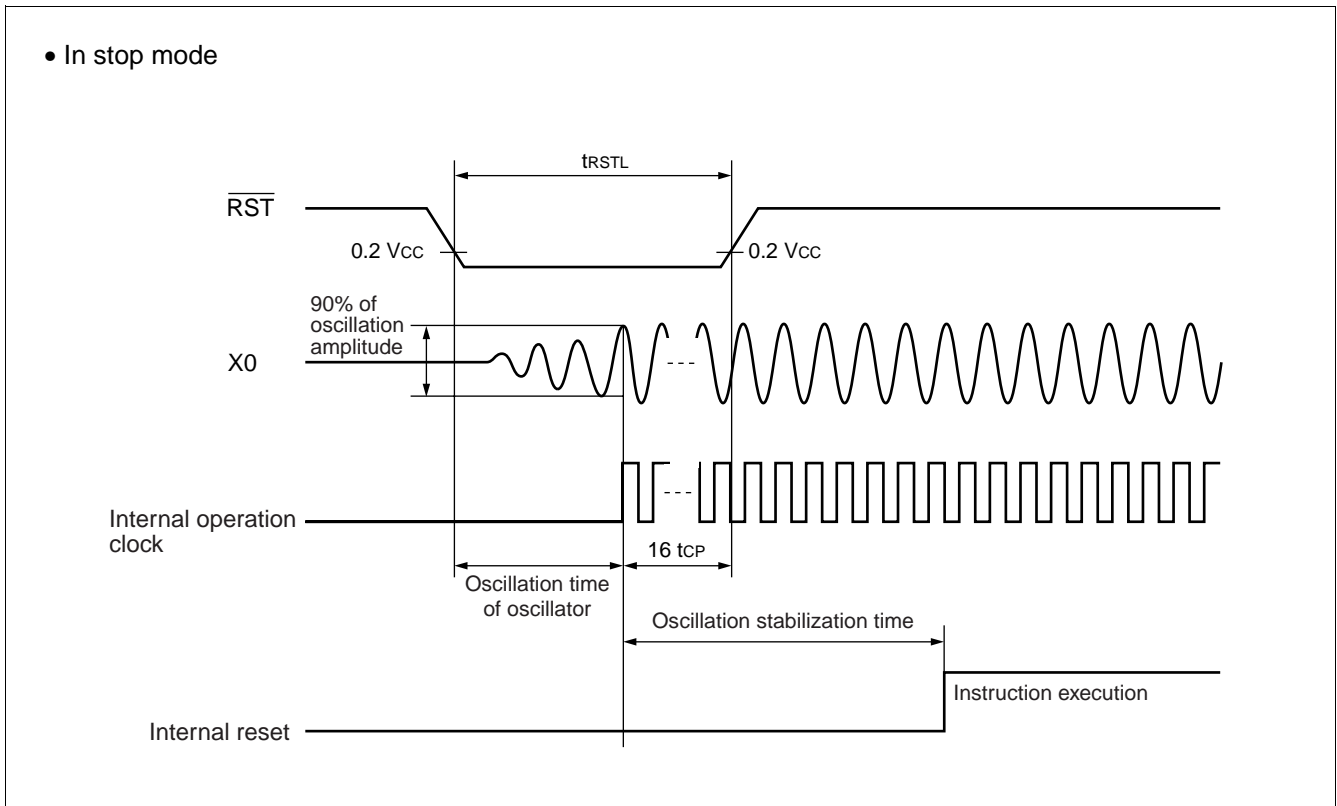
(2) Reset Input Timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	\overline{RST}	—	16 t_{CP}	—	ns	Normal operation
				Oscillation time of oscillator* + 16 t_{CP}	—	ms	In stop mode and sub-clock mode

* : Oscillation time of oscillator is the time to reach to 90% of the oscillation amplitude from stand still. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR/ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for t_{CP} .



(3) Power-on Reset

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

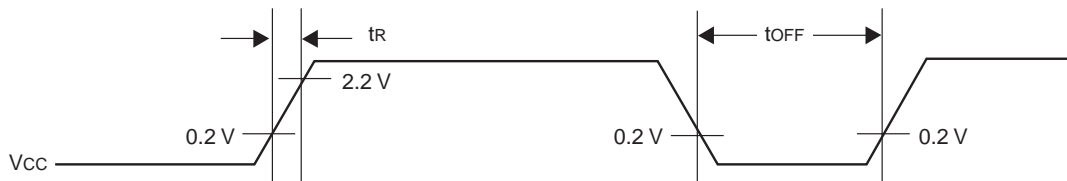
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}^*	—	—	50	ms	
Power supply cut-off time	t_{OFF}	V_{CC}^*	—	1	—	ms	Due to repeated operations

* : V_{CC} must be kept lower than 0.2 V before power-on.

Notes : • The above values are used for causing a power-on reset.

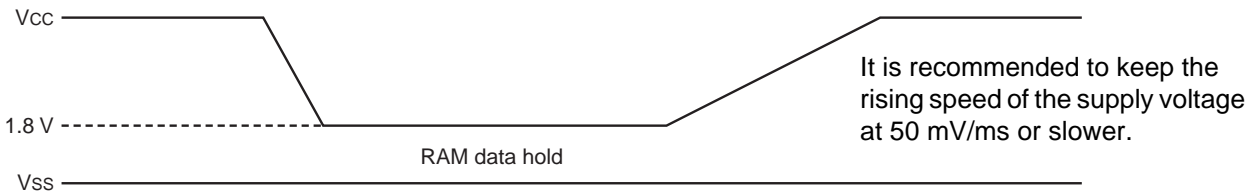
Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.

- Make sure that power supply rises within the selected oscillation stabilization time. If the power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



Sudden changes in the power supply voltage may cause a power-on reset.

To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below. In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or fewer per second, however, you can use the PLL clock.



MB90378 Series

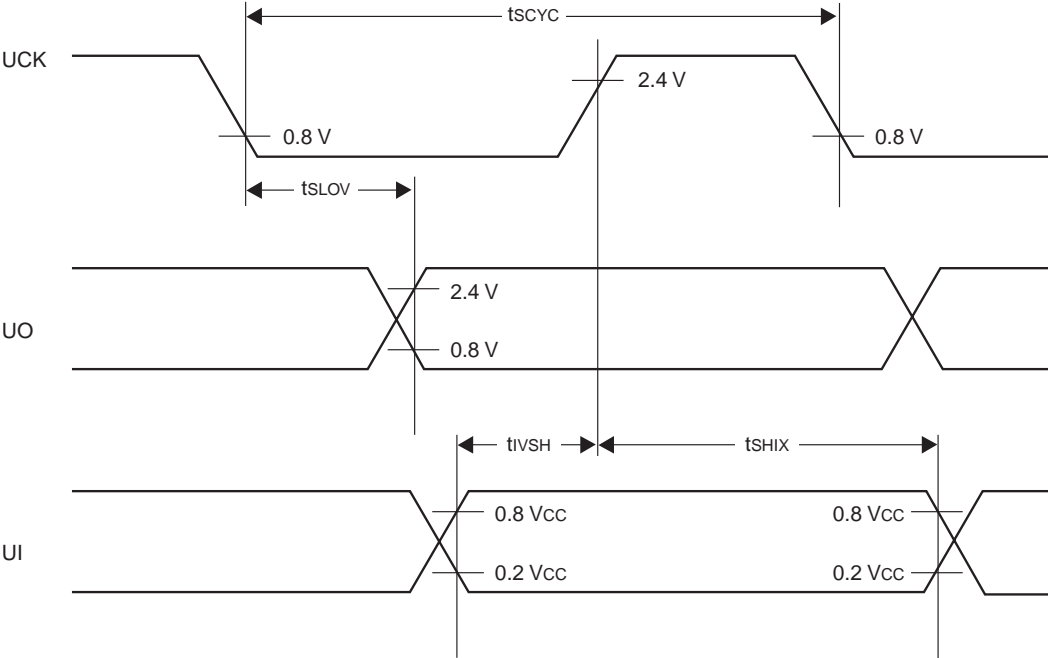
(4) UART1 to UART3

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

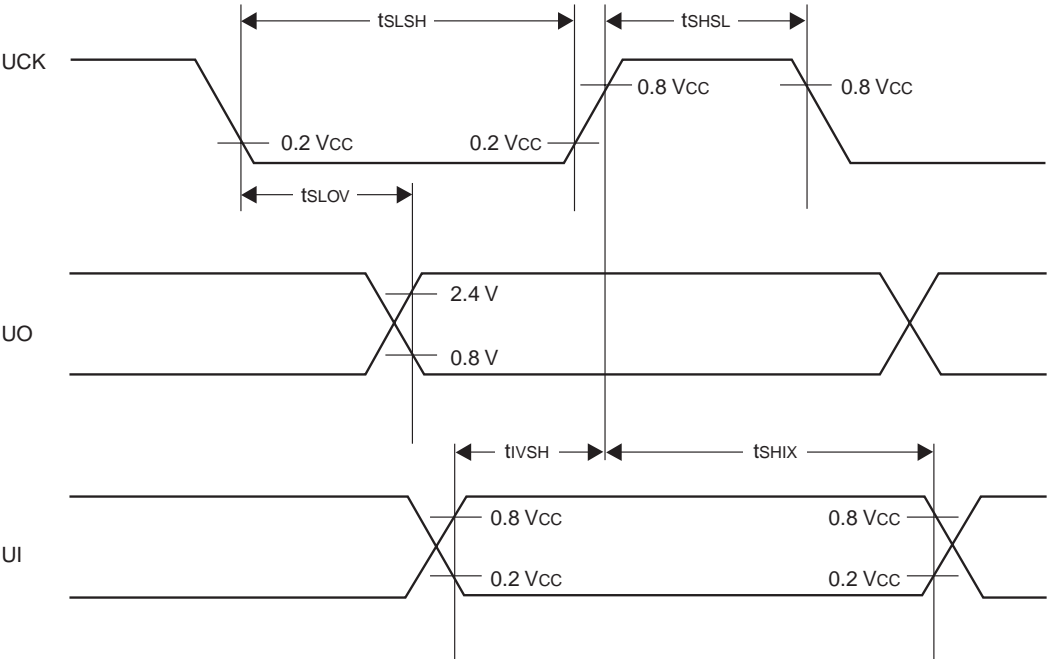
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of internal shift clock mode	$4 t_{CP}$	—	ns	
UCK ↓ → UO delay time	t_{SLOV}	UCK1 to UCK3, UO1 to UO3		-80	80	ns	
Valid UI → UCK ↑	t_{VSH}	UCK1 to UCK3, UI1 to UI3		100	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK1 to UCK3, UI1 to UI3		t_{CP}	—	ns	
Serial clock "H" pulse width	t_{SHSL}	UCK1 to UCK3	$C_L = 80\text{ pF} + 1\text{ TTL}$ for an output pin of external shift clock mode	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{SLSH}	UCK1 to UCK3		$4 t_{CP}$	—	ns	
UCK ↓ → UO delay time	t_{SLOV}	UCK1 to UCK3, UO1 to UO3		—	150	ns	
Valid UI → UCK ↑	t_{VSH}	UCK1 to UCK3, UI1 to UI3		60	—	ns	
UCK ↑ → valid UI hold time	t_{SHIX}	UCK1 to UCK3, UI1 to UI3		60	—	ns	

- Notes :
- These are AC ratings in the CLK synchronous mode.
 - C_L is the load capacitance value connected to pins while testing.
 - t_{CP} is the internal operating clock cycle time. Refer to "(1) Clock Timings" rating for t_{CP} .

• Internal shift clock mode



• Internal shift clock mode



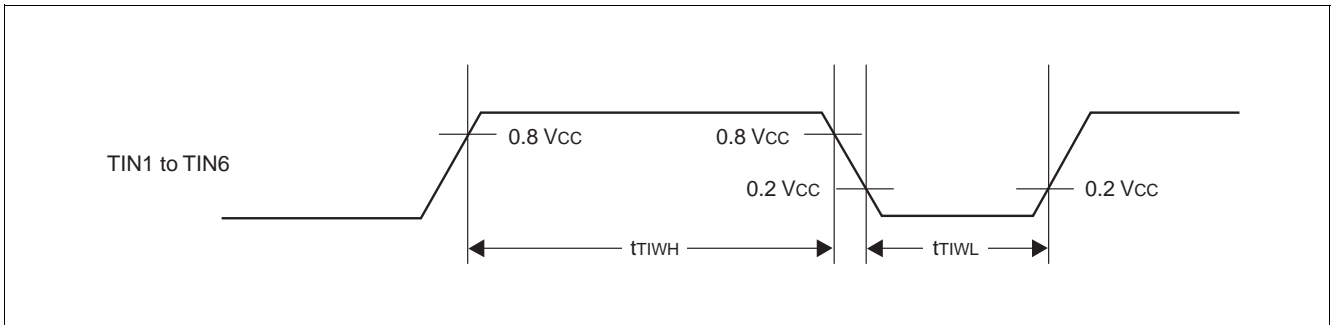
MB90378 Series

(5) Resources Input Timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Timer input pulse width	t_{TIWH} t_{TIWL}	TIN1 to TIN6	—	$4 t_{CP}$	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for t_{CP} .

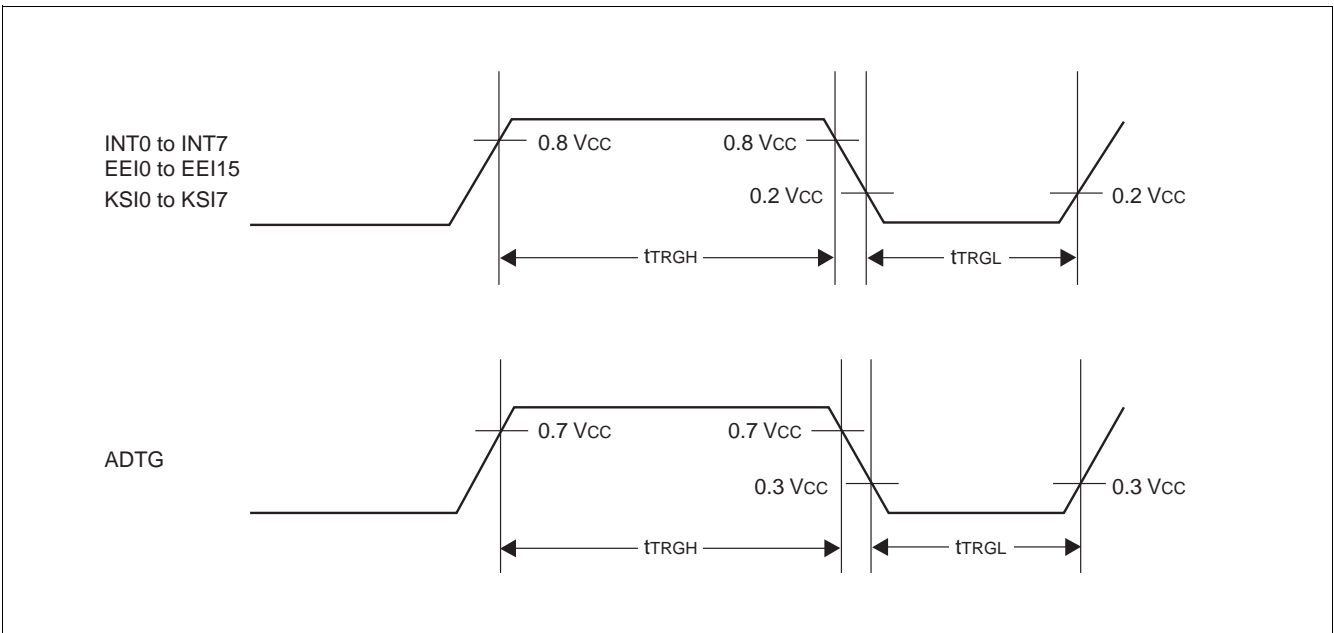


(6) Trigger Input Timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}	ADTG, INT0 to INT7, EEI0 to EEI15, KSI0 to KSI7	—	$5 t_{CP}$	—	ns	Normal operation
	t_{TRGL}			1	—	μs	Stop mode

Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for t_{CP} .



(7) I²C / Multi-address I²C Timing

(V_{CC} = 2.7 V to 3.6 V, AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Start condition output	t _{STA}	SCL, SDA	t _{CP} (m x n/2 - 1) - 20	t _{CP} (m x n/2 - 1) + 20	ns	Master mode
Stop condition output	t _{STO}	SCL, SDA	t _{CP} (m x n/2 + 3) - 20	t _{CP} (m x n/2 + 3) + 20	ns	Master mode
Start condition detect	t _{STA}	SCL, SDA	t _{CP} + 40	—	ns	
Stop condition detect	t _{STO}	SCL, SDA	t _{CP} + 40	—	ns	
Restart condition output	t _{STASU}	SCL, SDA	t _{CP} (m x n/2 + 3) - 20	t _{CP} (m x n/2 + 3) + 20	ns	Master mode
Restart condition detect	t _{STASU}	SCL, SDA	t _{CP} + 40	—	ns	
SCL output “L” width	t _{LOW}	SCL	t _{CP} x m x n/2 - 20	t _{CP} x m x n/2 + 20	ns	Master mode
SCL output “H” width	t _{HIGH}	SCL	t _{CP} (m x n/2 + 2) - 20	t _{CP} (m x n/2 + 2) + 20	ns	Master mode
SDA output delay	t _{DO}	SDA	t _{CP} x 3 - 20	t _{CP} x 3 + 20	ns	
SDA output setup time after interrupt	t _{DOSU}	SDA	t _{CP} x m x n/2 - 20	—	ns	*1
			t _{CP} x 4 - 20	—	ns	*2
SCL input “L” pulse	t _{LOW}	SCL	t _{CP} x 3 + 40	—	ns	
SCL input “H” pulse	t _{HIGH}	SCL	t _{CP} + 40	—	ns	
SDA output setup time	t _{SU}	SDA	40	—	ns	
SDA hold time	t _{HO}	SDA	0	—	ns	

- Notes :
- t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock Timings” rating for t_{CP}.
 - m is the setting bit of shift clock oscillation defined in the “ICCR register (CS4, CS3)” and “MCCR register (CS4, CS3)”. Please refer to the MB90378 series H/W manual for details.
 - n is the setting bit of shift clock oscillation defined in the “ICCR register (CS2 to CS0)” and “MCCR register (CS2 to CS0)”. Please refer to the MB90378 series H/W manual for details.
 - t_{DOSU} is shown in the interrupt time is longer than the “L” width of SCL.
 - SDA and SCL output value is specified on condition that the rise/fall time is “0 ns”.

*1 : At the stop condition or transferring of next byte.

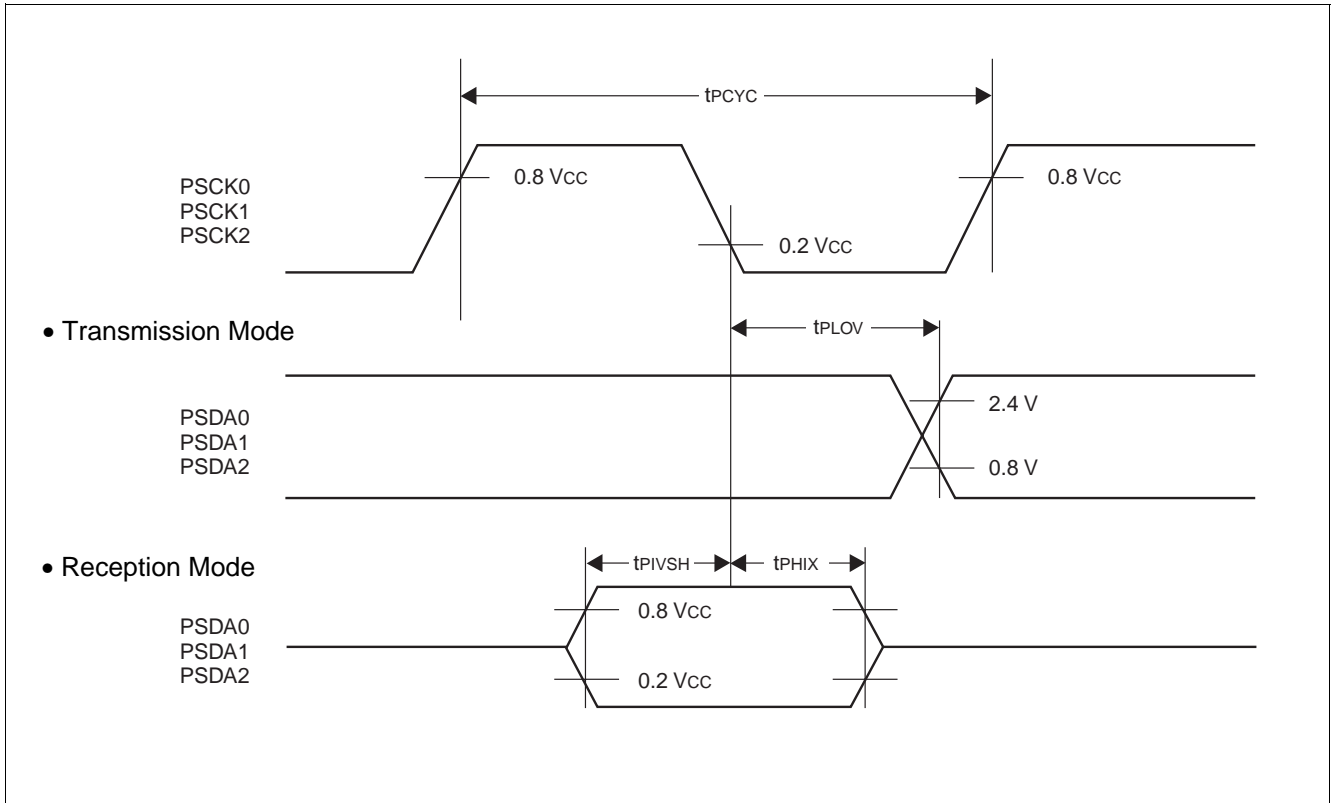
*2 : After setting register bit IBCRH : SCC at restart.

(8) PS/2 Interface Timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
PSCK clock cycle time	t_{PCYC}	PSCK0 to PSCK2, PSDA0 to PSDA2	—	$4 t_{CP}$	—	—	ns	
PSCK \downarrow → PSDA	t_{PLOV}	PSCK0 to PSCK2, PSDA0 to PSDA2	Transmission Mode	$2 t_{CP}$	—	—	ns	
Valid PSDA → PSCK \downarrow	t_{PIVSH}	PSCK0 to PSCK2, PSDA0 to PSDA2	Reception Mode	$1 t_{CP}$	—	—	ns	
PSCK \downarrow → valid PSDA hold time	t_{PHIX}	PSCK0 to PSCK2, PSDA0 to PSDA2		$1 t_{CP}$	—	—	ns	
PSCK clock "H" pulse width	t_{PHSL}	PSCK0 to PSCK2, PSDA0 to PSDA2	—	$2 t_{CP}$	—	—	ns	
PSCK clock "L" pulse width	t_{PLSH}	PSCK0 to PSCK2, PSDA0 to PSDA2		$2 t_{CP}$	—	—	ns	

Note : t_{CP} is the internal operating clock cycle time. Refer to "(1) Clock Timings" rating for t_{CP} .



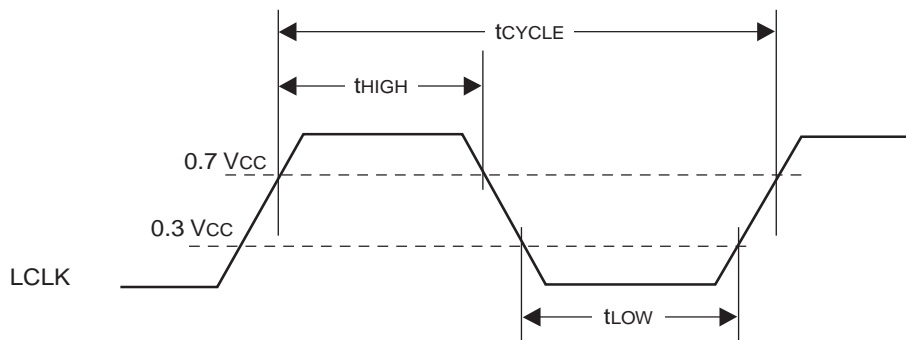
MB90378 Series

(9) LPC Timing

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+85\text{ }^\circ\text{C}$)

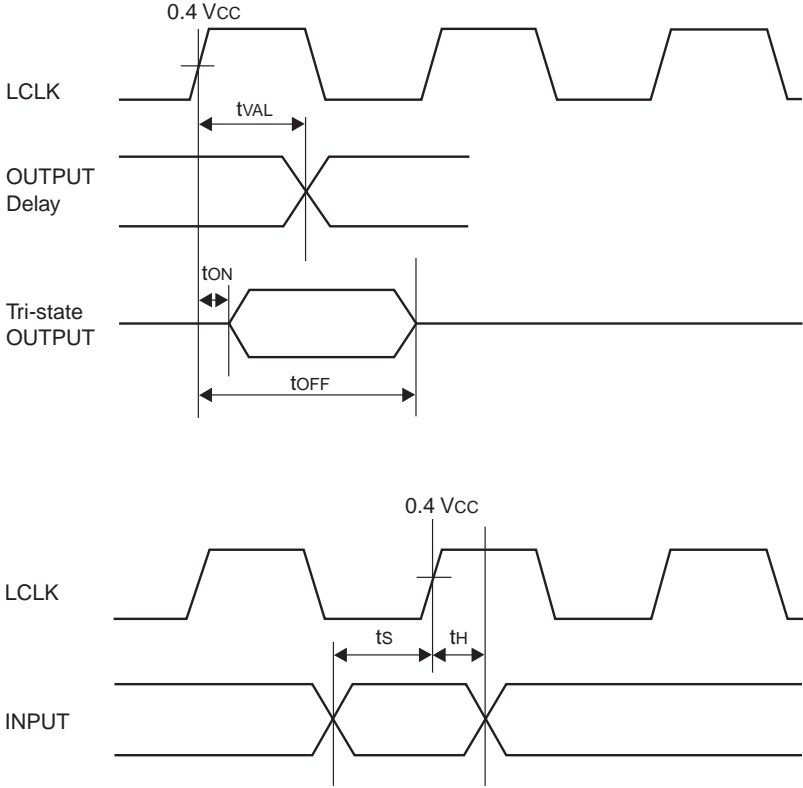
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
LCLK cycle time	t_{CYCLE}	—	—	30	—	—	ns	
LCLK high time	t_{HIGH}	—	—	12	—	—	ns	
LCLK low time	t_{LOW}	—	—	12	—	—	ns	

- LCLK AC timing



Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output valid delay	t_{VAL}	—	—	2	—	12	ns	
Float to active delay	t_{ON}	—	—	2	—	—	ns	
Active to float delay	t_{OFF}	—	—	—	—	28	ns	
Input setup time	t_s	—	—	7	—	—	ns	
Input hold time	t_H	—	—	0	—	—	ns	

• LAD, \overline{LFRAME} , GA20 AC timing



MB90378 Series

5. A/D Converter Electrical Characteristics

($2.7\text{ V} \leq \text{AVR} - \text{AV}_{\text{SS}}$, $\text{V}_{\text{CC}} = \text{AV}_{\text{CC}} = 2.7\text{ V}$ to 3.6 V , $\text{V}_{\text{SS}} = \text{AV}_{\text{SS}} = 0.0\text{ V}$, $\text{T}_{\text{A}} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Non-linear error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN11	$\text{AV}_{\text{SS}} - 1.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 0.5\text{ LSB}$	$\text{AV}_{\text{SS}} + 5.5\text{ LSB}$	mV	For MB90V378
					$\text{AV}_{\text{SS}} + 2.5\text{ LSB}$		For MB90F378
Full-scale transition voltage	V_{FST}	AN0 to AN11	$\text{AVR} - 3.5\text{ LSB}$	$\text{AVR} - 1.5\text{ LSB}$	$\text{AVR} + 0.5\text{ LSB}$	mV	
Conversion time	—	—	3.1	—	—	μs	Actual value is specified as a sum of values specified in ADCR0 : CT1, CT0 and ADCR0 : ST1, ST0. Be sure that the setting value is greater than the min value
Sampling period	—	—	2	—	—	μs	Actual value is specified in ADCR0 : ST1, ST0 bits. Be sure that the setting value is greater than the min value
Analog port input current	I_{AIN}	AN0 to AN11	—	0.1	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN11	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	$\text{AV}_{\text{SS}} + 2.7$	—	AV_{CC}	V	
Power supply current	I_{A}	AV_{CC}	—	1.4	6.4	mA	
	I_{AH}		—	—	5	μA	*
Reference voltage supply current	I_{R}	AVR	—	94	300	μA	
	I_{RH}		—	—	5	μA	*
Offset between channels	—	AN0 to AN11	—	—	4	LSB	

*: The current when the A/D converter is not operating or the CPU is in stop mode (for $\text{V}_{\text{CC}} = \text{AV}_{\text{CC}} = \text{AVR} = 3.0\text{ V}$).

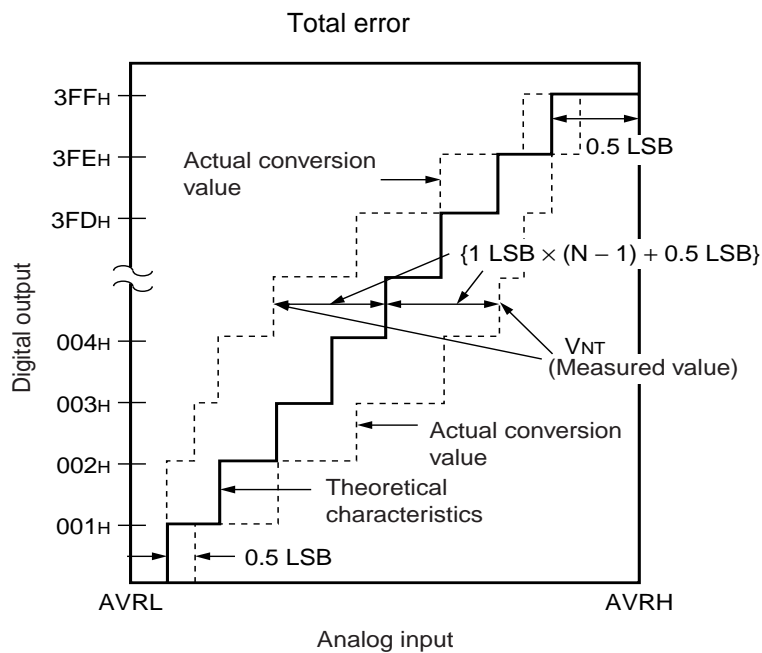
6. A/D Converter Glossary

Resolution : Analog changes that are identifiable with the A/D converter.

Linearity error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.

Differential linearity error : The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.

Total error : The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB (Theoretical value)} = \frac{AVR - AV_{SS}}{1024} \quad [\text{V}]$$

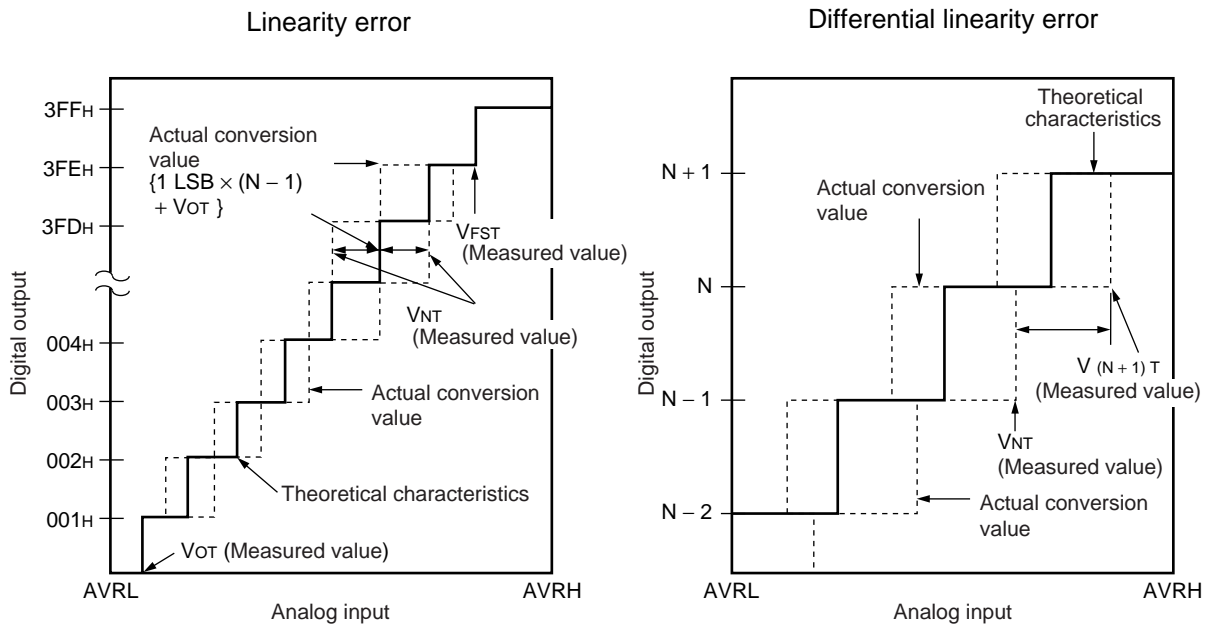
$$V_{OT} \text{ (Theoretical value)} = AV_{SS} + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} \text{ (Theoretical value)} = AVR - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : Voltage at a transition of digital output from (N - 1) to N

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

V_{OT} : Voltage at transition of digital output from "000H" to "001H"

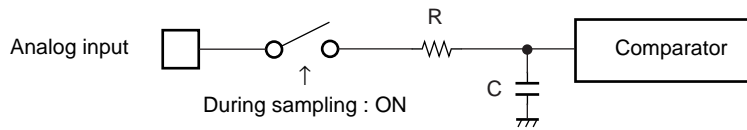
V_{FST} : Voltage at transition of digital output from "3FEH" to "3FFH"

7. Notes on Using A/D Converter

• About the external impedance of the analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sampling and hold capacitor is insufficient, adversely affecting A/D conversion precision.

• Analog input circuit model

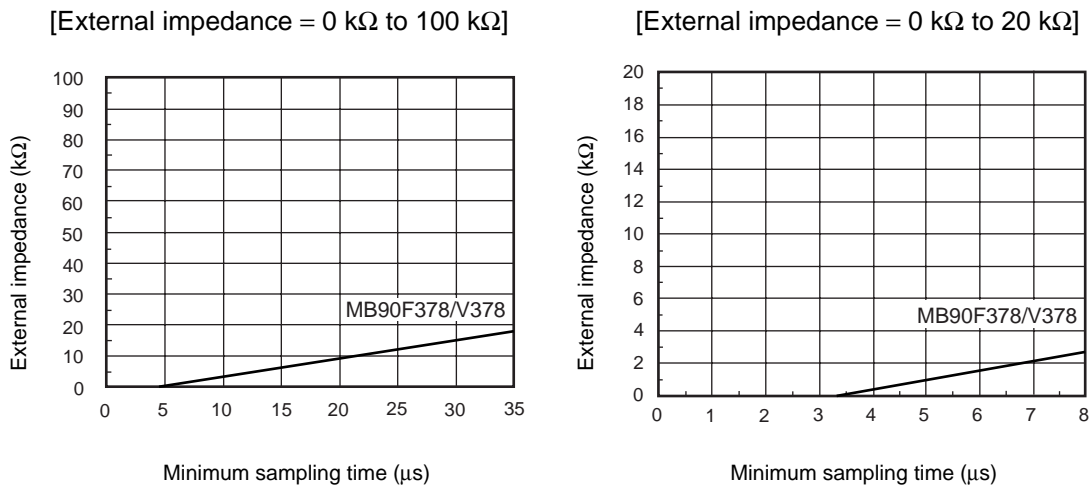


Note : The values are reference values.

MB90F378/V378 R C
 1.9 kΩ (Max) 25 pF (Max)

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

• The relationship between the external impedance and minimum sampling time



- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

• About errors

As $|AVR - AV_{SS}|$ becomes smaller, values of relative errors grow larger.

MB90378 Series

8. D/A Electrical Characteristics

($V_{CC} = AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+85\text{ °C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Differential linearity error	—	—		—	—	± 0.9	LSB	
Non-linearity error	—	—		—	—	± 1.5	LSB	
Conversion time	—	—		—	0.6	—	μs	*
Analog output impedance	—	—		2.0	2.9	3.8	$\text{k}\Omega$	
Power supply current	I_{DVR}	AV_{CC}		—	—	460	μA	
	I_{DVRs}	AV_{CC}	—	0.1	—	μA	D/A stops	

* : With load capacitance is 20 pF.

9. Serial IRQ Electrical Characteristics

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $AV_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ °C to }+85\text{ °C}$)

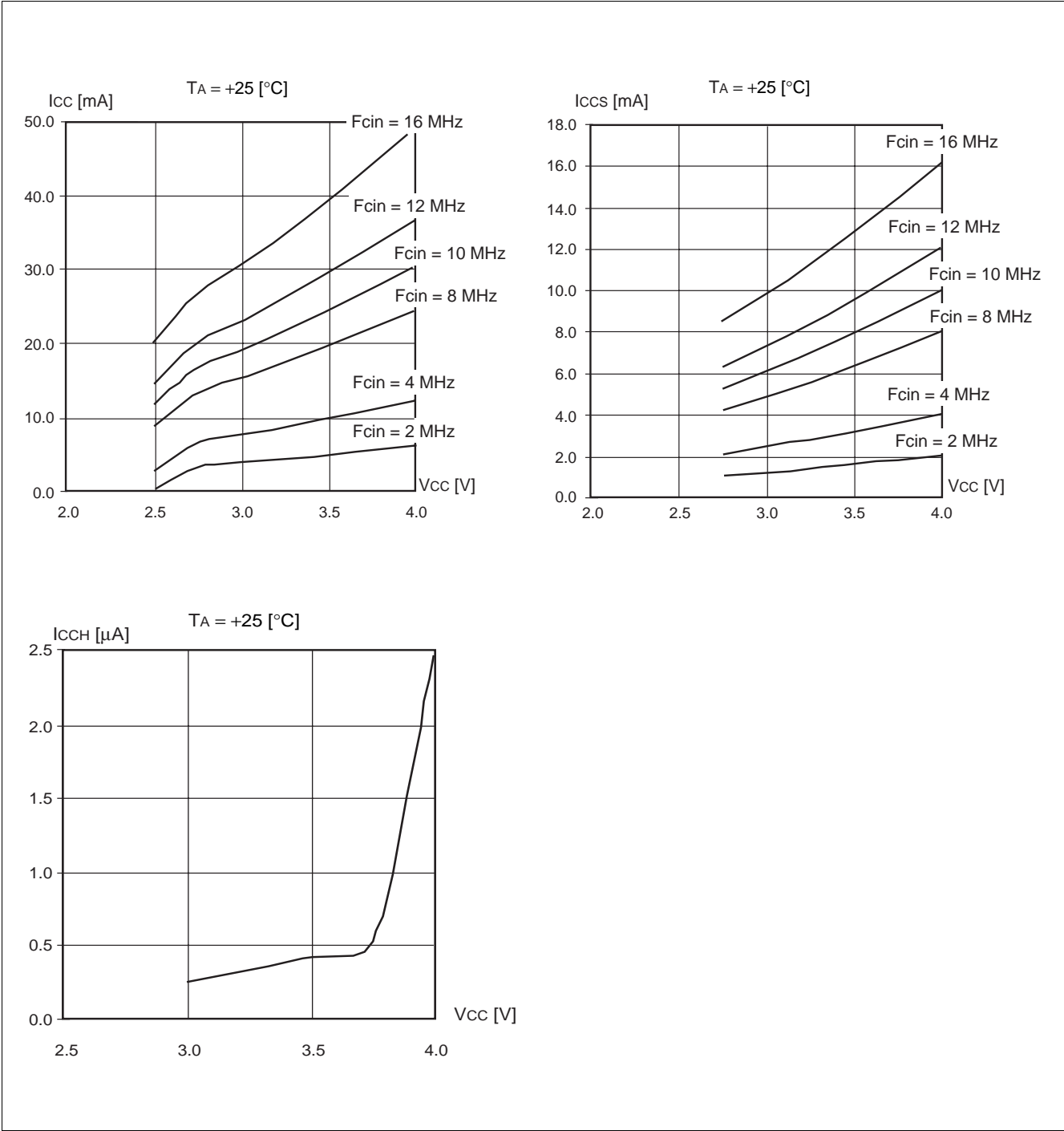
Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH}	—	—	$0.7 V_{CC}$	—	V_{CC}	V	
“L” level input voltage	V_{IL}	—	—	V_{SS}	—	$0.3 V_{CC}$	V	
“H” level output voltage	V_{OH}	—	—	$V_{CC} - 0.5$	—	—	V	
“L” level output voltage	V_{OL}	—	—	—	—	0.4	V	

10. Flash Memory Program/Erase Characteristics

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	$T_A = +25\text{ °C}$ $V_{CC} = 3.0\text{ V}$	—	0.2	0.5	s	Excludes 00H programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes 00H programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes 00H programming prior to erasure
Byte (8-bit width) programing time		—	32	3,600	μs	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	

■ EXAMPLE CHARACTERISTICS (MB90F378)

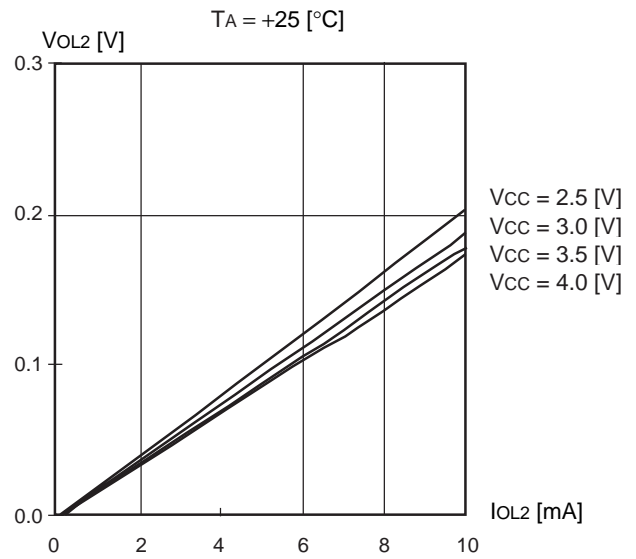
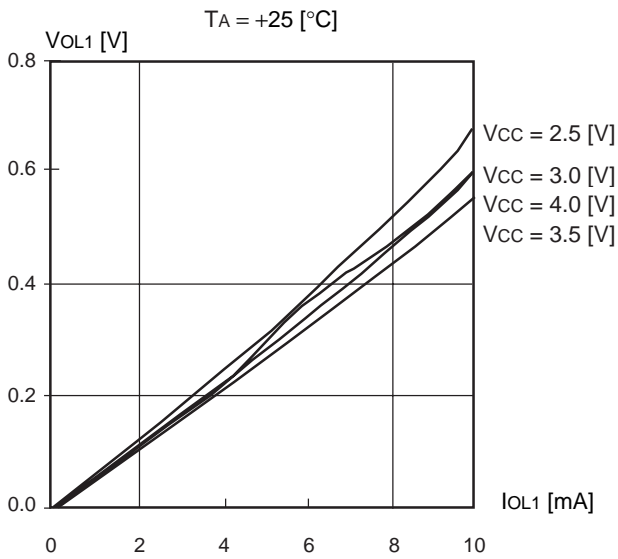
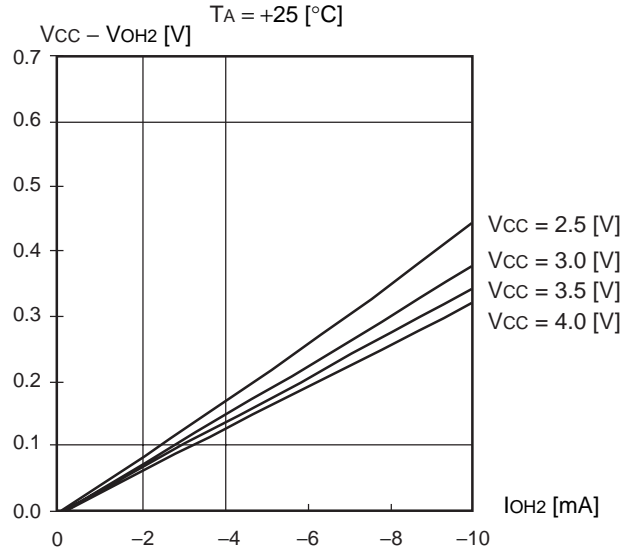
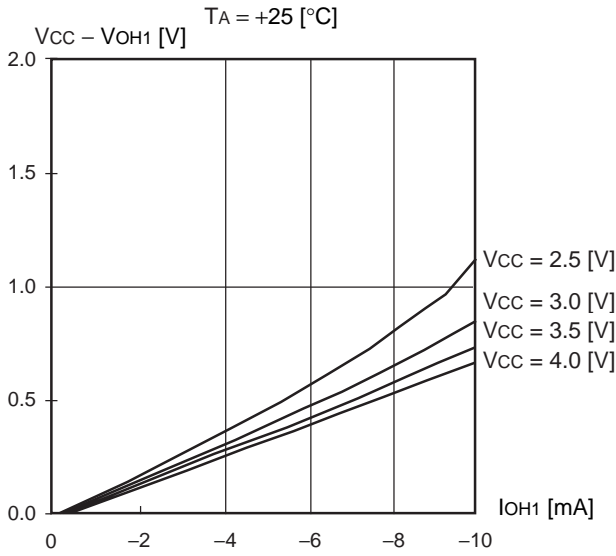
- Power Supply Current



(Continued)

MB90378 Series

(Continued)



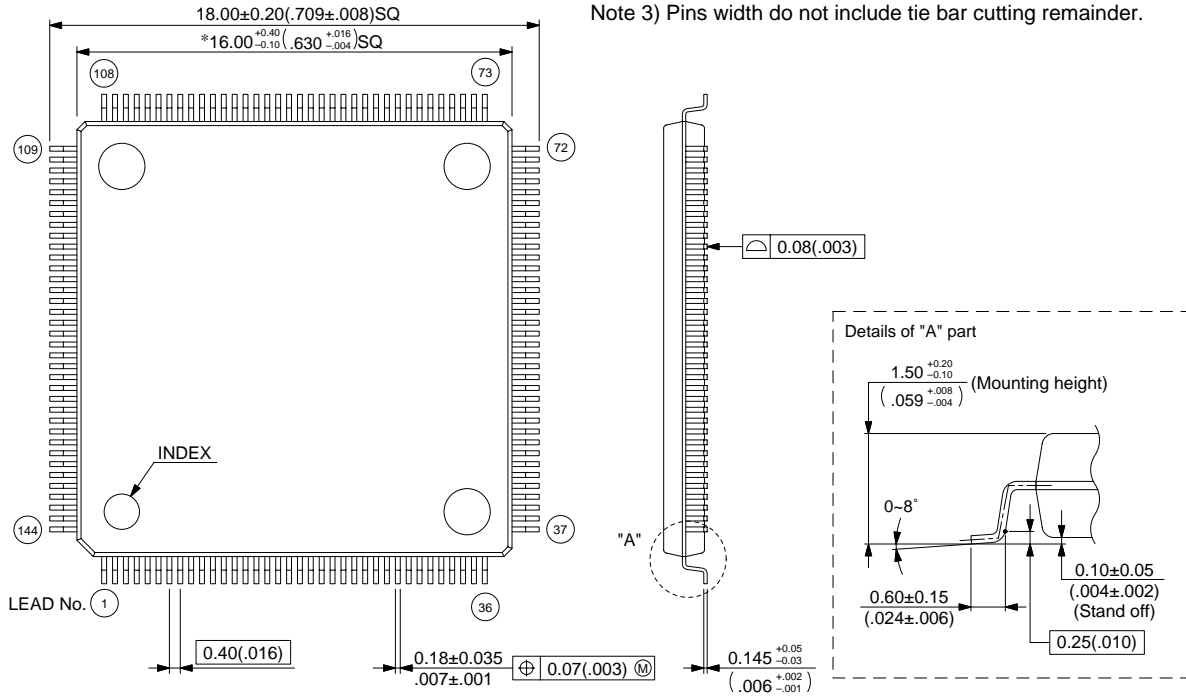
■ ORDERING INFORMATION

Part number	Package	Remarks
MB90F378PFF-GE1	144-pin Plastic LQFP (FPT-144P-M12)	

MB90378 Series

■ PACKAGE DIMENSION

144-pin plastic LQFP
(FPT-144P-M12)



Note 1) * : These dimensions include resin protrusion.
Resin protrusion is $+0.25(.010)$ Max(each side).
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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