March 2006

FAN7311
LCD Backlight Inverter Drive IC

Features

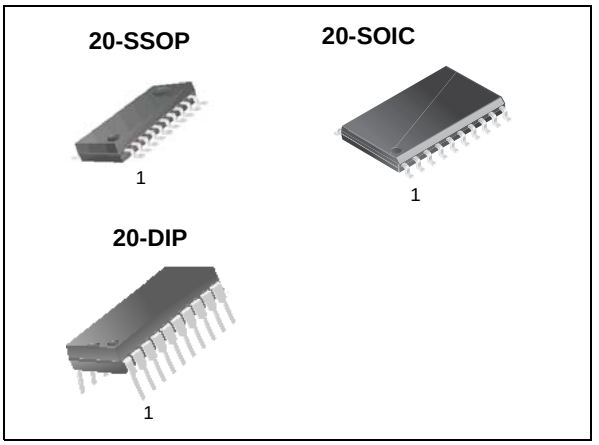
- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range : 5V to 25.5V
- Back Light Lamp Ballast and Soft Dimming
- Reduces Number of Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS Full-Bridge Topology
- Soft Start
- PWM Control at Fixed Frequency
- Analog and Burst Dimming Function
- Programmable Striking Frequency
- Open Lamp Protection
- Open Lamp Regulation
- 20-Pin SSOP/SOIC

Applications

- LCD TV
- LCD Monitor

Description

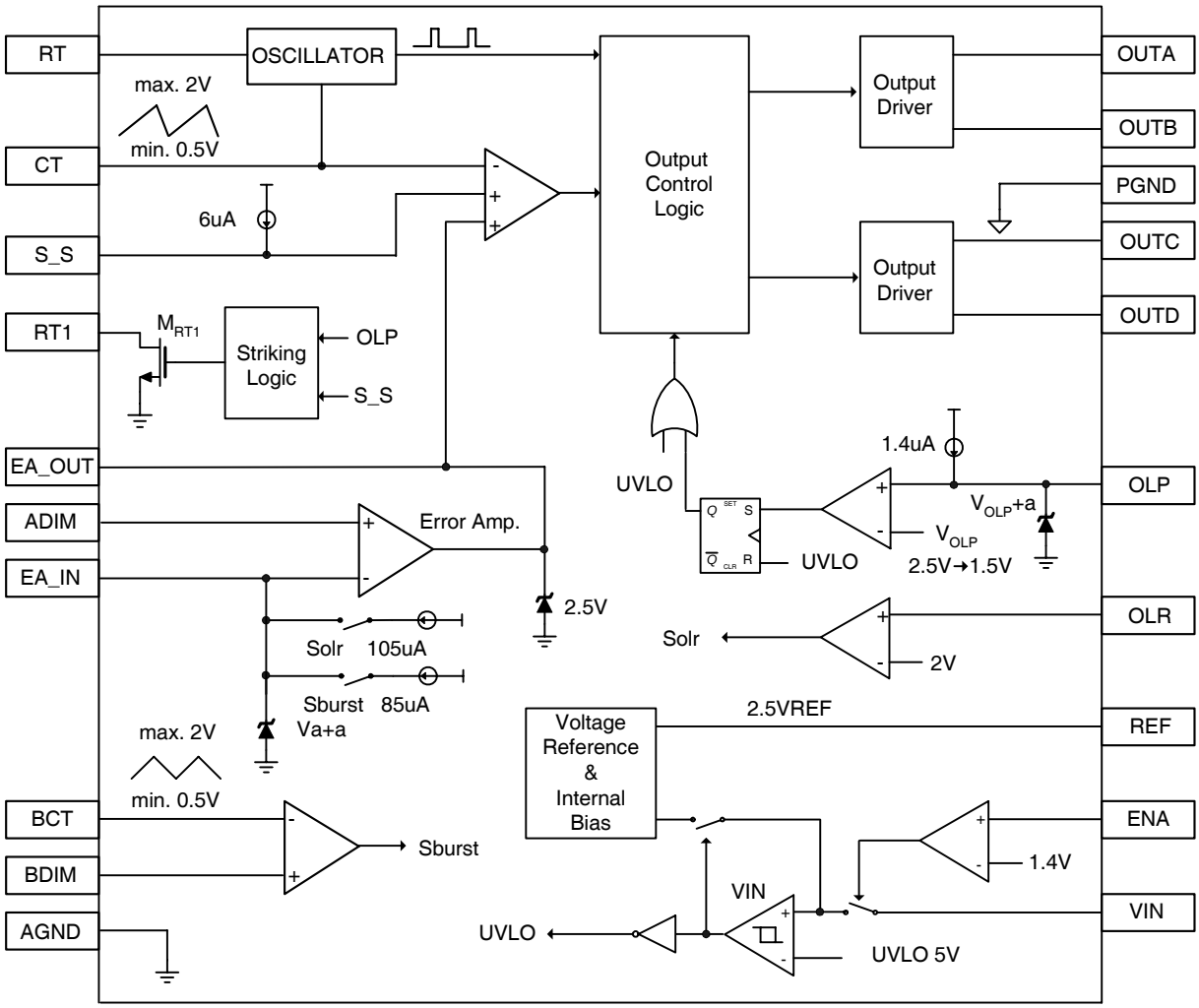
The FAN7311 provides all the control functions for a series parallel resonant converter as well as a pulse width modulation (PWM) controller to develop a supply voltage. Typical operating frequency range is between 30kHz and 250kHz, depending on the CCFL and the transformer's characteristics. The FAN7311 uses a new patent-pending phase-shift control.



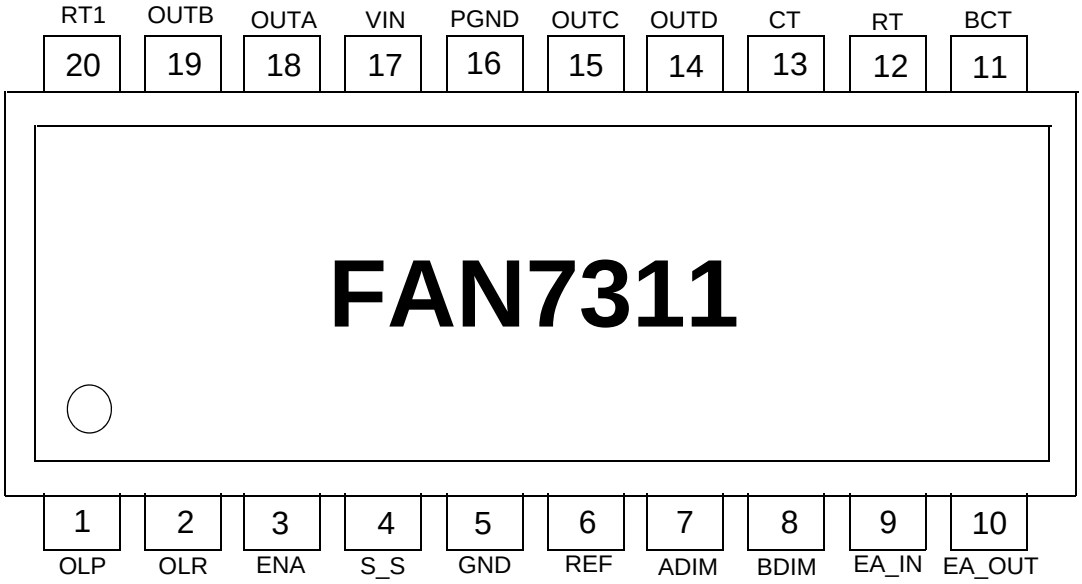
Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN7311G	20-SSOP	Y	-25°C ~ 85°C	Rail
FAN7311GX	20-SSOP	Y		Tape & Reel
FAN7311M	20-SOIC	Y		Rail
FAN7311MX	20-SOIC	Y		Tape & Reel
FAN7311N	20-DIP	Y		Rail

Internal Block Diagram



Pin Assignments



Pin Definitions

No	Name	Function/Description	No	Name	Function/Description
1	OLP	Open Lamp Protection	11	BCT	Burst Dimming Timing Capacitor
2	OLR	Open Lamp Regulation	12	RT	Timing Resistor
3	ENA	Enable Input	13	CT	Timing Capacitor
4	S_S	Soft Start	14	OUTD	NMOSFET Drive Output D
5	GND	Analog Ground	15	OUTC	PMOSFET Drive Output C
6	REF	2.5V Reference Voltage	16	PGND	Power Ground
7	ADIM	Analog Dimming Input	17	VIN	Supply Voltage
8	BDIM	Burst Dimming Input	18	OUTA	PMOSFET Drive Output A
9	EA_IN	Error Amplifier Input	19	OUTB	NMOSFET Drive Output B
10	EA_OUT	Error Amplifier Output	20	RT1	Striking Frequency Resistor

Absolute Maximum Ratings

For typical values T_A=25°C, Vcc=12V and for min/max values T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ Vcc ≤ 25.5V, unless otherwise specified.

Symbol	Characteristics	Value	Unit
V_{CC}	Supply Voltage	5 ~ 25.5	V
Topr	Operating Temperature Range	-25 ~ 85	°C
Tj	Junction Temperature	150	°C
Tstg	Storage Temperature Range	-65 ~ 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Air (Note1,2)		°C/W
	20-SSOP	112	
	20-SOIC	70	
	20-DIP	TBD(Note3)	
Pd	Power Dissipation		W
	20-SSOP	1.1	
	20-SOIC	1.8	
	20-DIP	TBD	

Note:

1. Thermal resistance test board
   Size: 76.2mm * 114.3mm * 1.6mm(1S0P)
   JEDEC standard: JESD51-2, JESD51-3
2. Assume no ambient airflow
3. To be decided

Electrical Characteristics

For typical values T_A=25°C, Vcc=12V and for min/max values T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ Vcc ≤ 25.5V, unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
REFERENCE SECTION (Recommend X7R Capacitor)						
ΔVref	Line Regulation	5 ≤ V_{CC} ≤ 25.5V	-	2	25	mV
V25	2.5V Regulation Voltage	-	2.45	2.5	2.55	V
	OSCILLATOR SECTION(MAIN)					
fosc	Oscillation Frequency	T_A = 25°C, Ct = 270pF Rt = 18k	110.4	115	119.6	kHz
		Ct = 270pF, Rt = 18k	108	115	122	
Vcth	CT High Voltage	-	-	2.0	-	V
Vctl	CT Low Voltage	-	-	0.5	-	V
OSCILLATOR SECTION(BURST)						
foscb	Oscillation Frequency	T_A = 25°C, Ctb = 10nF, Rt=18k	209.45	225	240.55	Hz
		Ctb = 10nF, Rt=18k	206.25	225	241.75	
Vbcth	BCT High Voltage	-	-	2	-	V
Vbctl	BCT Low Voltage	-	-	0.5	-	V
	ERROR AMP SECTION					
	Open Loop Gain	-	-	80	-	dB
	Unit Gain Bandwidth	-	-	1.5	-	MHz
Veh	Feedback Output High Voltage	EA_IN = 0V	2.0	2.27	2.54	V
Isin	Output Sink Current	EA_OUT = 1.5V	-	-	-1	mA
Isur	Output Source Current	EA_OUT = 1.5V	1	-	-	mA
Iolr	EA_IN Driving Current On OLR	-	75	105	135	uA
Iburst	EA_IN Driving Current On Burst Dimming	-	61	85	109	uA
Vfbh	Feedback High Voltage On Burst Dimming	R(EA_IN) = 60kΩ	Va+0.1	Va+0.4	Va+0.7	V
SOFT START SECTION						
I_{SS}	Soft Start Current	S_S=2V	4	6	8	uA
Vssh	Soft Start Clamping Voltage	-	-	5	-	V
	PROTECTION SECTION					
Volp0	Open Lamp Protection Voltage 0	Start at open lamp	2.2	2.5	2.8	V
Volp1	Open Lamp Protection Voltage 1	Normal -> open lamp	1.3	1.5	1.7	V
Volr	Open Lamp Regulation Voltage	-	1.75	2	2.25	V
Iolp	Open Lamp Protection Charging Current	-	0.7	1.4	2.1	uA
	UNDER VOLTAGE LOCK OUT SECTION					
Vth	Start Threshold Voltage	-	-	-	5	V
Ist	Start Up Current	V_{CC} = Vth-0.2	-	130	180	uA
Iop	Operating Supply Current	V_{CC} = 12V	-	1.5	4	mA
Isb	Stand-by Current	V_{CC} = 12V	-	200	370	uA
ON/OFF SECTION						
Von	On State Input Voltage	-	2	-	5	V
Voff	Off Stage Input Voltage	-	-	-	0.7	V

Electrical Characteristics (Continued)

For typical values T_A=25°C, Vcc=12V and for min/max values T_A is the operating ambient temperature range with -25°C ≤ T_A ≤ 85°C and 5V ≤ Vcc ≤ 25.5V, unless otherwise specified.

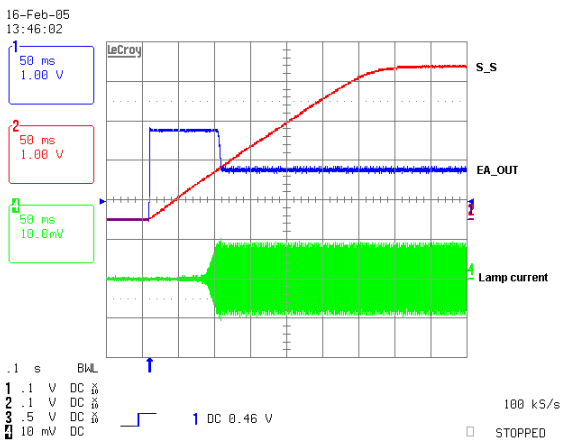
Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
OUTPUT SECTION						
Vpdhv	PMOS Gate High Voltage	V_{CC} = 12V	-	Vcc	-	V
Vphlv	PMOS Gate Low Voltage	V_{CC} = 12V	Vcc-10.5	Vcc-8.5	Vcc-6.5	V
Vndhv	NMOS Gate Drive Volgate	V_{CC} = 12V	6.5	8.5	10.5	V
Vndhv	NMOS Gate Drive Volgate	V_{CC} = 12V	-	0	-	V
Vpuv	PMOS Gate Voltage With UVLO Activated	V_{CC} = Vth-0.2	Vcc-0.3	-	-	V
Vnuv	NMOS Gate Voltage With UVLO Activated	V_{CC} = Vth-0.2	-	-	0.3	V
Tr	Rising Time	V_{CC} = 12V, Cload=2nF	-	200	500	ns
Tf	Falling Time	V_{CC} = 12V, Cload=2nF	-	200	500	ns
MAX./MIN OVERLAP						
	Min. Overlap between diagonal switches	fosc=100KHz	-	0	-	%
	Max. Overlap between diagonal switches	fosc=100KHz	-	100	-	%
DELAY TIME						
	PDR_A/NDR_B	Rt=18k	-	450	-	ns
	PDR_C/NDR_D	Rt=18k	-	450	-	ns

Function Description

UVLO: The under voltage lockout circuit guarantees stable operation of the IC's control circuit by stopping and starting it as a function of the Vin value. The UVLO circuit turns on the control circuit when Vin exceeds 5V. When Vin is lower than 5V, the IC's standby current is less than 200uA.

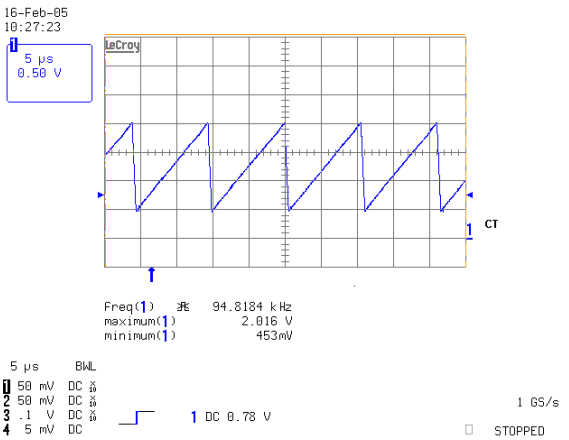
ENA: Applying voltage higher than 2V to the ENA pin enables the operation of the IC. Applying voltage lower than 0.7V to the ENA pin will disable the operation of the inverter.

Soft start: The soft start function requires that the S_S pin is connected through a capacitor to GND. A soft start circuit ensures a gradual increase in the input and output power. The capacitor connected to the S_S pin determines the rate at which the duty ratio rises. It is charged by a 6uA current source.



Main oscillator: The timing capacitors (CTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next, the timing capacitors start charging again and a new switching cycle begins. The main frequency can be programmed by adjusting the Rt and CT values. The main frequency can be calculated as shown below.

$$f_{op} = \frac{19}{32\ R_T\ C_T}$$

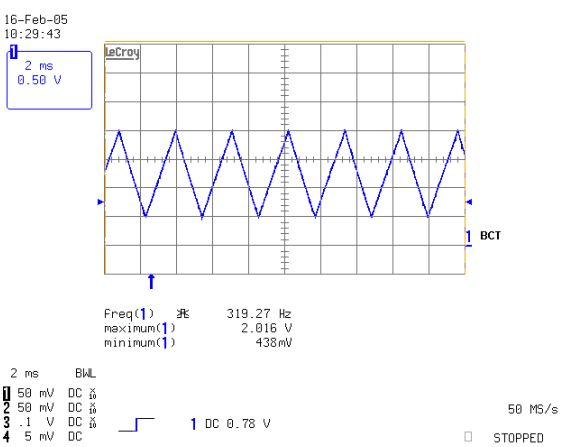


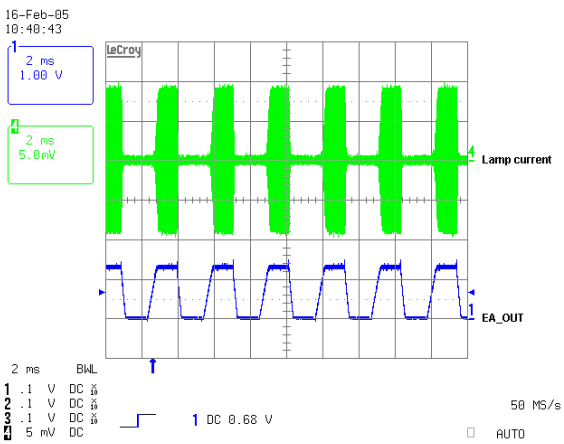
Burst oscillator & burst dimming: The timing capacitors (BCTs) are charged by the reference current source, which is formed by the timing resistor (RT). The timing resistor's voltage is regulated at 1.25V. The sawtooth waveform charges up to 2V. Once this voltage is reached, the capacitors begin discharging down to 0.5V. Next the timing capacitors start charging again and a new switching cycle begins. The burst dimming frequency can be programmed by adjusting the Rt and BCT values. The burst dimming frequency can be calculated as shown below.

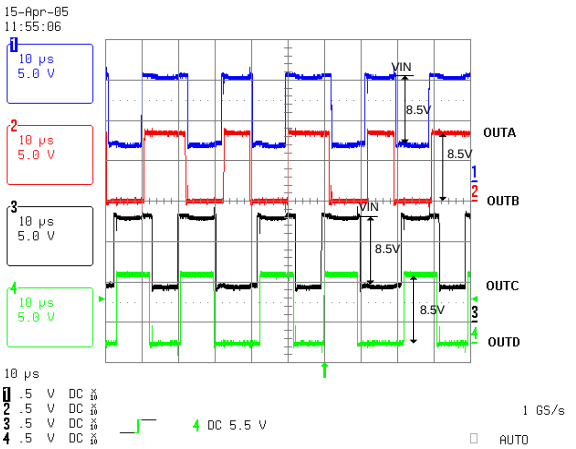
$$f_{burst} = \frac{3.75}{96\ R_T\ BC_T}$$

To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.

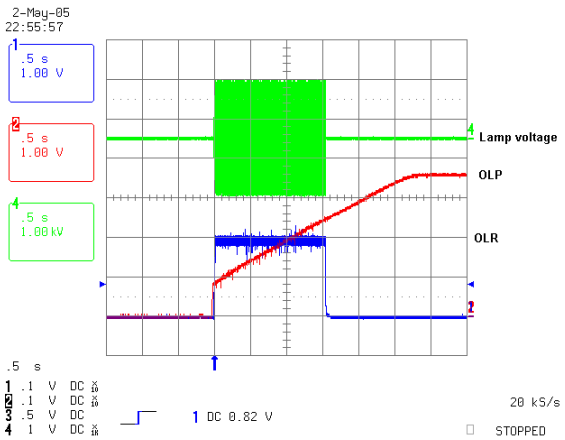
By comparing the input of BDIM pin with the 0.5~2V triangular wave of the burst oscillator the PWM pulses for burst dimming. The PWM pulse controls EA_OUT's voltage by summing 85uA into the EA_IN pin.







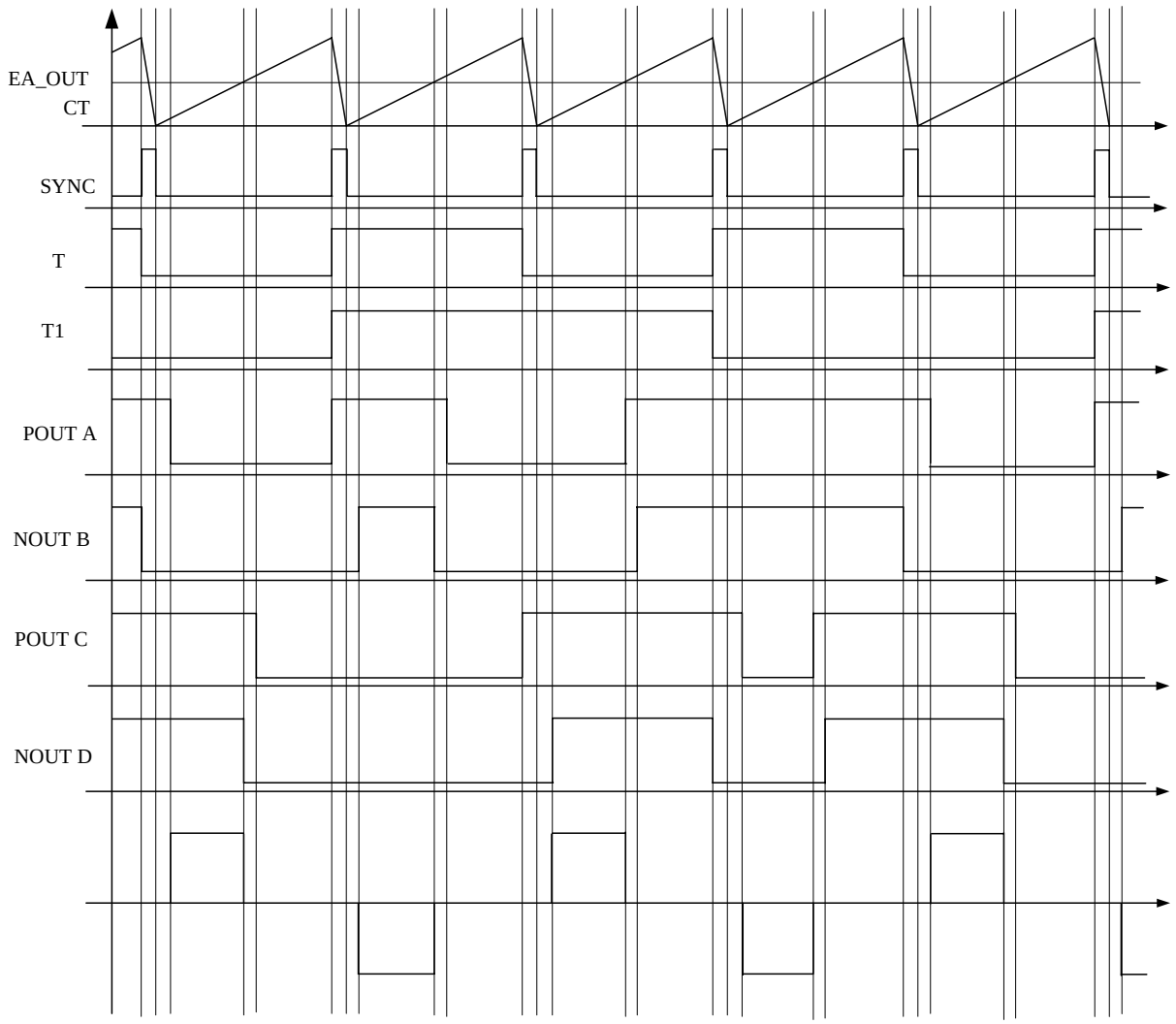
Open lamp regulation & open lamp protection: It is necessary to suspend power stage operation if an open lamp occurs, because the power stage has high gain. When a voltage higher than 2V is applied to the OLR pin, the part enters regulation mode and controls the EA_OUT voltage. This limits the lamp voltage by summing 105uA into the feedback node. At the same time, the OLP capacitor, connected to the OLP pin, is charged by the 1.4uA internal current source. Once it reaches 2.5V, the IC enters shut down where all the output is high.



Output Drives: The four output drives are designed so that switches A and B, C and D never turn on simultaneously. The OUTA-OUTB pair is intended to drive one half-bridge in the external power stage. The OUTC-OUTD pair will drive the other half-bridge.

Timing Diagram

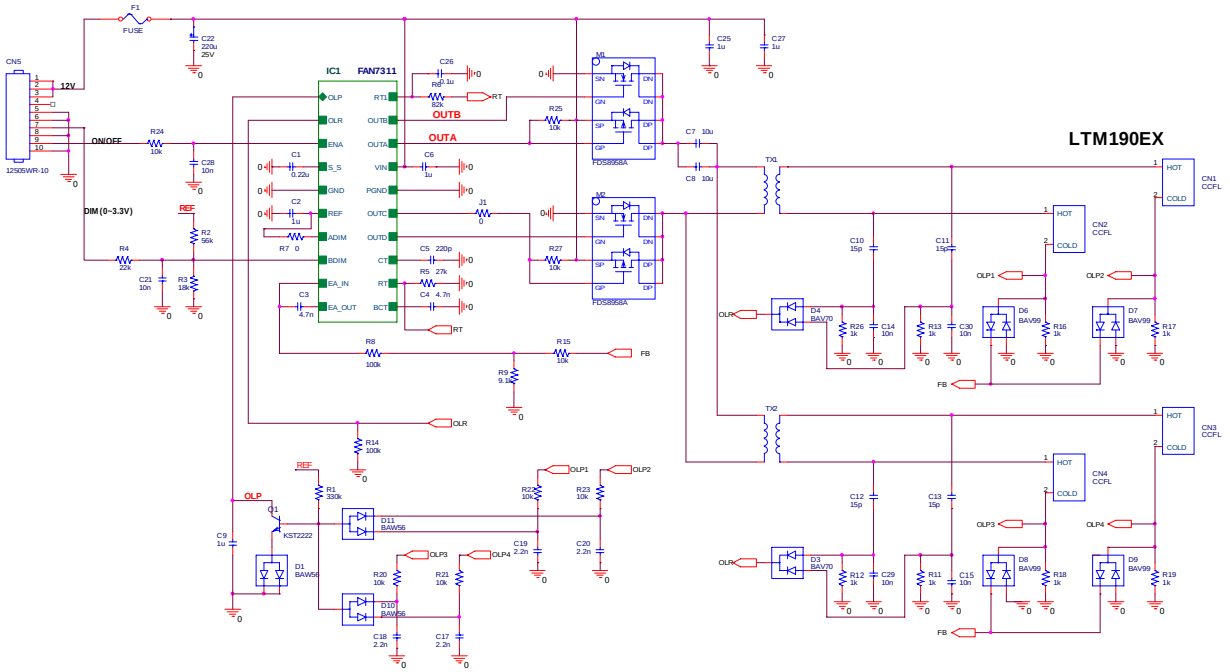
The FAN7311 uses the improved phase-shift control full-bridge to drive CCFL. As a result, the temperature difference between the left and the right leg is almost zero. The detail timing is shown below.



Typical Application Circuits

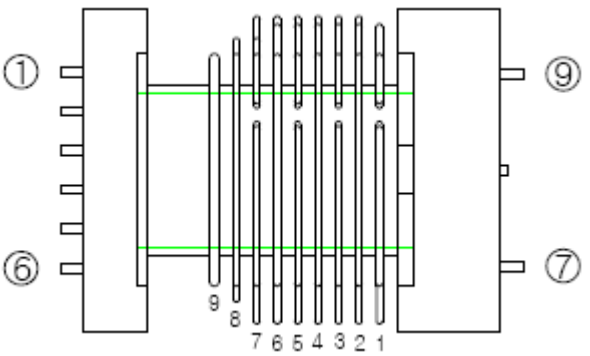
Application	Lamps	Input voltage
19 inch LCD Monitor	4	13V

1. Schematic



2. Transformer schematic Diagram

- Supported by Namyang electronics (http://www.namyangelec.co.kr)



3. Core & Bobbin

- Core : EFD2124
- Material : PL7
- Bobbin : EFE2124

4. Winding specification

Pin No.	Wire	Turns	Inductance	Leakage Inductance	Remarks
5 --> 2	1 UEW 0.45 ϕ	19	115 uH	21.5uH	1KHz, 1V
7 --> 9	1 UEW 0.04 ϕ	2300	1.5 H	280mH	1KHz, 1V

5. BOM of the application circuit

Part Ref.	Value	Description / Vendor	Part Ref.	Value	Description / Vendor
Fuse			C5	220p	50V 1608 J
F1	24V 3A	Fuse	C6	1u	50V 2012 K
Resistor (SMD)			C7	10u	16V 3216
R1	330K	1608 J	C8	10u	16V 3216
R2	56K	1608 F	C9	1u	16V 1608 K
R3	18K	1608 F	C10	15p	3KV 3216
R4	22K	1608 F	C11	15p	3KV 3216
R5	27K	1608 F	C12	15p	3KV 3216
R6	82K	1608 F	C13	15p	3KV 3216
R8	100K	1608 F	C14	10n	50V 1608 K
R9	9.1K	1608 F	C15	10n	50V 1608 K
R11	1K	1608 F	C17	2.2n	50V 1608 Z
R12	1K	1608 F	C18	2.2n	50V 1608 Z
R13	1K	1608 F	C19	2.2n	50V 1608 Z
R14	100K	1608 F	C20	2.2n	50V 1608 Z
R15	10K	1608 F	C21	10n	50V 1608 Z
R16	1K	1608 F	C25	1u	50V 2012 K
R17	1K	1608 F	C26	0.1u	16V 1608 K
R18	1K	1608 F	C27	1u	50V 2012 K
R19	1K	1608 F	C28	10n	50V 1608 Z
R20	10K	1608 J	C29	10n	50V 1608 K
R21	10K	1608 J	C30	10n	50V 1608 K
R22	10K	1608 J	**Diode / TR (SMD)**		
R23	10K	1608 J	D1	BAW56	Fairchildsemi
R24	10K	1608 J	D3	BAV70	Fairchildsemi
R25	10K	1608 J	D4	BAV70	Fairchildsemi
R26	1K	1608 F	D6	BAV99	Fairchildsemi
R27	10K	1608 J	D7	BAV99	Fairchildsemi
Capacitor (SMD)			D8	BAV99	Fairchildsemi
C1	0.22u	16V 1608 K	D9	BAV99	Fairchildsemi
C2	1u	50V 2012 K	D10	BAW56	Fairchildsemi
C3	4.7n	50V 1608 K	D11	BAW56	Fairchildsemi
C4	4.7n	50V 1608 K	Q1	KST2222	Fairchildsemi

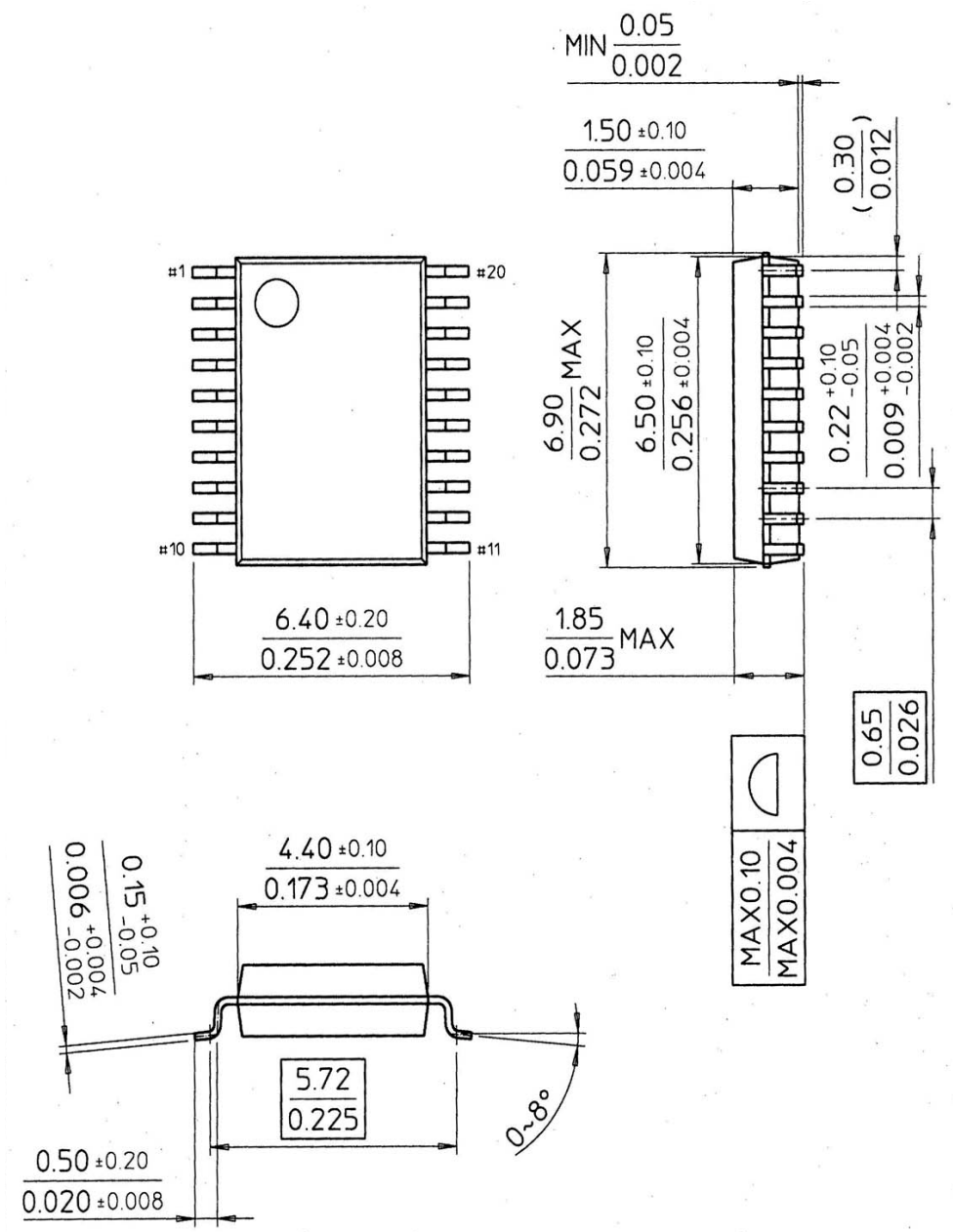
Part Ref.	Value	Description / Vendor	Part Ref.	Value	Description / Vendor
Electrolytic capacitor			**Wafer (SMD)**		
C22	220u	25V	CN1	35001WR-02A	
MOSFET (SMD)			CN2	35001WR-02A	
M1	FDS8958A	Fairchildsemi	CN3	35001WR-02A	
M2	FDS8958A	Fairchildsemi	CN4	35001WR-02A	
Transformer (SMD)			CN5	12505WR-10	
TX1	EFD2124	**Supported by Namyang electronics (http://www.namyangelec.co.kr)**			
TX2	EFD2124				

Mechanical Dimensions

Package

20-SSOP

Dimensions in millimeters

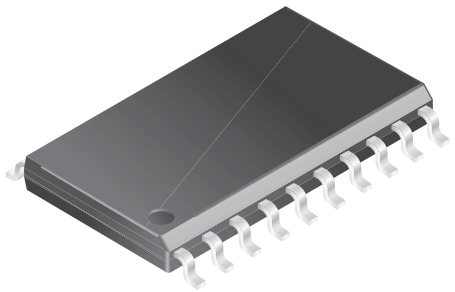


Mechanical Dimensions (Continued)

Package

20-SOIC

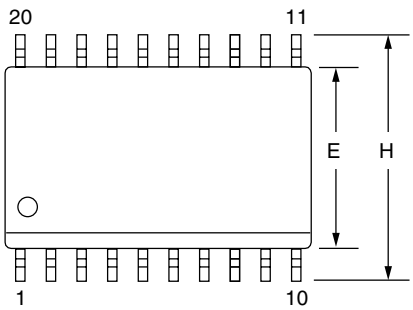
Dimensions in millimeters

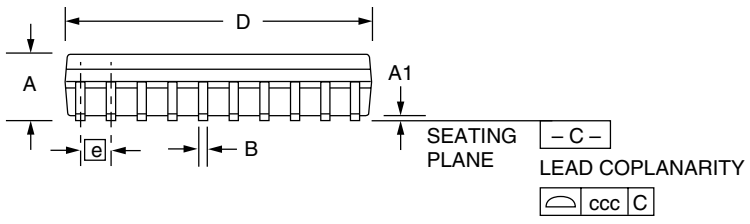


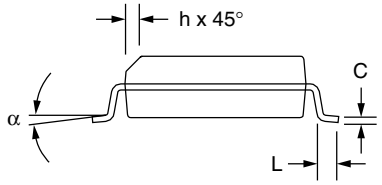
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



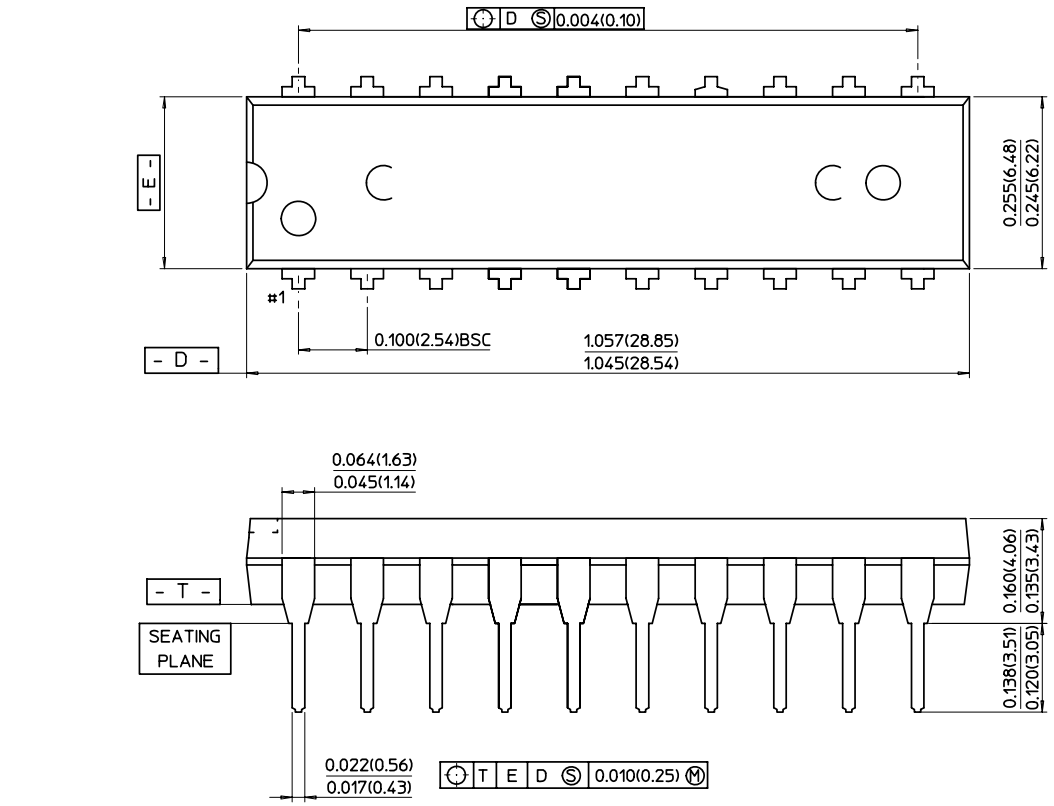


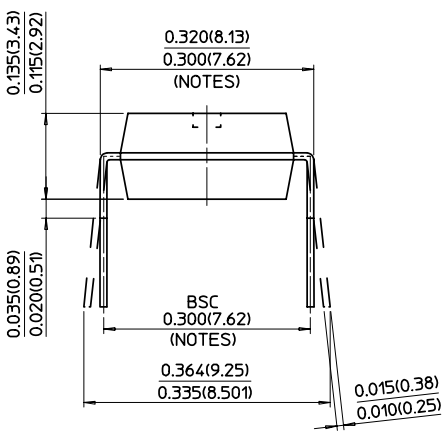


Mechanical Dimensions (Continued)

Package

20-DIP **Dimensions in millimeters**





NOTES

1. Controlling dimension : Inches. Metrics are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AE for standard Dual In Line(DIP) package 0.300 inch row sapcing (plastic) 20 leads (Issue B,7/85).
3. Dimension and tolerancing per ANSI Y14,5M-1982.
4. "T","D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #20 when viewed from the top.

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E²CMOS™	*i-Lo*™	OCX™	µSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
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Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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