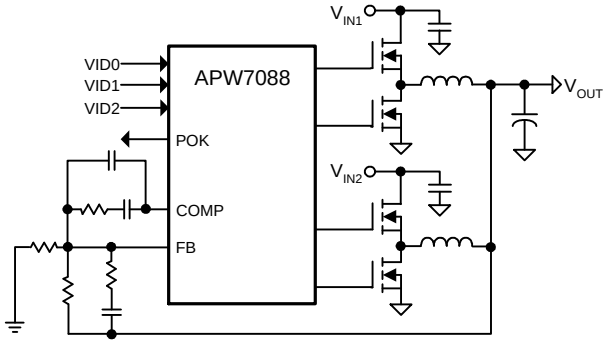
Two-Phase Buck PWM Controller with Integrated MOSFET Drivers

Features

- **Voltage-Mode Operation with Current Sharing**
  - **Adjustable Feedback Compensation**
  - **Fast Load Transient Response**
- **Operate with 8V~13.2V_{CC} Supply Voltage**
- **Programmable 3-Bit DAC Reference**
  - **±1.5% System Accuracy Over Temperature**
- **Support Single- and Two-Phase Operations**
- **5V Linear Regulator Output on 5VCC**
- **8~12V Gate Drivers with Internal Bootstrap Diode**
- **Lossless Inductor DCR Current Sensing**
- **Fixed 300kHz Operating Frequency Per Phase**
- **Power-OK Indicator Output**
  - **Regulated 1.5V on POK**
- **Adjustable Over-Current Protection (OCP)**
- **Accurate Load Line (DROOP) Programming**
- **Adjustable Soft-Start**
- **Over-Voltage Protection (OVP)**
- **Under-Voltage Protection (UVP)**
- **Over-Temperature Protection (OTP)**
- **QFN4x4 24-Lead Package (QFN4x4-24)**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Simplified Application Circuit



General Description

The APW7088, two-phase PWM control IC, provides a precision voltage regulation system for advanced graphic microprocessors in graphics card applications. The integration of power MOSFET drivers into the controller IC reduces the number of external parts for a cost and space saving power management solution.

The APW7088 uses a voltage-mode PWM architecture, operating with fixed-frequency, to provides excellent load transient response. The device uses the voltage across the DCRs of the inductors for current sensing. Load line voltage positioning (DROOP), channel-current balance and over-current protection are accomplished through continuous inductor DCR current sensing.

The MODE pin programs single- or two- phase operation. When IC operates in two-phase mode normally, it can transfer two-phase mode to single phase mode at liberty. Nevertheless, once operates in single-phase mode, the operation mode is latched. It is required to toggle SS or 5VCC pin to reset the IC. Such feature of the MODE pin makes the APW7088 ideally suitable for dual power input applications, such as PCIE interfaced graphic cards.

This control IC's protection features include a set of sophisticated over temperature, over-voltage, under-voltage, and over-current protections. Over-voltage results in the converter turning the lower MOSFETs on to clamp the rising output voltage and protects the microprocessor. The over-current protection level is set through external resistors. The device also provides a power-on-reset function and a programmable soft-start to prevent wrong operation and limit the input surge current during power-on or start-up.

The APW7088 is available in a QFN4x4-24 package.

Applications

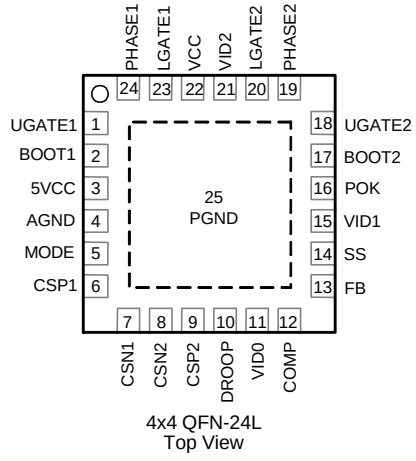
- **Graphics Card GPU Core Power Supply**
- **Motherboard Chipset or DDR SDRAM Core Power Supply**
- **On-Board High Power PWM Converter with Output Current up to 60A**

Ordering and Marking Information

APW7088 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN4x4-24 Operating Ambient Temperature Range E : -20 to 70°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7088 QA : APW7088 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020C for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



4x4 QFN-24L
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to AGND)	-0.3 ~ 15	V
$V_{BOOT1/2}$	BOOT1/2 Voltage (BOOT1/2 to PHASE1/2)	-0.3 ~ 15	V
	UGATE1/2 Voltage (UGATE1/2 to PHASE1/2) <200ns pulse width >200ns pulse width	 -5 ~ $V_{BOOT1/2}$+5 -0.3 ~ $V_{BOOT1/2}$+0.3	V
	LGATE1/2 Voltage (LGATE1/2 to PGND) <200ns pulse width >200ns pulse width	 -5 ~ V_{CC}+5 -0.3 ~ V_{CC}+0.3	V
	PHASE1/2 Voltage (PHASE1/2 to PGND) <200ns pulse width >200ns pulse width	 -10 ~ 30 -2 ~ 15	V
	BOOT1/2 to AGND Voltage <200ns pulse width >200ns pulse width	 -0.3 ~ 42 -0.3 ~ 30	V

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
V_{5VCC}	5VCC Supply Voltage (5VCC to AGND, $V_{5VCC} < V_{CC}$ +0.3V)	-0.3 ~ 7	V
V_{MODE}	MODE to AGND Voltage	-0.3 ~ 7	V
	Input Voltage (SS, FB, COMP, DROOP, CSP1/2, CSN1/2, VID0/1/2 to AGND)	-0.3 ~ V_{5VCC} +0.3	V
	PGND to AGND Voltage	-0.3 ~ +0.3	V
P_{DMAX}	Maximum Power Dissipation	Limited Internally	W
	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note 1: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Rating	Unit
θ_{JA}	Junction-to-Ambient Resistance (Note 2)	45	°C/W
θ_{JC}	Junction-to-Case Resistance (Note 3)	7	

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of QFN4x4-24 is soldered directly on the PCB.
Note 3: The case temperature is measured at the center of the exposed pad on the underside of the QFN4x4-24 package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	8 ~ 13.2	V
V_{5VCC}	5VCC Supply Voltage ($V_{5VCC} < V_{CC}$ +0.3V)	5 ± 5%	V
V_{OUT}	Converter Output Voltage	0.85 ~ 2.5	V
V_{IN1}	PWM 1 Converter Input Voltage	3.1 ~ 13.2	V
V_{IN2}	PWM 2 Converter Input Voltage	3.1 ~ 13.2	V
I_{OUT}	Converter Output Current	~ 60	A
T_A	Ambient Temperature	-20 ~ 70	°C
T_J	Junction Temperature	-20 ~ 125	°C
C_{VCC}	Linear Regulator Output Capacitor	0.8 ~ 15	µF
C_{5VCC}	5VCC Linear Regulator Output Capacitor	0.8 ~ 15	µF

Note 4 : Refer to the typical application circuits.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=1.2V and T_A= -20 ~ 70°C, unless otherwise specified. Typical values are at T_A=25°C. The V_{5VCC} is supplied by the internal regulator.

Symbol	Parameter	Test Conditions	APW7088			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{CC}	VCC Nominal Supply Current	UGATEx and LGATEx Open, FB forced above regulation point	-	5	10	mA
I_{SD}	VCC Shutdown Supply Current	SS=GND	-	5	-	mA

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=1.2V and T_A= -20 ~ 70°C, unless otherwise specified. Typical values are at T_A=25°C. The V_{5VCC} is supplied by the internal regulator.

Symbol	Parameter	Test Conditions	APW7088			Unit
			Min.	Typ.	Max.	
POWER-ON-RESET (POR) AND OPERATION PHASE SELECTION						
V_{5VCC_THR}	5VCC Rising Threshold Voltage		4.2	4.5	4.8	V
	5VCC POR Hysteresis		0.4	0.58	0.76	V
	MODE Rising Threshold Voltage	V_{MODE} Rising	0.77	0.8	0.83	V
I_{MODE}	MODE Pin Input Current		-100	-	+100	nA
5VCC LINEAR REGULATOR						
V_{REG_5VCC}	Output Voltage	I_O = 0A, V_{CC} =8V	4.75	5	5.25	V
	Line Regulation	I_O = 0A, V_{CC} = 8V ~ 13.2V	-20	-	20	mV
	Load Regulation	I_O = 3mA, V_{CC} > 8V	-200	-	200	mV
	Current-Limit	5VCC = GND	20	30	-	mA
REFERENCE VOLTAGE						
	Accuracy	T_A=25°C	-1	-	+1	%
		Over temperature	-1.5	-	+1.5	
I_{FB}	FB Pin Input Current		-100	-	+100	nA
	VID0/1/2 Logic High Threshold		1.2	-	-	V
	VID0/1/2 Logic Low Threshold		-	-	0.5	V
	VID0/1/2 Pull-high Current		-	1	-	µA
V_{POK}	POK Output Voltage		-	1.5	-	V
	POK Accuracy	I_O = 0~3mA, T_A=25°C	-2	-	+2	%
		I_O = 0~3mA, Over temperature	-3	-	+3	
	POK Current-Limit	POK = GND	4	8	15	mA
	POK Pull-Low Resistance	I_{POK} = 5mA	-	70	100	Ω
ERROR AMPLIFIER						
	DC Gain	R_L = 10kΩ to the ground	-	85	-	dB
	Gain-Bandwidth Product	C_L = 100pF, R_L = 10kΩ to the ground	-	20	-	MHz
	Slew Rate	C_L = 100pF, I_O = ±400µA	-	8	-	V/µs
	Upper Clamp Voltage	I_O = 1mA	2.7	3.0	-	V
	Lower Clamp Voltage	I_O = -1mA	-	-	0.1	V
	COMP Pull-Low Resistance	In fault or shutdown condition	-	2	-	kΩ
OSCILLATOR						
F_{OSC}	Oscillator Frequency		255	300	345	kHz
$\Delta V_{OSC1/2}$	Oscillator Sawtooth Amplitude		-	1.5	-	V
	Maximum Duty Cycle		85	88	-	%

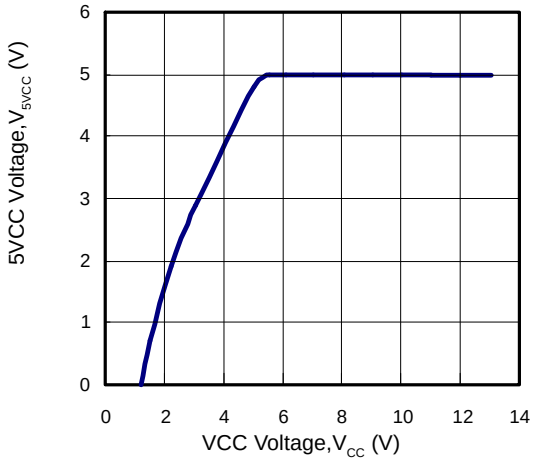
Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=1.2V and T_A= -20 ~ 70°C, unless otherwise specified. Typical values are at T_A=25°C. The V_{5VCC} is supplied by the internal regulator.

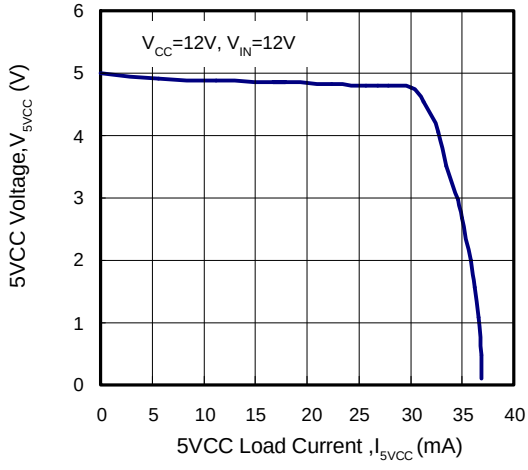
Symbol	Parameter	Test Conditions		APW7088			Unit
				Min.	Typ.	Max.	
MOSFET GATE DRIVERS							
	UGATE1/2 Source Current	V_{BOOT} = 12V, V_{UGATE}-V_{PHASE} = 2V		-	2.6	-	A
	UGATE1/2 Sink Current	V_{BOOT} = 12V, V_{UGATE}-V_{PHASE} = 2V		-	1	-	A
	LGATE1/2 Source Current	V_{CC} = 12V, V_{LGATE} = 2V		-	2.6	-	A
	LGATE1/2 Sink Current	V_{CC} =12V, V_{LGATE} = 2V		-	1.4	-	A
	UGATE1/2 Source Resistance	V_{BOOT} = 12V, 100mA Source Current		-	2.5	3.75	Ω
	UGATE1/2 Sink Resistance	V_{BOOT} = 12V, 100mA Sink Current		-	2	3	Ω
	LGATE1/2 Source Resistance	V_{CC} = 12V, 100mA Source Current		-	2	3	Ω
	LGATE1/2 Sink Resistance	V_{CC} = 12V, 100mA Sink Current		-	1.4	2.1	Ω
T_D	Dead-Time			-	30	-	ns
CURRENT SENSE AND DROOP FUNCTION							
I_{CSP}	CSP1/2 Pin Input Current			-100	-	+100	nA
I_{CSN}	CSN1/2 Maximum Output Current	$R_{CSN1/2}$ = 2kΩ,	Sourcing current	80	-	-	µA
			Sinking current	15	-	-	
	Current Sense Amplifier Bandwidth			-	3	-	MHz
	DROOP Output Current Accuracy	R_{DROOP} = 2kΩ, V_{DROOP} =0.005V		-	50	-	µA
	DROOP Accuracy	ΔV_{FB} = V_{DROOP}/20, V_{DROOP}=1V		-5	-	+5	mV
	Current Difference Between Channel1/2 and Average Current			-10	-	+10	%
SOFT-START AND ENABLE							
I_{SS}	Soft-Start Current Source	Flowing out of SS pin		8	10	12	µA
	Soft-Start Complete Threshold			-	3.2	-	V
	SS Pull-low Resistance			-	10	18	kΩ
POWER OK AND PROTECTIONS							
	Over-Current Trip Level	I_{CS1} + I_{CS2}		110	120	140	µA
V_{UV}	FB Under-Voltage Threshold	~ 2µs noise filter, V_{FB} falling, Percentage of V_R at Error Amplifier		40	50	60	%
V_{POK_L}	POK Lower Threshold			-	87.5	-	%
V_{OV}, V_{POK_H}	FB Over-Voltage Threshold and POK Upper Threshold	~ 2µs noise filter, V_{FB} rising Percentage of V_R at Error Amplifier		115	125	135	%
	FB Over-Voltage Hysteresis			-	60	80	mV
T_{OTR}	Over-Temperature Trip Level	T_J rising		-	150	-	°C
	Over-Temperature Hysteresis			-	50	-	°C

Typical Operating Characteristics

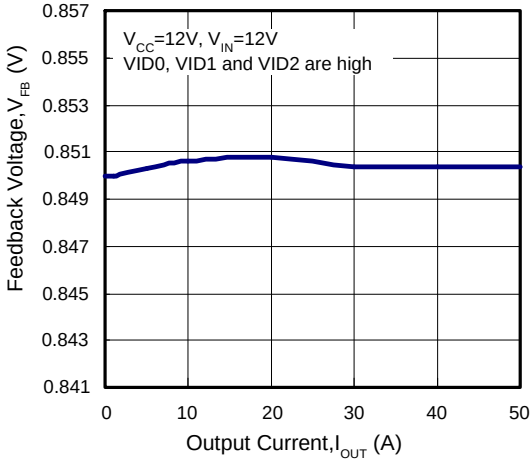
5VCC Line Regulation



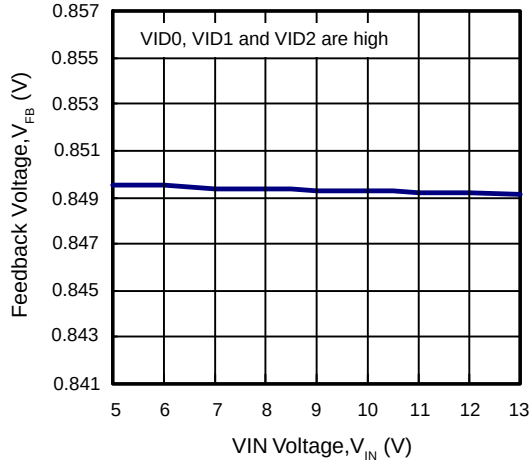
5VCC Load Regulation



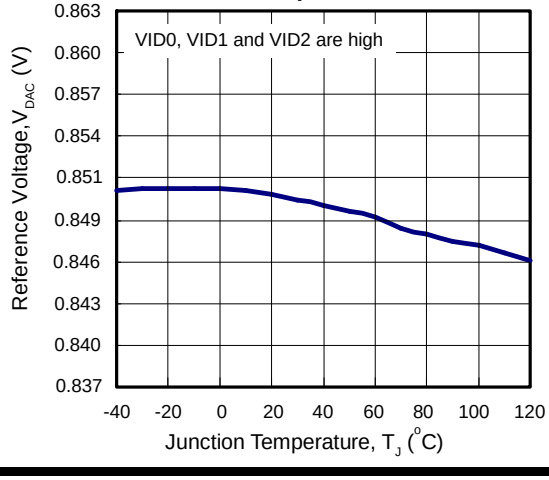
Output Voltage Load Regulation



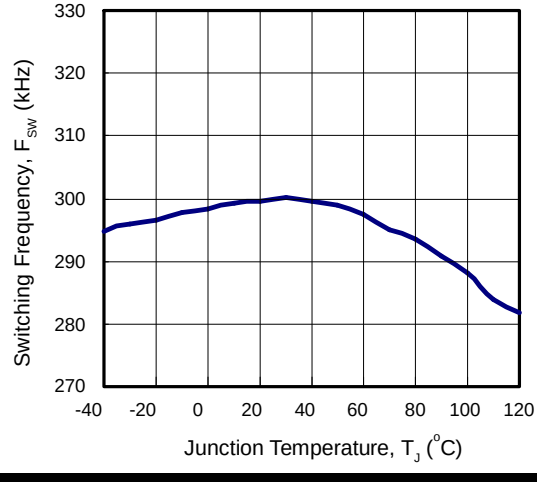
Output Voltage Line Regulation



Reference Voltage Accuracy Over Temperature

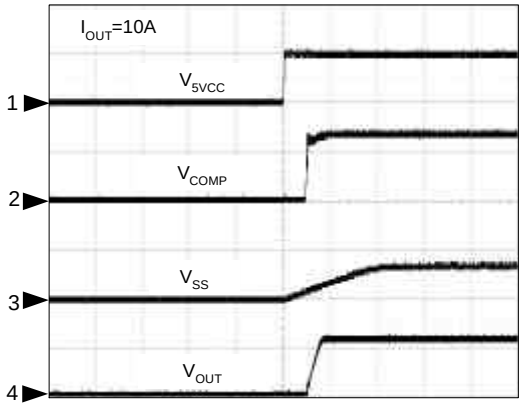


Switching Frequency Over Temperature



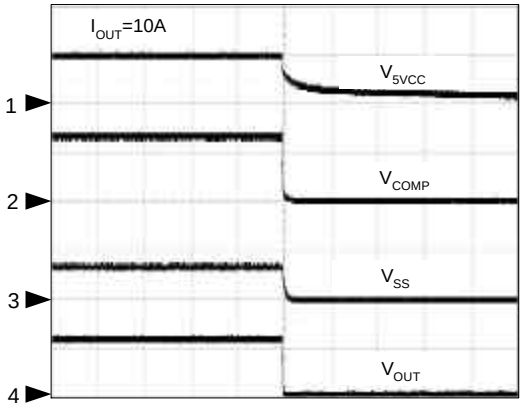
Operating Waveforms

Power On



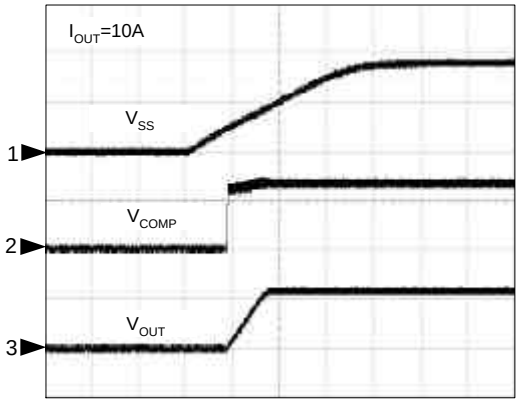
CH1: V_{5VCC} (5V/div)
CH2: V_{COMP} (1V/div)
CH3: V_{SS} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 5ms/div

Power Off



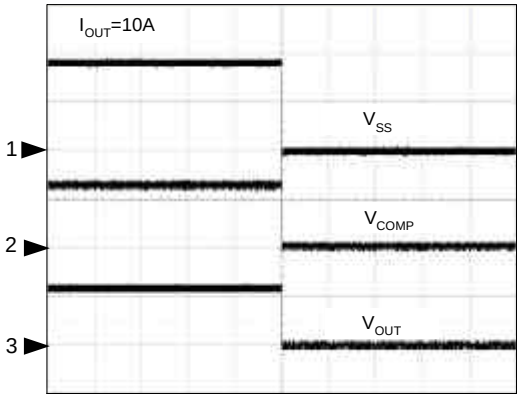
CH1: V_{5VCC} (5V/div)
CH2: V_{COMP} (1V/div)
CH3: V_{SS} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 5ms/div

Enable by SS Pin



CH1: V_{SS} (2V/div)
CH2: V_{COMP} (1V/div)
CH3: V_{OUT} (1V/div)
Time: 10ms/div

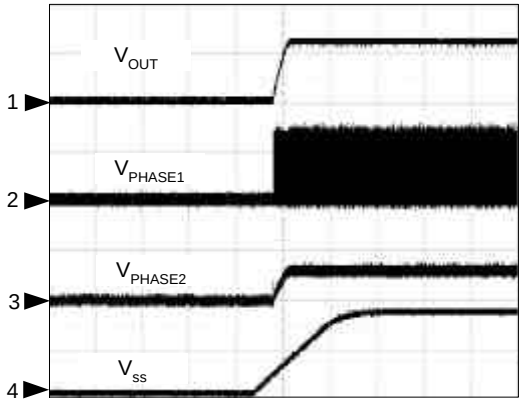
Shutdown by SS Pin



CH1: V_{SS} (2V/div)
CH2: V_{COMP} (1V/div)
CH3: V_{OUT} (1V/div)
Time: 10ms/div

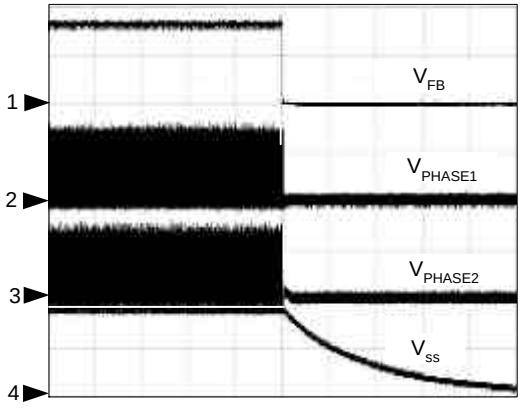
Operating Waveforms (Cont.)

Power On Without V_{IN2} Voltage



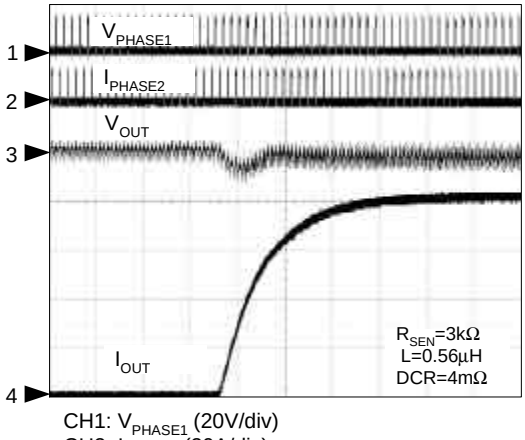
CH1: V_{OUT} (1V/div)
CH2: V_{PHASE1} (10V/div)
CH3: V_{PHASE2} (2V/div)
CH4: V_{SS} (2V/div)
Time: 5ms/div

Under-Voltage Protection (UVP)



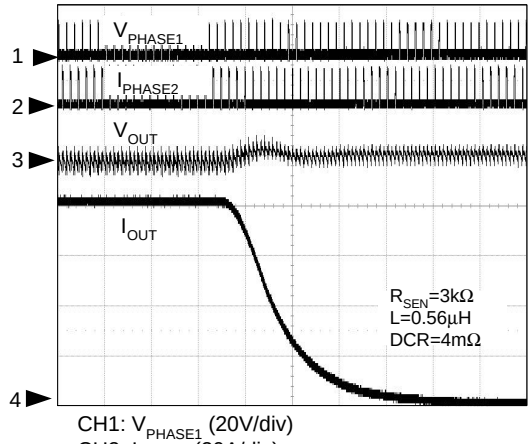
CH1: V_{FB} (500mV/div)
CH2: V_{PHASE1} (10V/div)
CH3: V_{PHASE2} (10V/div)
CH4: V_{SS} (2V/div)
Time: 500µs/div

Load Transient , 0A==>40A



CH1: V_{PHASE1} (20V/div)
CH2: I_{PHASE2} (20A/div)
CH3: V_{OUT} (AC, 200mV/div)
CH4: I_{OUT} (10A/div)
Time: 20µs/div

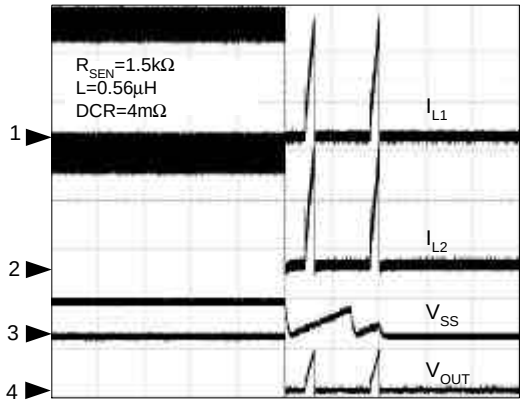
Load Transient , 40A==>0A



CH1: V_{PHASE1} (20V/div)
CH2: I_{PHASE2}(20A/div)
CH3: V_{OUT} (AC, 200mV/div)
CH4: I_{OUT} (10A/div)
Time: 20µs/div

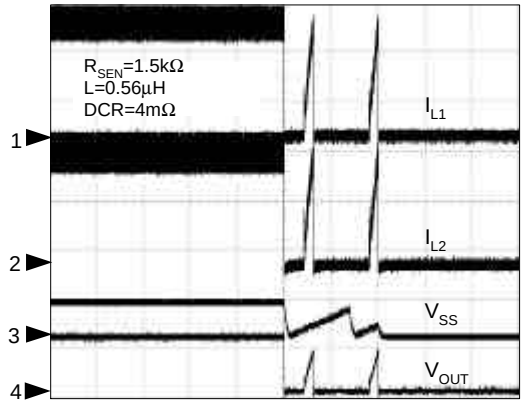
Operating Waveforms (Cont.)

OCP at Slow Slew I_{OUT}



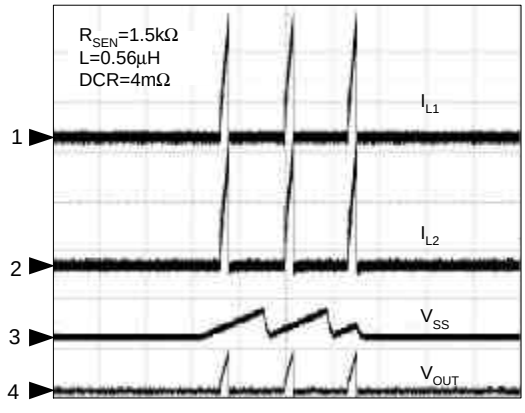
CH1: I_{L1} (10A/div)
CH2: I_{L2} (10A/div)
CH3: V_{SS} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 5ms/div

Short-Circuit Test After Power On



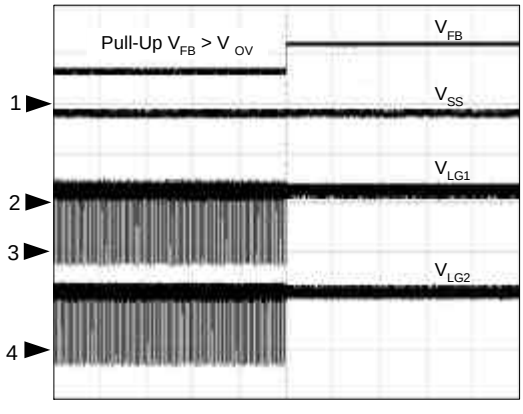
CH1: I_{L1} (10A/div)
CH2: I_{L2} (10A/div)
CH3: V_{SS} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 5ms/div

Short-Circuit Test Before Power On



CH1: I_{L1} (10A/div)
CH2: I_{L2} (10A/div)
CH3: V_{SS} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 5ms/div

OVP After Power On



CH1: V_{FB} (500mV/div)
CH2: V_{SS} (2V/div)
CH3: V_{LG1} (10V/div)
CH4: V_{LG2} (10V/div)
Time: 100µs/div

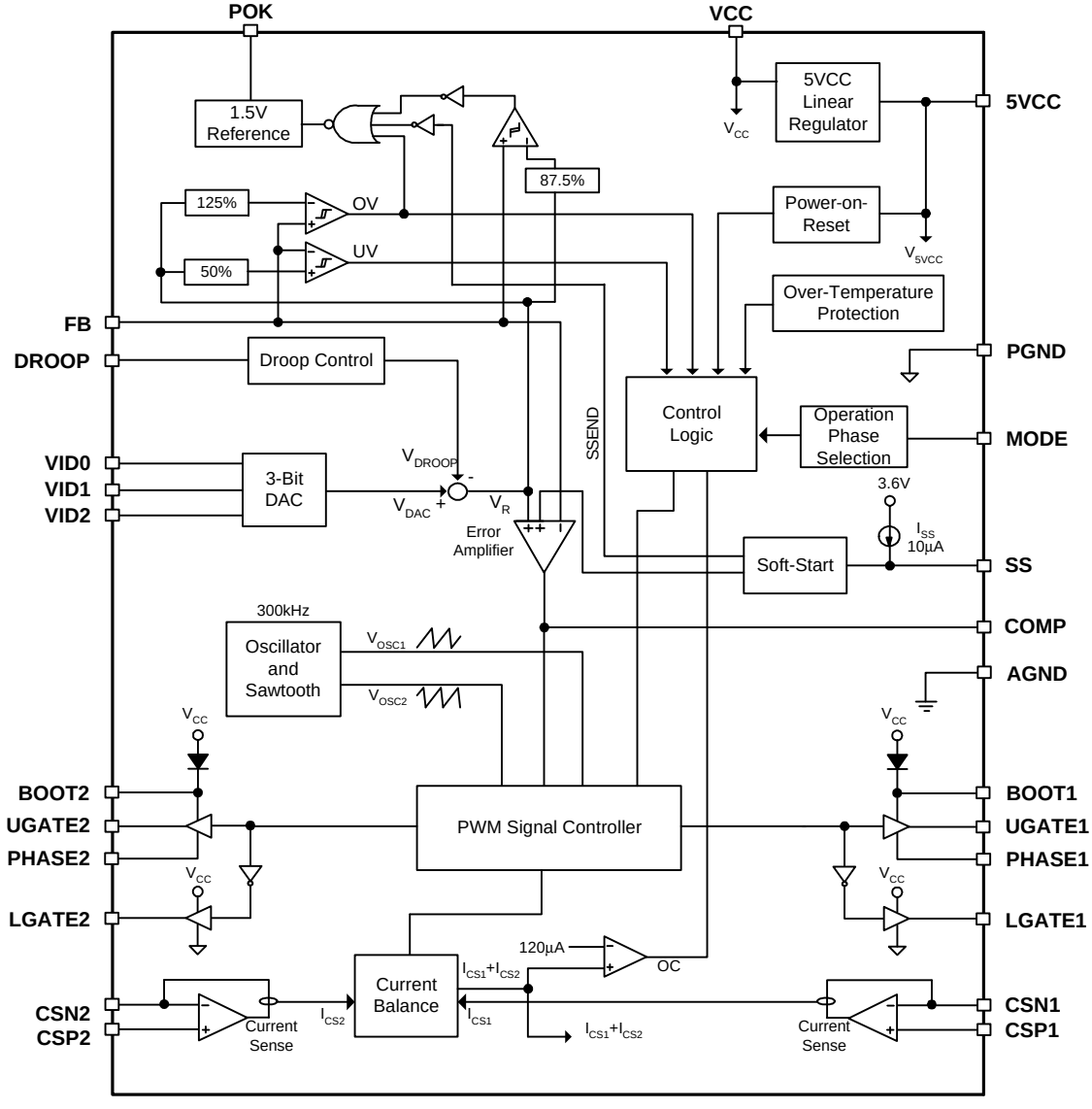
Pin Description

PIN	NAME	FUNCTION
1	UGATE1	High-side Gate Driver Output for channel 1. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
2	BOOT1	Bootstrap Supply for the floating high-side gate driver of channel 1. Connect the Bootstrap capacitor between the BOOT1 pin and the PHASE1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for C_{BOOT} ranged from 0.1µF to 1µF. Ensure that C_{BOOT} is placed near the IC.
3	5VCC	Internal Regulator Output. This is the output pin of the linear regulator, which is converting power from VCC and provides output current up to 20 mA minimums for internal bias and external usage.
4	AGND	Signal Ground for the IC. All voltage levels are measured with respect to this pin. Tie this pin to ground island/plane through the lowest impedance connection available.
5	MODE	Operation Phase Selection Input. Pulling this pin lower than 0.64V sets two-phase operation with both channels enabled. Pulling this pin higher than 0.8V sets single-phase operation with the channel 2 disabled. Once operating in single-phase mode, the operation mode is latched. It is required to toggle SS or 5VCC pin to reset the IC.
6	CSP1	Positive Input of current sensing Amplifier for channel 1. This pin combined with CSN1 senses the inductor current through an RC network.
7	CSN1	Negative Input of current sensing amplifier for channel 1. This pin combined with CSP1 senses the inductor current through an RC network.
8	CSN2	Negative Input of current sensing amplifier for channel 2. This pin combined with CSP2 senses the inductor current through an RC network.
9	CSP2	Positive Input of current sensing Amplifier for Channel 2. This pin combined with CSN2 senses the inductor current through an RC network.
10	DROOP	Load Line (droop) Setting. Connect a resistor between this pin and AGND to set the droop. A sourcing current, proportional to output current is present on the DROOP pin. The droop scale factor is set by the resistors (connected with CSP1, CSP2, and DROOP), resistance of the output inductors and the internal voltage divider with the ratio of 5%.
11	VID0	This is one of the inputs for the internal DAC that provides the reference voltage for output regulation. This pin responds to logic threshold. The APW7088 decodes the VID inputs to establish the output voltage; see VID Tables for correspondence between DAC codes and output voltage settings. This pin is internally pulled high at floating status.
12	COMP	Error Amplifier Output. Connect the compensation network between COMP, FB, and V_{OUT} for Type 2 or Type 3 feedback compensation.
13	FB	Feedback Voltage. This pin is the inverting input to the error comparator. A resistor divider from the output to AGND is used to set the regulation voltage.
14	SS	Soft-start Current Output. Connect a capacitor from this pin to AGND to set the soft-start interval. Pulling the voltage on this pin below 0.5V causes COMP to pull low and then shuts off the output.
15	VID1	One of DAC Inputs, same as VID0 and VID2.
16	POK	Power OK and 1.5V Reference Output. This pin is a reference output used to indicate the status of the voltages on SS pin and FB pin. POK provides 1.5V reference if V_{FB}> 87.5% of reference (V_R).
17	BOOT2	Bootstrap Supply for the floating high-side gate driver of channel 2. Connect the Bootstrap capacitor between the BOOT2 pin and the PHASE2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Typical values for C_{BOOT} range from 0.1µF to 1µF. Ensure that C_{BOOT} is placed near the IC.
18	UGATE2	High-side Gate Driver Output for Channel 2. Connect this pin to the gate of high-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off.
19	PHASE2	Switch Node for Channel 2. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off. An Schottky diode between this pin and ground is recommended to reduce negative transient voltage that is common in a power supply system.
20	LGATE2	Low-side Gate Driver Output for Channel 2. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.

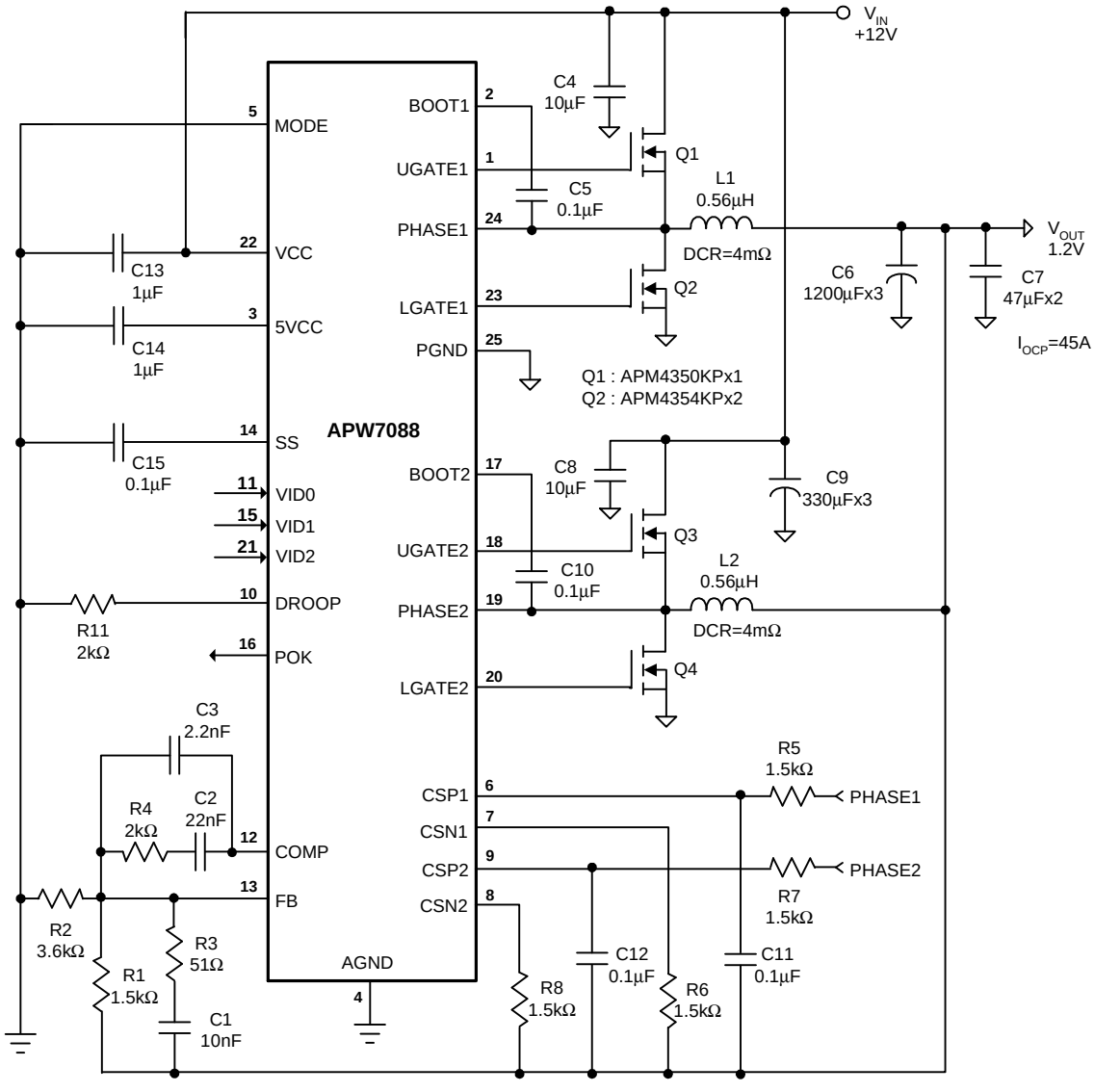
Pin Description (Cont.)

PIN	NAME	FUNCTION
21	VID2	One of DAC Inputs, same as VID0 and VID1.
22	VCC	Supply Voltage Input. This pin provides bias supply for the low-side gate drivers and the bootstrap circuit for high-side drivers. This pin can receive a well-decoupled 8V~13.2V supply voltage. Ensure that this pin is bypassed by a ceramic capacitor next to the pin.
23	LGATE1	Low-side Gate Driver Output for Channel 1. Connect this pin to the gate of low-side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the low-side MOSFET has turned off.
24	PHASE1	Switch Node for Channel 1. Connect this pin to the source of high-side MOSFET and the drain of the low-side MOSFET. This pin is used as sink for UGATT1 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the high-side MOSFET has turned off. An Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
25	PGND	Power Ground for the low-side gate drivers. Connect this pin to the source of low-side MOSFETs. This pin is used as sink for LGATE1 and LGATE2 drivers.

Block Diagram



Typical Application Circuit



Function Description

5VCC Linear Regulator

5VCC is the output terminal of the internal 5V linear regulator which regulates a 5V voltage on 5VCC by controlling an internal bypass transistor between VCC and 5VCC. The linear regulator powers the internal control circuitry and is stable with a low-ESR ceramic output capacitor. Bypass 5VCC to GND with a ceramic capacitor of at least 1µF. Place the capacitor physically close to the IC to provide good noise decoupling. The linear regulator can also provide output current, up to 20mA, for external loads. The linear regulator with current-limit protection can protect itself during over-load or short-circuit conditions on 5VCC pin.

The 5VCC linear regulator stop regulating in Over-Temperature Protection. When the junction temperature is cooled by 50°C, the 5VCC linear regulator starts to regulate the output voltage again.

5VCC Power-On-Reset (POR)

Figure 1 shows the power sequence. The APW7088 keeps monitoring the voltage on 5VCC pin to prevent wrong logic operations which may occur when 5VCC voltage is not high enough for the internal control circuitry to operate. The 5VCC POR has a rising threshold of 4.6V (typical) with 0.58V of hysteresis. After the 5VCC voltage exceeds its rising Power-On-Reset (POR) voltage threshold, the IC starts a start-up process and then ramps up the output voltage to the setting of output voltage. The 5VCC POR signal resets the fault latch, set by the undervoltage or over-current event, when the signal is at low level.

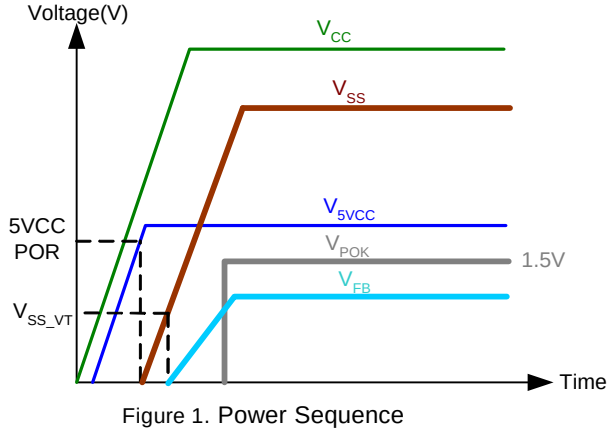


Figure 1. Power Sequence

When soft-start is initiated, the internal 10µA current source starts to charge the capacitor. When the soft-start voltage across the soft-start capacitor reaches the enabled threshold about 0.8V (V_{SS_VT}), the internal reference starts to rise and follows the soft-start voltage with converter operating at fixed 300kHz PWM switching frequency. When output voltage rises up to 87.5% of the regulation voltage, the power-ok is enabled. The soft-start time (from the moment of enabling the IC to the moment when V_{POK} goes high) can be expressed as below :

$$T_{SS} = \frac{C_{SS} \times (V_{SS\_VT} + V_{DAC} \times 0.875)}{I_{SS}}$$

where

C_{SS}= external soft-start capacitor

V_{SS_VT}= internal soft start threshold voltage, is about 0.8V

V_{DAC}= Internal digital VID programmable reference voltage

I_{SS}= soft-start current=10µA

During soft-start stage, the under-voltage protection is inhibited. However, the over-voltage and over-current protection functions are enabled. If the output capacitor has residue voltage before startup, both lower and upper MOSFETs are in off-state until the internal soft-start voltage equals the FB pin voltage. This will ensure the output voltage starts from its existing voltage level.

Operation Phase Selection

The MODE pin programs single- or two- phase operation. It has a typical value for rising threshold of 0.8V, V_{MODE_THR}, with 0.16V of hysteresis (0.64V), V_{MODE_THF}. When the MODE pin voltage is higher than the V_{MODE_THR}, the device operates in single-phase; when the MODE pin voltage is lower than V_{MODE_THF} and V_{IN2} supply voltage is above approximate 4V, the device operates in two-phase operation. This function makes the APW7088 ideally suitable for dual power input applications like PCIE interfaced graphic cards.

The figure 2 shows the power sources of the two channels. The input power of PWM1 converter is supplied by PCIE bus power and the input power of PWM2 converter is supplied by an external power. If the input power connector of PWM2 converter is not plugged into

Function Description (Cont.)

Operation Phase Selection (Cont.)

the socket before start-up, the internal V_{IN2} sensing circuit can sense the absence of V_{IN2} and set the IC to operate in single-phase mode with PWM2 disabled. When the IC operates in two-phase mode, it can switch the operating mode from two-phase to single-phase operation. Once operating in single-phase mode, the operation mode is latched. It is required to toggle SS or 5VCC pin to reset the IC.

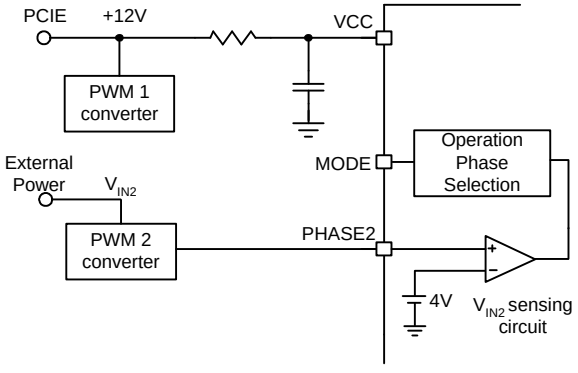


Figure 2. V_{IN2} Sensing Circuit

Over-Voltage Protection (OVP)

The over-voltage protection function monitors the output voltage through FB pin. When the FB voltage increases over 125% of the reference voltage (V_R) due to the high-side MOSFET failure or other reasons, the over-voltage protection comparator designed with a 2µs noise filter will force the low-side MOSFET gate drivers high. This action actively pulls down the output voltage and eventually attempts to trigger the over-current shutdown of an ATX power supply. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The chip will restore its normal operation. When the OVP occurs, the POK will drop to low as well.

This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFETs driver, which is a common problem for OVP schemes with a latch.

Under-Voltage Protection (UVP)

In the operational process, when a short-circuit occurs, the output voltage will drop quickly. Before the over-current protection responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the V_{FB} voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output. Cycling the 5VCC POR resets the fault latch and starts a start-up process. The under-voltage threshold is 50% of the nominal output voltage. The under-voltage comparator has a built-in 2µs noise filter to prevent the chips from wrong UVP shutdown being caused by noise.

Over-Current Protection (OCP)

Figure 3 shows the circuit of sensing inductor current. Connecting a series resistor (R_S) and a capacitor (C_S) network in parallel with the inductor and measuring the voltage (V_C) across the capacitor can sense the inductor current.

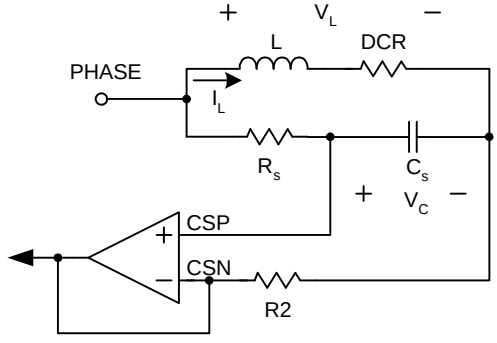


Figure 3. Illustration of Inductor Current Sensing Circuit

The equations of the sensing network are,

$$V_L(s)=I_L(s)\times(SL+DCR)$$

$$V_C(S) = V_L(S)\times\frac{1}{1+SR_SC_S} = \frac{I_L(S)\times(SL+DCR)}{1+SR_SC_S}$$

Take

$$R_SC_S = \frac{L}{DCR}$$

for example, if the above is true, the voltage across the capacitor C_S is equal to voltage drop across the inductor DCR, and the voltage V_C is proportional to the current I_L. The sensing current through the resistor R2 can be expressed as below :

$$I_{CS} = \frac{I_L\times DCR}{R2}$$

Function Description (Cont.)

Over-Current Protection (OCP) (Cont.)

where

I_{CS} is the sensed current
I_L is the inductor current
DCR is the inductor resistance
R2 is the sense resistor

The APW7088 is a two-phase PWM controller; therefore, the IC has two sensed current parts, I_{CS1} and I_{CS2}. When I_{CS1} plus I_{CS2} is greater than 120μA, the over current occurs. In over-current protection, the IC shuts off the converter and then initials a new soft-start process. After 3 over-current events are counted, the device turns off both high-side and low-side MOSFETs and the converter's output is latched to be floating.

Current Sharing

The APW7088 uses inductor's DCRs and external networks to sense the both currents flowing through the inductors of the PWM1 and PWM2 channels. The current sharing circuit, with closed-loop control, uses the sensed currents to adjust the two-phase inductor currents. For example, if the sensed current of PWM1 is bigger than PWM2, the duty of PWM1 will decrease and the duty of PWM2 will increase. Then, the device will reduce I_{L1} current and increase I_{L2} current for current sharing.

DROOP

In some high current applications, a requirement on precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed droop regulation.

As shown in figure 4, the droop control block generates a voltage through external resistor R_{DROOP}, then set the droop voltage. The droop voltage, V_{DROOP}, is proportional to the total current in two channels. As the following equation shows,

$$V_{DROOP} = 0.05 \times [(I_{CS1} + I_{CS2}) \times R_{DROOP}]$$

The V_{DROOP} voltage is used the regulator to adjust the output voltage so that it's equal to the reference voltage minus the droop voltage.

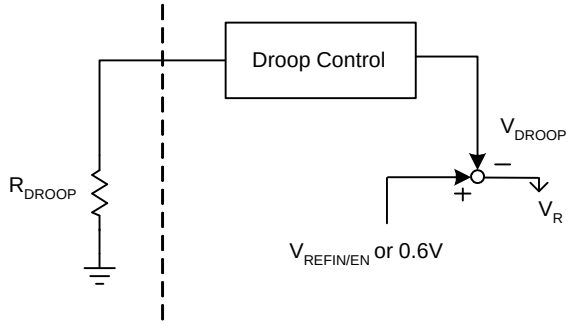


Figure 4. Illustration of Droop Setting Function

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTR}, the IC will enter the over-temperature protection state that suspends the PWM, which forces the LGATE and UGATE gate drivers to output low voltages and turns off the 5VCC linear regulator output. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, which increases lifetime of the APW7088.

Table 1. DAC Output Voltage vs. VID Inputs

VID2	VID1	VID0	DAC Output Voltage, V_{DAC} (V)
0	0	0	1.20
0	0	1	1.15
0	1	0	1.10
0	1	1	1.05
1	0	0	1.00
1	0	1	0.95
1	1	0	0.90
1	1	1	0.85

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.85V to 2.5V with a resistor-divider connected with FB, AGND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by :

$$V_{OUT} = V_{DAC} \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where V_{DAC} is the internal digital VID programmable reference voltage, the R_{TOP} is the resistor connected from converter's output to FB and R_{GND} is the resistor connected from FB to AGND. Suggested R_{GND} is in the range from 1K to 20KΩ. To prevent stray pickup, locate resistors R_{TOP} and R_{GND} close to the APW7088.

PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V_{OUT} should be added. The compensation network is shown in Figure 8. The output LC filters consists of the output inductors and output capacitors. For two-phase convertor, when assuming $V_{IN1}=V_{IN2}=V_{IN}$, L1=L2=L, the transfer function of the LC filter is given by :

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times \frac{1}{2} L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are :

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{\frac{1}{2} L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F_{LC} is the double-pole frequency of the two-phase LC filters, and F_{ESR} is the frequency of the zero introduced by the ESR of the output capacitors.

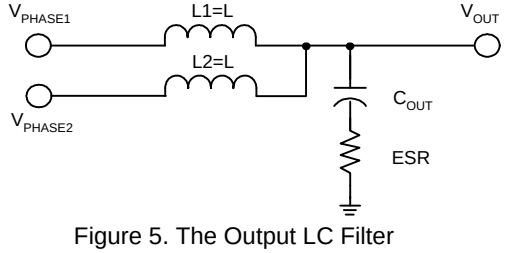


Figure 5. The Output LC Filter

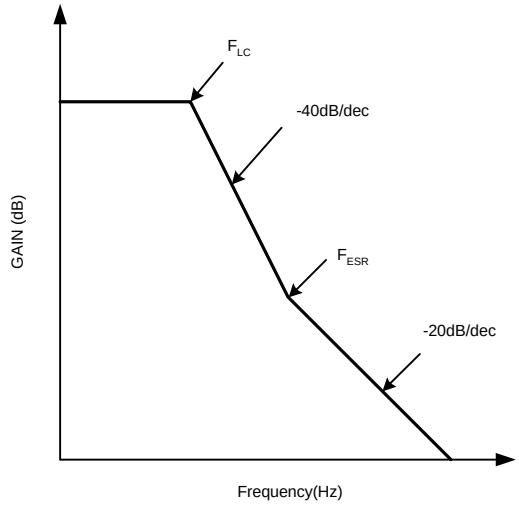


Figure 6. Frequency Resopnse of the LC filters

The PWM modulator is shown in figure 7. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by :

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

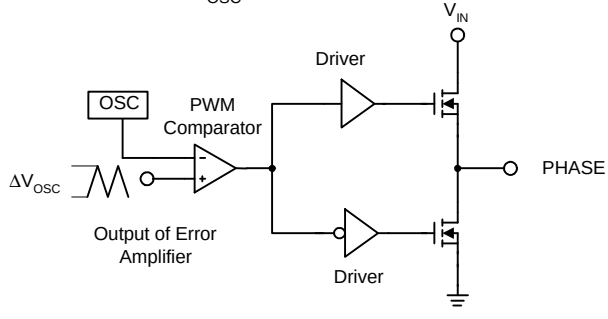


Figure 7. The PWM Modulator

The compensation network is shown in figure 8. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin.

The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{\frac{1}{sC1} // \left(R2 + \frac{1}{sC2}\right)}{R1 // \left(R3 + \frac{1}{sC3}\right)}$$

$$= \frac{R1+R3}{R1 \times R3 \times C1} \times \frac{\left(s + \frac{1}{R2 \times C2}\right) \times \left(s + \frac{1}{(R1+R3) \times C3}\right)}{s\left(s + \frac{C1+C2}{R2 \times C1 \times C2}\right) \times \left(s + \frac{1}{R3 \times C3}\right)}$$

Application Information (Cont.)

PWM Compensation (Cont.)

The pole and zero frequencies of the transfer function are:

$$F_{Z1} = \frac{1}{2\times\pi\times R2\times C2}$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R1+R3)\times C3}$$

$$F_{P1} = \frac{1}{2\times\pi\times R2\times\left(\frac{C1\times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\times\pi\times R3\times C3}$$

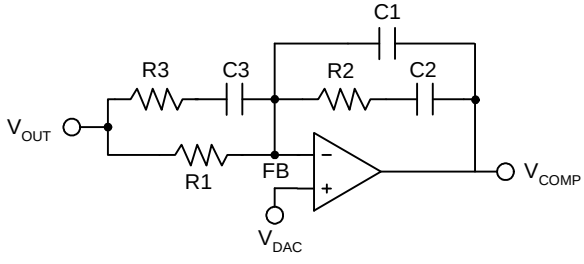


Figure 8. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \text{ X } GAIN_{PWM} \text{ X } GAIN_{AMP}$$

Figure 9. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/ decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.

2. Select the desired zero crossover frequency

F_O= (1/5 ~ 1/10) X F_{SW}

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}}\times\frac{F_O}{F_{LC}}\times R1$$

3. Place the first zero F_{Z1} before the output LC filter double pole frequency F_{LC}.

F_{Z1} = 0.75 X F_{LC}

Calculate the C2 by the following equation:

$$C2 = \frac{1}{2\times\pi\times R2\times F_{LC}\times 0.75}$$

4. Set the pole at the ESR zero frequency F_{ESR}:

F_{P1} = F_{ESR}

Calculate the C1 by the following equation:

$$C1 = \frac{C2}{2\times\pi\times R2\times C2\times F_{ESR} - 1}$$

5. Set the second pole F_{P2} at the half of the switching frequency and also set the second zero F_{Z2} at the output LC filter double pole F_{LC}. The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at F_{P2} with the capabilities of the error amplifier.

F_{P2} = 0.5 X F_{SW}

F_{Z2} = F_{LC}

Combine the two equations will get the following component calculations:

$$R3 = \frac{R1}{\frac{F_{SW}}{2\times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi\times R3\times F_{SW}}$$

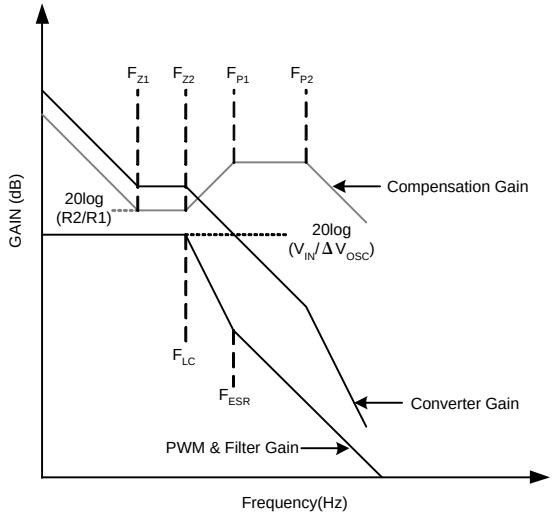


Figure 9. Converter Gain and Frequency

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

Application Information (Cont.)

Output Inductor Selection (Cont.)

$$D = \frac{V_{OUT}}{V_{IN}}$$

For two-phase converter, the inductor value (L) determines the sum of the two inductor ripple currents, ΔI_{P-P}, and affects the load transient reponse. Higher inductor value reduces the output capacitors' ripple current and induces lower output ripple voltage. The ripple current can be approxminated by :

$$\Delta I_{P-P} = \frac{V_{IN} - 2V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, select an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting output capacitors. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak sum of the inductor's current. The ripple voltage of output capacitors can be represented by:

$$\Delta V_{COUT} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times F_{SW}}$$

$$\Delta V_{ESR} = \Delta I_{P-P} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be parallelled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. For getting same load transient response, the output capacitance of two-phase converter only needs around half of output capacitance of single-phase converter.

Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current needed each time high-side MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of high-side MOSFET and the source of low-side MOSFET.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. For two-phase converter, the RMS current of the bulk input capacitor is roughly calculated as the following equation:

Application Information (Cont.)

Input Capacitor Selection (Cont.)

$$I_{RMS} = \frac{I_{OUT}}{2} \times \sqrt{2D \cdot (1-2D)}$$

For a through hole design, several electrolytic capacitors may be needed. For surface mount design, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.

MOSFET Selection

The APW7088 requires two N-Channel power MOSFETs on each phase. These should be selected based upon $R_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components, conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the high-side and the low-side MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by the APW7088 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature, and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

where

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short, wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Figure 10. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout :

Application Information (Cont.)

Layout Consideration (Cont.)

- Keep the switching nodes (UGATEx, LGATEx, BOOTx, and PHASEx) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATEx, LGATEx) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASEx nodes) can get better heat sinking.
- For experiment result of accurate current sensing, the current sensing components are suggested to place close to the inductor part. To avoid the noise interference, the current sensing trace should be away from the noisy switching nodes.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible).
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UGATEx, LGATEx, BOOTx, and PHASEx).

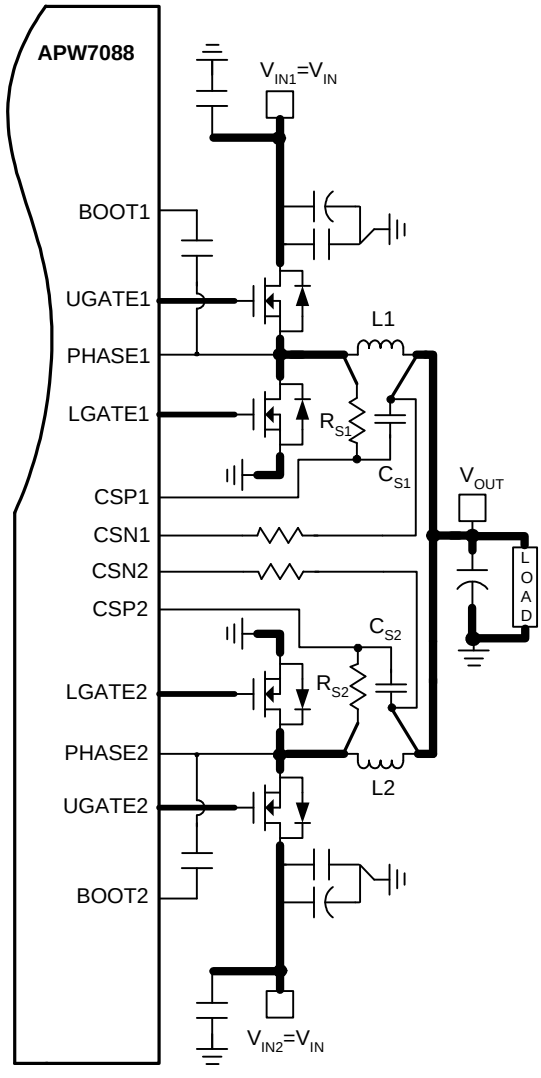
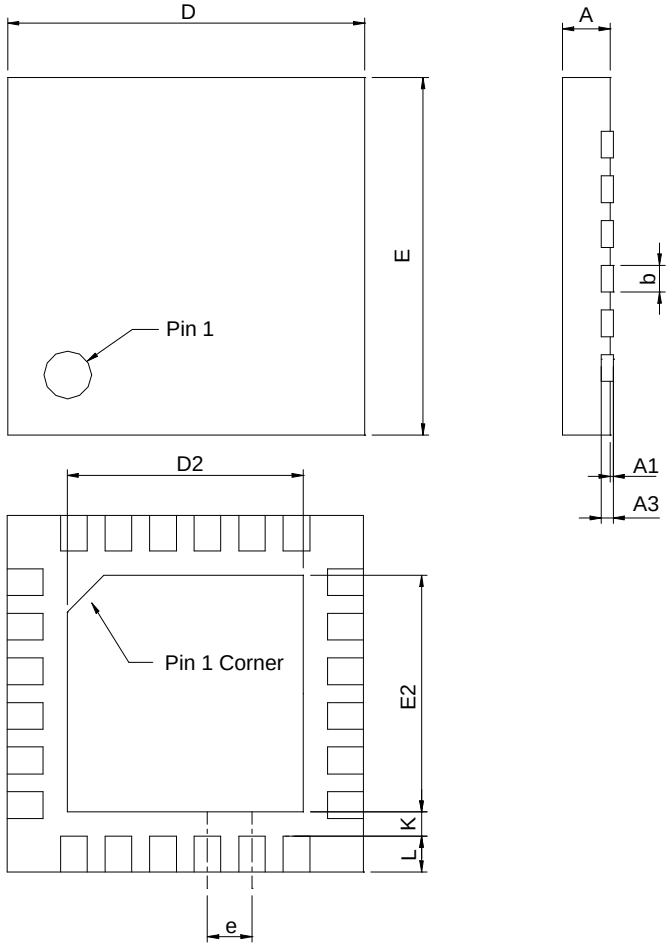


Figure 10. Layout Guidelines

Package Information

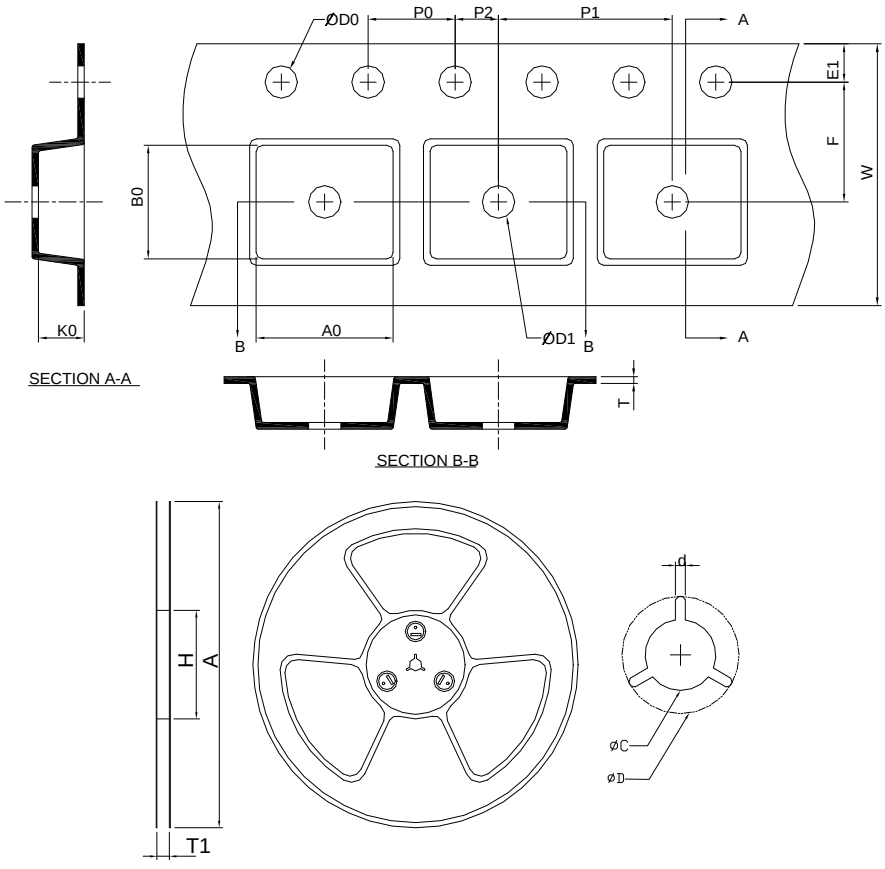
QFN4x4-24



SYMBOL	QFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.50	2.80	0.098	0.110
E	3.90	4.10	0.154	0.161
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-220 WGGD-6.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN4x4-24	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

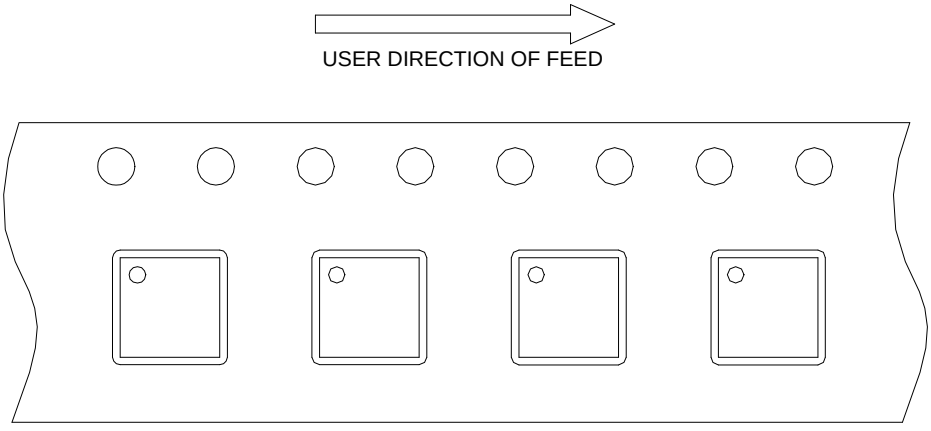
(mm)

Devices Per Unit

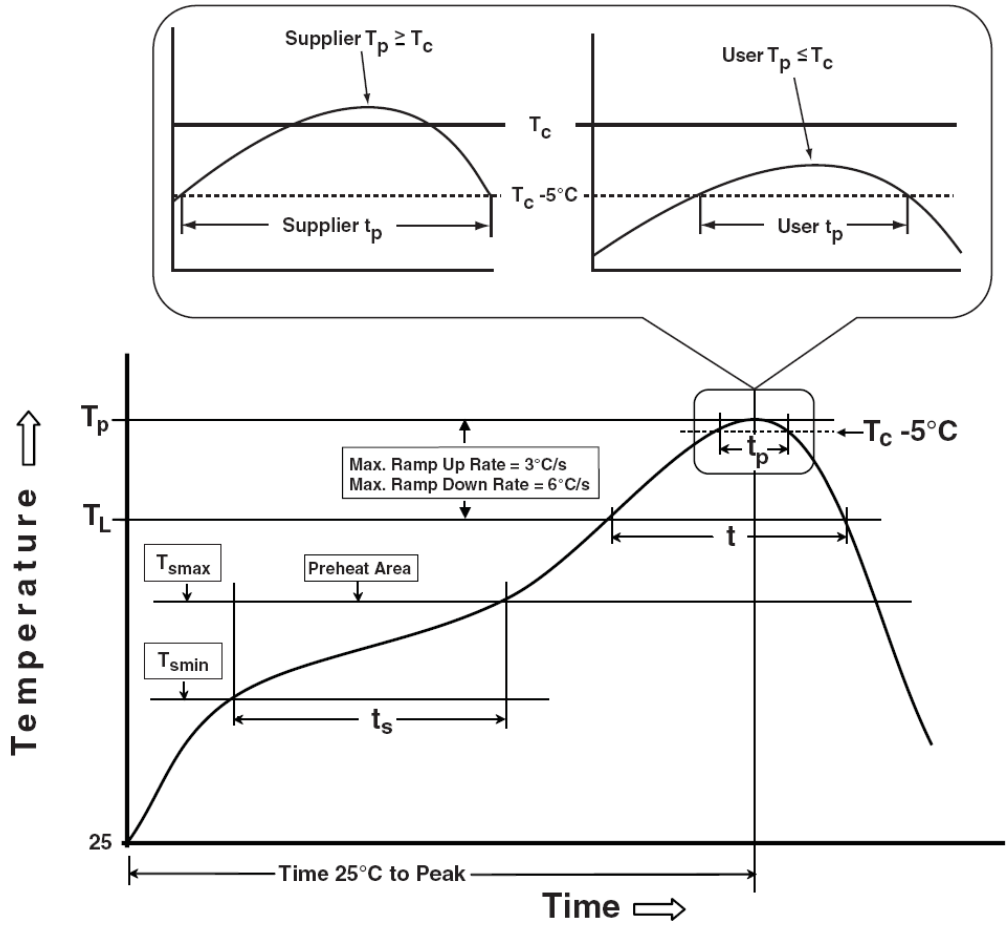
Package Type	Unit	Quantity
QFN4x4-24	Tape & Reel	3000

Taping Direction Information

QFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
ESD	MIL-STD-883E-3015.7	VHBM≧2KV, VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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