



# 6-Bit Programmable 2 / 3 / 4-Phase Synchronous Buck Controller

## Preliminary Technical Data

## ADP3168

### FEATURES

- Selectable 2-, 3- or 4-Phase Operation at up to 1 MHz per Phase
- ±10 mV DAC Accuracy Over Temperature
- Logic-level PWM Outputs for Interface to External High-power Drivers
- Active Current Balancing Between All Output Phases
- Built-in Power Good/Crowbar Blanking Supports
- On-the-fly VID Code Changes
- 6-Bit Digitally Programmable 0.8375 V to 1.6 V Output
- Programmable Short Circuit Protection with Programmable Latch-off Delay

### APPLICATIONS

- Desktop PC Power Supplies for:
  - Next-generation Intel Processors
  - VRM Modules

### GENERAL DESCRIPTION

The ADP3168 is a highly efficient multi-phase synchronous buck switching regulator controller optimized for converting a 12 V main supply into the core supply voltage required by high performance Intel processors. It uses an internal 6-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 0.8375 V and 1.6 V, and uses a multi-mode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 2-, 3-, or 4-phase operation, allowing for the construction of up to four complementary buck switching stages.

The ADP3168 also includes programmable no-load offset and slope functions to adjust the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3168 also provides accurate and reliable short circuit protection, adjustable current limiting, and a delayed Power Good output that accommodates on-the-fly output voltage changes requested by the CPU.

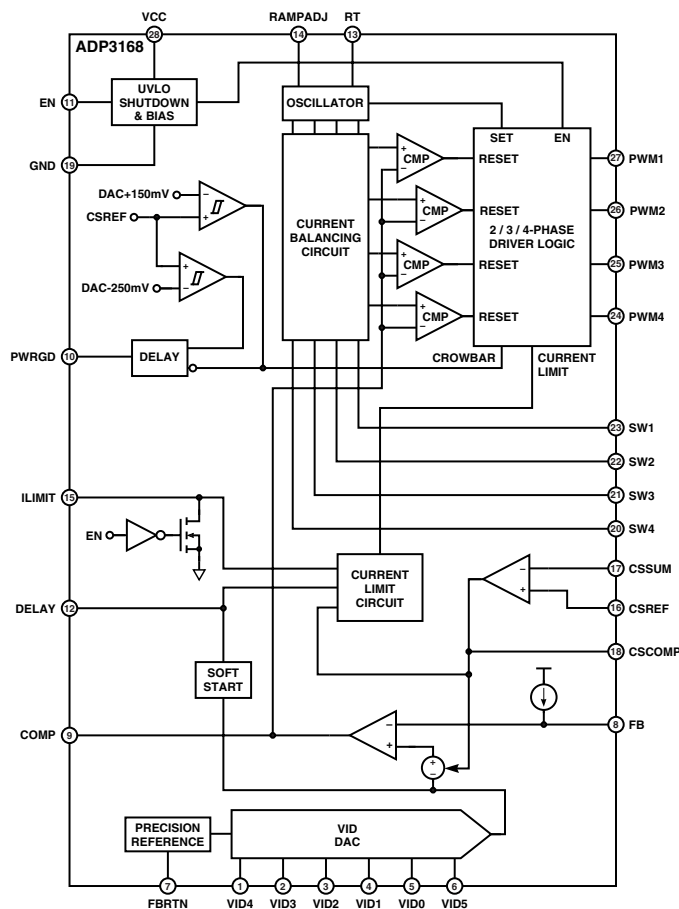
ADP3168 is specified over the commercial temperature range of 0°C to +85°C and is available in a 28-lead TSSOP package.

Patent Pending

REV. PrK 10/4/02

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### FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

# ADP3168—SPECIFICATIONS<sup>1</sup> (VCC = 12 V, FBRTN = GND, T<sub>A</sub> = 0°C to +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>ERROR AMPLIFIER</b>						
Accuracy	V <sub>FB</sub>	Relative to Nominal DAC Output, Referenced to FBRTN, CSSUM = CSCOMP, Figure 3	-10		10	mV
Line Regulation	ΔV <sub>FB</sub>	VCC = 10 V to 14 V		0.05		%
Input Bias Current	I <sub>FB</sub>		13	15	17	μA
FBRTN Current	I <sub>FBRTN</sub>			100	200	μA
Output Current	I <sub>O(ERR)</sub>	FB Forced to V <sub>OUT</sub> - 3%		500		μA
Gain Bandwidth Product	GBW <sub>(ERR)</sub>	COMP = FB		20		MHz
Slew Rate		C <sub>COMP</sub> = 10 pF		50		V/μs
<b>VID INPUTS</b>						
Input Low Voltage	V <sub>IL(VID)</sub>				0.4	V
Input High Voltage	V <sub>IH(VID)</sub>		0.8			V
Input Current, Input Voltage Low	I <sub>IL(VID)</sub>	VID(X) = 0 V		-20	-30	μA
Input Current, Input Voltage High	I <sub>IH(VID)</sub>	VID(X) = 1.25 V		15	25	μA
Pull-up Resistance	R <sub>VID</sub>		50	60		kΩ
Internal Pull-up Voltage			0.85	1.00	1.15	V
VID Transition Delay Time <sup>2</sup>		VID Code Change to FB Change	400			ns
No CPU Detection Turn-off Delay Time <sup>2</sup>		VID Code Change to 11111 to PWM going low	400			ns
<b>OSCILLATOR</b>						
Maximum Frequency <sup>2</sup>	f <sub>PHASE(MAX)</sub>	4-Phase	1			MHz
Frequency Variation	f <sub>PHASE</sub>	T <sub>A</sub> = +25°C, R <sub>T</sub> = 250 kΩ, 4-Phase	160	200	240	kHz
		T <sub>A</sub> = +25°C, R <sub>T</sub> = 115 kΩ, 4-Phase	320	400	480	kHz
		T <sub>A</sub> = +25°C, R <sub>T</sub> = 75 kΩ, 4-Phase	480	600	720	kHz
Output Voltage	V <sub>RT</sub>	R <sub>T</sub> = 100 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	V <sub>RAMPADJ</sub>	RAMPADJ - FB	-50		+50	mV
RAMPADJ Input Current Range	I <sub>RAMPADJ</sub>		0		50	μA
<b>CURRENT SENSE AMPLIFIER</b>						
Offset Voltage	V <sub>OS(CSA)</sub>	CSSUM - CSREF, See Figure 1	-1.5		+1.5	mV
Input Bias Current	I <sub>BIAS(CSA)</sub>			20	100	nA
Gain Bandwidth Product	GBW <sub>(CSA)</sub>			20		MHz
Slew Rate		C <sub>CSCOMP</sub> = 10 pF		50		V/μs
Input Common Mode Range		CSSUM and CSREF	0		3	V
Positioning Accuracy	ΔV <sub>FB</sub>	FB - V <sub>VID</sub> , See Figure 2	-76	-80	-84	mV
Output Current	I <sub>CSCOMP</sub>			500		μA
<b>CURRENT BALANCE CIRCUIT</b>						
Common Mode Range	V <sub>SW(X)CM</sub>		-600		+200	mV
Input Resistance	R <sub>SW(X)</sub>	SW(X) = 0 V	24	30	36	kΩ
Input Current	I <sub>SW(X)</sub>	SW(X) = 0 V	5	7	9	μA
Input Current Matching	ΔI <sub>SW(X)</sub>	SW(X) = 0 V	-5		+5	%
<b>CURRENT LIMIT COMPARATOR</b>						
Output Voltage						
Normal Mode	V <sub>ILIMIT(NM)</sub>	EN > 1.7 V, R <sub>ILIMIT</sub> = 250 kΩ	2.9	3	3.1	V
In Shutdown	V <sub>ILIMIT(SD)</sub>	EN < 0.8 V, I <sub>ILIMIT</sub> = -100 μA			400	mV
Output Current, Normal Mode	I <sub>ILIMIT(NM)</sub>	EN > 1.7 V, R <sub>ILIMIT</sub> = 250 kΩ		12		μA
Current Limit Threshold Voltage	V <sub>CL</sub>	V <sub>CSREF</sub> - V <sub>CSCOMP</sub> , R <sub>ILIMIT</sub> = 250 kΩ	115	125	135	mV
Current Limit Setting Ratio		V <sub>CL</sub> /I <sub>ILIMIT</sub>		10		mV/μA
Latch-off Delay Threshold	V <sub>DELAY</sub>	In Current Limit	1.7	1.8	1.9	V
Latch-off Delay Time	t <sub>DELAY</sub>	R <sub>DELAY</sub> = 250 kΩ, C <sub>DELAY</sub> = 4.7 nF		1.2		ms

NOTES

<sup>1</sup> All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

<sup>2</sup> Guaranteed by design, not tested in production.

Specifications subject to change without notice.

# PRELIMINARY TECHNICAL DATA

## ADP3168

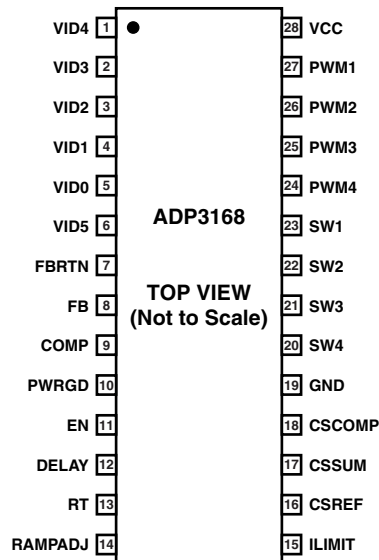
Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>SOFT START</b> Output Current, Soft-start Mode Soft-start Delay Time	$I_{\text{DELAY(SS)}}$ $t_{\text{DELAY(SS)}}$	During Start-up, $\text{DELAY} < 2.8 \text{ V}$ $R_{\text{DELAY}} = 250 \text{ k}\Omega$ , $C_{\text{DELAY}} = 4.7 \text{ nF}$ VID Code = 011111	15	20 1	25	$\mu\text{A}$ ms
<b>ENABLE INPUT</b> Input Low Voltage Input High Voltage Input Current, Input Voltage Low Input Current, Input Voltage High	$V_{\text{IL(EN)}}$ $V_{\text{IH(EN)}}$ $I_{\text{IL(EN)}}$ $I_{\text{IH(EN)}}$	$\text{EN} = 0 \text{ V}$ $\text{EN} = 1.25 \text{ V}$	0.8 -1	15	0.4 1 25	V V $\mu\text{A}$ $\mu\text{A}$
<b>POWER GOOD COMPARATOR</b> Undervoltage Threshold Overvoltage Threshold Output Low Voltage Power Good Delay Time VID Code Changing VID Code Static Crowbar Trip Point Crowbar Reset Point Crowbar Delay Time VID Code Changing VID Code Static	$V_{\text{PWRGD(UV)}}$ $V_{\text{PWRGD(OV)}}$ $V_{\text{OL(PWRGD)}}$ $V_{\text{CROWBAR}}$ $t_{\text{CROWBAR}}$	Relative to Nominal Output Relative to Nominal Output $I_{\text{PWRGD(SINK)}} = 4 \text{ mA}$ Relative to Nominal Output Overvoltage to PWM Going Low	-200 100 100	-250 150 250 200	-300 200 400 150 200 200 200 450 550 400	mV mV mV $\mu\text{s}$ ns mV mV $\mu\text{s}$ ns
<b>PWM OUTPUTS</b> Output Voltage Low Output Voltage High	$V_{\text{OL(PWM)}}$ $V_{\text{OH(PWM)}}$	$I_{\text{PWM(SINK)}} = 400 \mu\text{A}$ $I_{\text{PWM(SOURCE)}} = 400 \mu\text{A}$	4.0	100 5.0	500	mV V
<b>SUPPLY</b> DC Supply Current UVLO Threshold Voltage UVLO Hysteresis	$V_{\text{UVLO}}$		6.8 0.5	7 0.8	10 7.2 1.0	mA V V

### ABSOLUTE MAXIMUM RATINGS\*

VCC	-0.3 V to 15 V
FBRTN	-0.3 V to 0.3 V
VID0 – VID5	-0.3 V to 5.5 V
SW1 – SW4	-5 V to 25 V
All Other Inputs & Outputs	-0.3 V to VCC + 0.3 V
Operating Ambient Temperature Range	0°C to +85°C
Operating Junction Temperature	+125°C
Storage Temperature Range	-65°C to +150°C
$\theta_{\text{JA}}$	100°C/W
Lead Temperature (Soldering, 10 sec)	+300°C
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

\*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

### PIN CONFIGURATION RU-28



### CAUTION

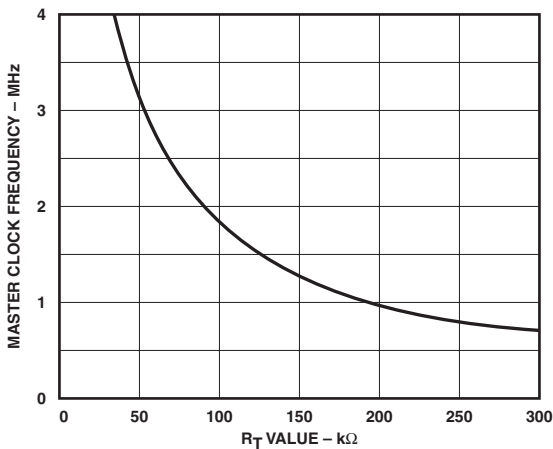
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3168 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADP3168

PIN FUNCTION DESCRIPTIONS

Pin	Name	Function
1-6	VID4 – VID0, VID5	Voltage Identification DAC Inputs. These six pins are pulled up to an internal reference, providing a logic one if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.8375 V to 1.6 V. Leaving all VID4 through VID0 open results in ADP3168 going into a “No CPU” mode, shutting off its PWM outputs.
7	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
8	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no-load offset point.
9	COMP	Error Amplifier Output and Compensation Point.
10	PWRGD	Power Good Output. Open drain output that signals when the output voltage is outside of the proper operating range.
11	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs.
12	DELAY	Soft-start Delay and Current Limit Latch-off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft-start ramp-up time and the overcurrent latch-off delay time.
13	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
14	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
15	ILIMIT	Current Limit Set Point / Enable Output. An external resistor from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the ADP3168 EN input is low, or when VCC is below its UVLO threshold to signal to the driver IC that the driver high-side and low-side outputs should go low.
16	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the Power Good and Crowbar functions. This pin should be connected to the common point of the output inductors.
17	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
18	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the slope of the load line and the positioning loop response time.
19	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
20-23	SW4 – SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be grounded.
24-27	PWM4 – PWM1	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3413 or ADP3418. Connecting the PWM3 and/or PWM4 outputs to GND will cause that phase to turn off, allowing the ADP3168 to operate as a 2-, 3-, or 4-phase controller.
28	VCC	Supply Voltage for the device.



TPC 1. Master Clock Frequency vs.  $R_T$

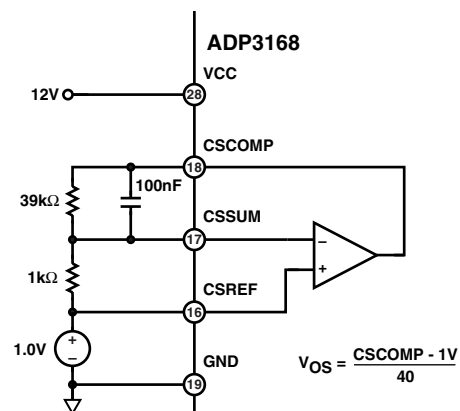


Figure 1. Current Sense Amplifier  $V_{OS}$  Test Circuit



# ADP3168

## THEORY OF OPERATION

The ADP3168 combines a multi-mode, fixed frequency PWM control with multi-phase logic outputs for use in 2, 3 and 4 phase synchronous buck CPU core supply power converters. The internal 6-bit VID DAC conforms to Intel's VRD / VRM 10 specifications. Multi-phase operation is important for producing the high currents and low voltages demanded by today's microprocessors. Handling the high currents in a single-phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs.

The multi-mode control of the ADP3168 ensures a stable, high performance topology for:

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- High current output from having up to 4 phase operation
- Reduced output ripple due to multi-phase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

### Number of Phases

The number of operational phases and their phase relationship is determined by internal circuitry which monitors the PWM outputs. Normally, the ADP3168 operates as a 4-phase PWM controller. Grounding the PWM4 pin programs 3-phase operation, and grounding the PWM3 and PWM4 pins programs 2-phase operation.

When the ADP3168 is enabled, the controller outputs a voltage on PWM3 and PWM4 that is approximately 500 mV. An internal comparator checks each pin's voltage versus a threshold of 400 mV. If the pin is grounded, then it will be below the threshold and the phase will be disabled. The output impedance of the PWM pin is approximately 5 k $\Omega$ . Any external pull-down resistance connected to the PWM pin should not be less than 25 k $\Omega$  to ensure proper operation. The phase detection is made during the first 2 clock cycles of the internal oscillator. After this time, if the PWM output was not grounded, then it will switch between 0 V and 5 V. If the PWM output was grounded, then it will remain off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3418. Since each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at a time for overlapping phases.

### Master Clock Frequency

The clock frequency of the ADP3168 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in TPC 1. To determine the frequency per phase, the clock is divided by the number of

phases in use. If PWM4 is grounded, then divide the master clock by 3 for the frequency of the remaining phases. If PWM3 and 4 are grounded, then divide by 2. If all phases are in use, divide by 4.

### Output Voltage Differential Sensing

The ADP3168 combines differential sensing with a high accuracy VID DAC and reference and a low offset error amplifier to maintain a worst-case specification of  $\pm 10$  mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the remote sense pin of the microprocessor. FBRTN should be connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 100  $\mu$ A to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

### Output Current Sensing

The ADP3168 provides a dedicated current sense amplifier (CSA) to monitor the total output current for proper voltage positioning versus load current and for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor ESR sensing without thermistor for lowest cost

- Output inductor ESR sensing with thermistor for improved accuracy with tracking of inductor temperature

- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor to set the load line required by the microprocessor. The current information is then given as the difference of CSREF – CSCOMP. This difference signal is used internally to offset the VID DAC for voltage positioning and as a differential input for the current limit comparator.

To provide the best accuracy for the sensing of current, the CSA has been designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate.

### Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, a signal proportional to the total output current at the CSCOMP pin can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the

input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This differs from previous implementations and allows enhanced feed-forward response.

#### Current Control Mode and Thermal Balance

The ADP3168 has individual inputs for each phase which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. Detailed information about programming the ramp is given in the applications section.

External resistors can be placed in series with individual phases to create an intentional current imbalance if desired, such as when one phase may have better cooling and can support higher currents. The ADP3168 gives the designer the flexibility to program the relative currents in each phase to support this.

Figure 4 shows the output voltage and inductor currents of a typical application circuit. Note that the currents between phases are evenly balanced, and that these currents are very well controlled during transitions between output current levels.

#### Voltage Control Mode

A high gain-bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is set via the VID 6-bit logic code according to the voltages listed in Table 1. This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the output sense location with a resistor  $R_B$  and is used for sensing and controlling the output voltage at this point. A current source from the FB pin flowing through  $R_B$  is used for setting the no-load offset voltage from the VID voltage. The no-load voltage will be negative with respect to the VID DAC. The main loop compensation is incorporated in the feedback network between FB and COMP.

#### Soft-start

The power-on ramp up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch off time as explained in the following

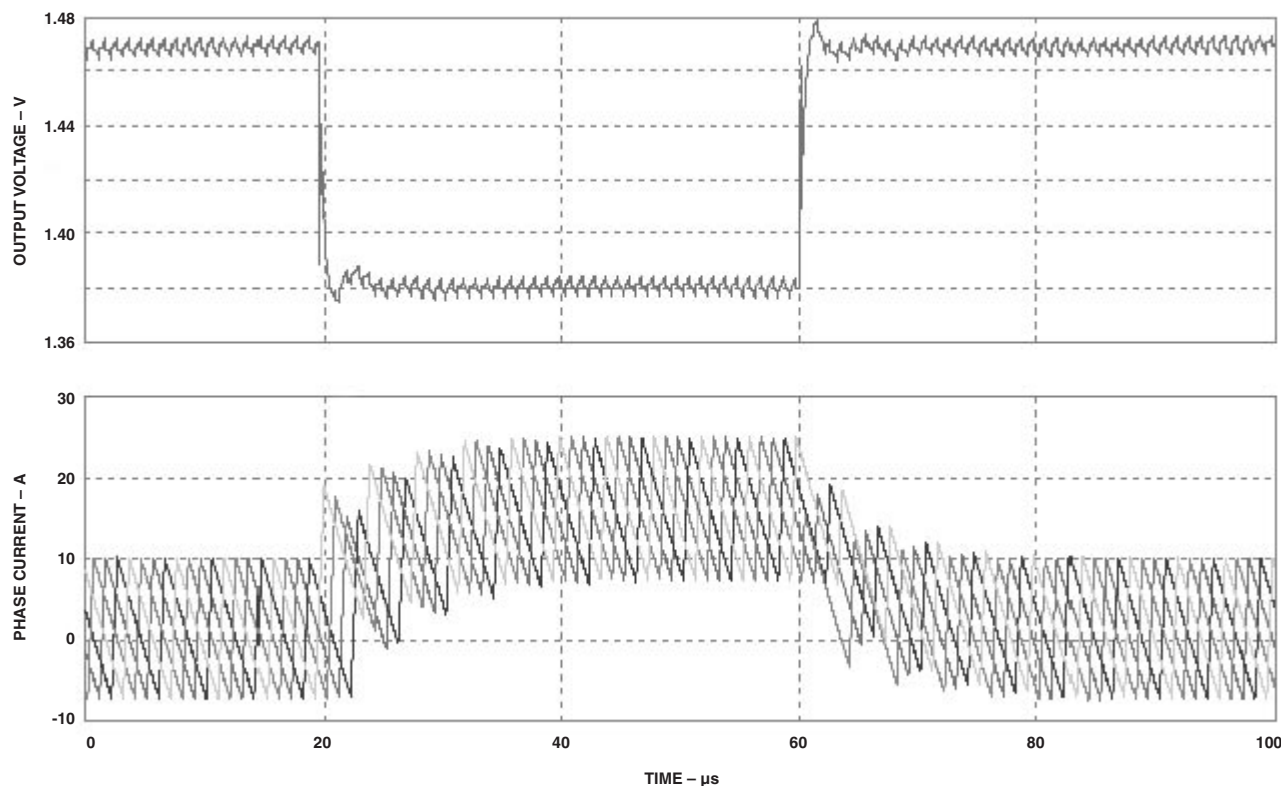


Figure 4. Transient Performance and Inductor Current Balance of the ADP3168 for a 5 A to 65 A Load Step



## ADP3168

section. In UVLO or when EN is a logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is a logic high, the DELAY cap is charged up with an internal 20  $\mu$ A current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft-start time depends on the value of VID DAC and  $C_{DLY}$ , with a secondary effect from  $R_{DLY}$ . Refer to the applications section for detailed information on setting  $C_{DLY}$ .

When the PWRGD threshold is reached, the soft-start cycle is stopped and the DELAY pin is pulled up to 3 V. This ensures that the output voltage is at the VID voltage when the PWRGD signals to the system that the output voltage is good. If either EN is taken low or VCC drops below UVLO, the DELAY cap is reset to ground to be ready for another soft start cycle.

### Current Limit, Short Circuit and Latch-off Protection

The ADP3168 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3V. The current through the external resistor is internally scaled to give a current limit threshold of 10 mV/ $\mu$ A. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier will control the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current limit latch off delay time is therefore set by the RC time constant discharging from 3 V to 1.8 V. The applications section discusses the selection of  $C_{DLY}$  and  $R_{DLY}$ .

Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.8 V threshold is reached, the controller will return to normal operation. The recovery characteristic depends on the state of PWRGD. If the output voltage is within the PWRGD window, the controller resumes normal operation. However, if short circuit has caused the output voltage to drop below the PWRGD threshold, then a soft-start cycle is initiated.

The latch-off function can be reset by either removing and reapplying VCC to the ADP3168, or by pulling the EN pin low for a short time. To disable the short circuit latch-off function, the external resistor to ground should be left open, and a large (greater than 1 M $\Omega$ ) resistor should be connected from VCC to DELAY. This prevents the DELAY capacitor from discharging so the 1.8 V threshold is never reached. The resistor will have an impact on the soft-start time because the current through it will add to the internal 20  $\mu$ A current source.

During start-up when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This will

limit the voltage drop across the low side MOSFETs through the current balance circuitry.

There is also an inherent per phase current limit that will protect individual phases in the case where one or more phases may stop functioning because of a faulty component. This limit is based on the maximum normal-mode COMP voltage.

### Dynamic VID

The ADP3168 incorporates the ability to dynamically change the VID input while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as VID-on-the-fly (OTF). A VID-OTF can occur under either light load or heavy load conditions. The processor signals the controller by changing the VID inputs in multiple steps from the start code to the finish code. This change can be either positive or negative.

When a VID input changes state, the ADP3168 detects the change and ignores the DAC inputs for a minimum of 400 ns. This time is to prevent a false code due to logic skew while the 6 VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 250  $\mu$ s to prevent a false PWRGD or CROWBAR event. Each VID change will reset the internal timer.

### Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the specifications above based on the VID voltage setting. PWRGD will go low if the output voltage is outside of this specified range. PWRGD is blanked during a VID-OTF event for a period of 250  $\mu$ s to prevent false signals during the time the output is changing.

### Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs will be driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper power good threshold. This crowbar action will stop once the output voltage has fallen below the release threshold of approximately 450 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action will current limit the input supply or blow its fuse, protecting the microprocessor from destruction.

### Output Enable and UVLO

The input supply (VCC) to the controller must be higher than the UVLO threshold and the EN pin must be higher than its logic threshold for the ADP3168 to begin switching. If UVLO is less than the threshold or the EN pin is a logic low, the ADP3168 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the  $\overline{OD}$  pins of the ADP3418 drivers. Because



ILIMIT is grounded, this disables the drivers such that both DRVH and DRVL are grounded. This feature is important to prevent discharging of the output capacitors when the controller is shut off. If the driver outputs were not disabled, then a negative voltage could be generated on the output due to the high current discharge of the output capacitors through the inductors.

### APPLICATION INFORMATION

The design parameters for a typical Intel VRD 10-compliant CPU application are as follows:

Input voltage ( $V_{IN}$ ) = 12 V

VID setting voltage ( $V_{VID}$ ) = 1.500 V

Duty cycle (D) = 0.125

Nominal output voltage at no load ( $V_{ONL}$ ) = 1.480 V

Nominal output voltage at 65 A load ( $V_{OFL}$ ) = 1.3825 V

Static output voltage drop based on a 1.5 m $\Omega$  load line ( $R_O$ ) from no load to full load

( $V_D$ ) =  $V_{ONL} - V_{OFL} = 1.480 \text{ V} - 1.3825 \text{ V} = 97.5 \text{ mV}$

Maximum Output Current ( $I_O$ ) = 65 A

Number of Phases (n) = 3

Switching frequency per phase ( $f_{SW}$ ) = 330 kHz

### Setting the Clock Frequency

The ADP3168 uses a fixed-frequency control architecture. The frequency is set by an external timing resistor ( $R_T$ ). The clock frequency and the number of phases determine the switching frequency per phase, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. With  $n = 3$  for three phases, a clock frequency of 990 kHz sets the switching frequency of each phase,  $f_{SW}$ , to 330 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. TPC 1 shows that to achieve a 990 kHz oscillator frequency, the correct value for  $R_T$  is 200 k $\Omega$ . For good initial accuracy and frequency stability, it is recommended to use a 1% resistor.

### Soft-Start and Current Limit Latch-Off Delay Times

Because the soft-start and current limit latch off delay functions share the DELAY pin, these two parameters must be considered together. The first step is to set  $C_{DLY}$  for the soft-start ramp. This ramp is generated with a 20  $\mu$ A internal current source. The value of  $R_{DLY}$  will have a second-order impact on the soft-start time because it sinks part of the current source to ground. However, as long as  $R_{DLY}$  is kept greater than 200 k $\Omega$ , this effect is minor. The value for  $C_{DLY}$  can be approximated using:

$$C_{DLY} = \left( 20\mu\text{A} - \frac{V_{VID}}{2 \times R_{DLY}} \right) \times \frac{t_{SS}}{V_{VID}} \quad (1)$$

Where  $t_{SS}$  is the desired soft-start time. Assuming an  $R_{DLY}$  of 250 k $\Omega$  and a desired a soft-start time of 900  $\mu$ s,  $C_{DLY}$  is 10 nF.

Once  $C_{DLY}$  has been chosen,  $R_{DLY}$  can be calculated for the current limit latch off time using:

$$R_{DLY} = \frac{2 \times t_{DELAY}}{C_{DLY}} \quad (2)$$

If the result for  $R_{DLY}$  is less than 200 k $\Omega$ , then a smaller soft-start time should be considered by recalculating the equation for  $C_{DLY}$  or a longer latch-off time should be used. In no case should  $R_{DLY}$  be less than 200 k $\Omega$ . In this example, a delay time of 2 ms gives  $R_{DLY} = 400 \text{ k}\Omega$ . The closest standard 5% value is 390 k $\Omega$ . Substituting 390 k $\Omega$  back into Equation 1 shows that the soft-start time changes slightly from 900  $\mu$ s to 830  $\mu$ s.

### Inductor Selection

The choice of inductance for the inductor determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, less total output capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In any multi-phase converter, a practical value for the peak-to-peak inductor ripple current is less than 80% of the maximum DC current in the same inductor. Equation 3 shows the relationship between the inductance, oscillator frequency, and peak-to-peak ripple current in the inductor. Equation 4 can be used to determine the minimum inductance based on a given output ripple voltage:

$$I_{RIPPLE} = \frac{V_O \times (1 - D)}{f_{SW} \times L} \quad (3)$$

$$L \geq \frac{V_O \times R_O \times (1 - D) \times (1 - (n \times D))}{f_{SW} \times V_{RIPPLE}} \quad (4)$$

Intel recommends that the ripple voltage should not exceed 10 mV peak-to-peak at the socket. Solving Equation 4 for a 12 mV peak-to-peak output ripple voltage at the regulator's output to allow for drops through the PCB traces yields:

$$L \geq \frac{1.5\text{V} \times 1.5\text{m}\Omega \times 0.875 \times (1 - 0.375)}{330\text{kHz} \times 12\text{mV}} = 310\text{nH}$$

If the ripple voltage ends up less than that designed for, the inductor can be made smaller until the ripple value is met. This will allow optimal transient response and minimum output decoupling.

The smallest possible inductor should be used to minimize the number of output capacitors. Choosing a 300 nH inductor is a good choice for a starting point, and it gives a calculated ripple current of 13.3 A, which is 61% of the full load current of 21.7 A. The inductor should not saturate at the peak current of 29 A, and should be able to handle the sum of the power dissipation caused by the average current of 22 A in the winding and the core loss.

Another important factor in the inductor design is the DCR, which is used for measuring the phase currents. A large DCR will cause excessive power losses, while too small a value will lead to increased measurement error. A good rule of thumb is to have the DCR be about 1 to 1½ times the droop resistance ( $R_O$ ).

ADP3168

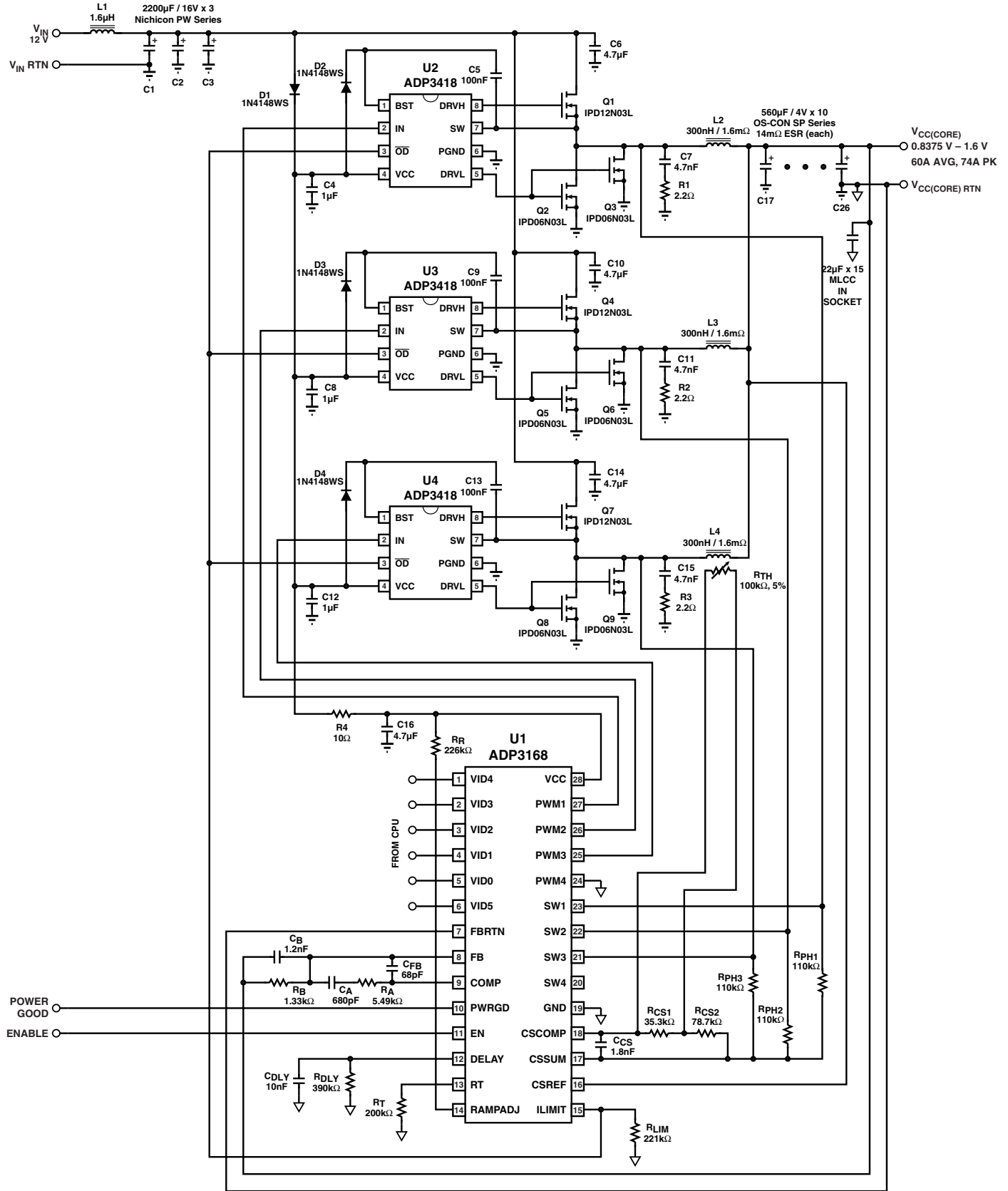


Figure 5. 65 A Intel Pentium 4 CPU Supply Circuit, VRD 10 Design

**Designing an Inductor**

Once the inductance and DCR are known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. It is also important to have the inductance and DCR tolerance specified to keep the accuracy of the system controlled. Using 15% for the inductance and 8% for the DCR (at room temperature) are reasonable tolerances that most manufacturers can meet.

The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-M $\mu$ <sup>®</sup> from Magnetics, Inc. or Micrometals) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

The best choice for a core geometry is a closed-loop types, such as pot cores, PQ, U, and E cores, or toroids. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table II gives some examples.

**Table II. Magnetics Design References**

Magnetic Designer Software Intusoft ( <a href="http://www.intusoft.com">http://www.intusoft.com</a> )
Designing Magnetic Components for High-Frequency DC-DC Converters McLyman, Kg Magnetics ISBN 1-883107-00-08

**Selecting a Standard Inductor**

The companies listed in Table III can provide design consultation and deliver power inductors optimized for high power applications upon request.

**Table III. Power Inductor Manufacturers**

Coilcraft (847)639-6400 <a href="http://www.coilcraft.com">http://www.coilcraft.com</a>
Coiltronics (561)752-5000 <a href="http://www.coiltronics.com">http://www.coiltronics.com</a>
Sumida Electric Company (510) 668-0660 <a href="http://www.sumida.com">http://www.sumida.com</a>

**Output Droop Resistance**

The design requires that the regulator output voltage measured at the CPU pins drops when the output current increases. The specified voltage drop corresponds to a DC output resistance ( $R_O$ ).

The output current is measured by summing together the voltage across each inductor and then passing the signal through a low-pass filter. This summer-filter is the CS amplifier configured with resistors  $R_{PH(X)}$  (summers), and  $R_{CS}$  and  $C_{CS}$  (filter). The output resistance of the regulator is set by the following equations, where  $R_L$  is the DCR of the output inductors:

$$R_O = \frac{R_{CS}}{R_{PH(X)}} \times R_L \tag{5}$$

$$C_{CS} = \frac{L}{R_L \times R_{CS}} \tag{6}$$

One has the flexibility of choosing either  $R_{CS}$  or  $R_{PH(X)}$ . It is best to start with  $R_{PH(X)}$  in the range of 100 - 200 k $\Omega$ , then solve for  $R_{CS}$  by rearranging Equation 5. Using 100 k $\Omega$  for  $R_{PH(X)}$ :

$$R_{CS} = \frac{R_O}{R_L} \times R_{PH(X)}$$

$$R_{CS} = \frac{1.5m\Omega}{1.6m\Omega} \times 100k\Omega = 93.8k\Omega$$

Next, use equation 6 to solve for  $C_{CS}$ :

$$C_{CS} = \frac{300nH}{1.6m\Omega \times 93.8k\Omega} = 2.0nF$$

The closest standard value for  $C_{CS}$  is 1.8 nF. If the calculated value does not happen to be a standard value, then recalculate for the closest 1% resistor values for  $R_{CS}$  and  $R_{PH(X)}$  using the final selected value for  $C_{CS}$ . This can be quickly calculated by multiplying the original values of  $R_{CS}$  and  $R_{PH(X)}$  by the ratio of the calculated  $C_{CS}$  to the actual value used. For best accuracy,  $C_{CS}$  should be a 5% or 10% NPO capacitor. For this example, the actual values used for  $R_{CS}$  and  $R_{PH(X)}$  are 104.2 k $\Omega$  and 111.1 k $\Omega$ . The closest standard 1% value for  $R_{PH(X)}$  110 k $\Omega$ .  $R_{CS}$  will be used later and should not be rounded at this time.

**Inductor DCR Temperature Correction**

With the inductor's DCR being used as the sense element, and copper wire being the source of the DCR, one needs to compensate for temperature changes of the inductor's winding. Fortunately, copper has a well-known temperature coefficient (TC) of 0.39%/°C.

If  $R_{CS}$  is designed to have an opposite and equal percentage change in resistance to that of the wire, it will cancel the temperature variation of the inductor's DCR. Due to the nonlinear nature of NTC thermistors, resistors  $R_{CS1}$  and  $R_{CS2}$  are needed (see Figure 6) to linearize the NTC and produce the desired temperature tracking.

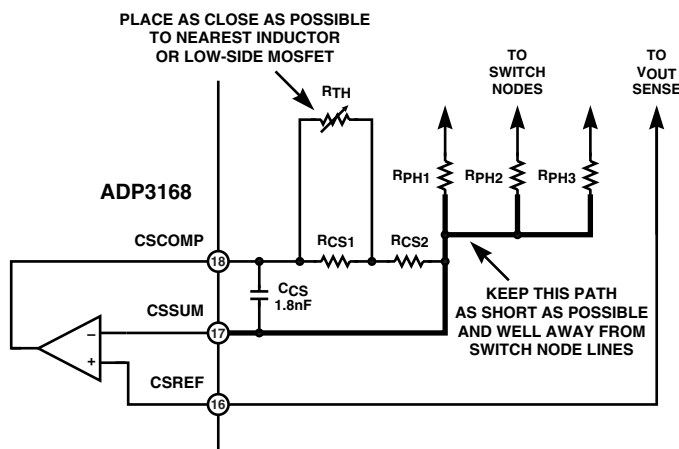


Figure 6. Temperature Compensation Circuit Values

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The following procedure and expressions will yield values to use for  $R_{CS1}$ ,  $R_{CS2}$ , and  $R_{TH}$  (the thermistor value at 25°C) for a given  $R_{CS}$  value.

1. Select an NTC to be used based on type and value. Since we do not have a value yet, start with a thermistor with a value close to  $R_{CS}$ . The NTC should also have an initial tolerance of better than 5%.
2. Based on the type of NTC, find its relative resistance value at two temperatures. The temperatures to use that work well are 50°C and 90°C. We will call these resistance values A (A is  $R_{TH(50°C)}/R_{TH(25°C)}$ ) and B (B is  $R_{TH(90°C)}/R_{TH(25°C)}$ ). Note that the NTC's relative value is always 1 at 25°C.
3. Next, find the relative value of  $R_{CS}$  required for each of these temperatures. This is based on the percentage change needed, which we will initially make 0.39%/°C. We will call these  $r_1$  ( $r_1$  is  $1/(1 + TC \times (T_1 - 25))$ ) and  $r_2$  ( $r_2$  is  $1/(1 + TC \times (T_2 - 25))$ ), where  $TC=0.0039$ ,  $T_1 = 50°C$  and  $T_2 = 90°C$ .

4. Compute the relative values for  $R_{CS1}$ ,  $R_{CS2}$ , and  $R_{TH}$  using:

$$r_{CS2} = \frac{(A - B) \times r_1 \times r_2 - A \times (1 - B) \times r_2 + B \times (1 - A) \times r_1}{A \times (1 - B) \times r_1 - B \times (1 - A) \times r_2 - (A - B)}$$

$$r_{CS1} = \frac{(1 - A)}{1 - r_{CS2} - \frac{A}{r_1 - r_{CS2}}}$$

$$r_{TH} = \frac{1}{\frac{1}{1 - r_{CS2}} - \frac{1}{r_{CS1}}}$$
(7)

5. Calculate  $R_{TH} = r_{TH} \times R_{CS}$ , then select the closest value of thermistor available. Also compute a scaling factor  $k$  based on the ratio of the actual thermistor value used relative to the computed one:

$$k = \frac{R_{TH(ACTUAL)}}{R_{TH(CALCULATED)}} \quad (8)$$

6. Finally, calculate values for  $R_{CS1}$  and  $R_{CS2}$  using the following:

$$R_{CS1} = R_{CS} \times k \times r_{CS1}$$

$$R_{CS2} = R_{CS} \times ((1 - k) + (k \times r_{CS2})) \quad (9)$$

For this example,  $R_{CS}$  has already been calculated in the previous section to be 104.2 kΩ, so we start with a thermistor value of 100 kΩ. Looking through available 0603 size thermistors, we find a Vishay NTHS0603N01N1003JR NTC thermistor with  $A = 0.3602$  and  $B = 0.09174$ . From these we compute  $r_{CS1} = 0.3796$ ,  $r_{CS2} = 0.7195$  and  $r_{TH} = 1.0751$ . Solving for  $R_{TH}$  yields 112.05 kΩ, so we choose 100 kΩ, making  $k = 0.8925$ . Finally, we find  $R_{CS1}$  and  $R_{CS2}$  to be 35.30 kΩ and 78.11 kΩ. Choosing the closest 1% resistor values yields a choice of 35.7 kΩ and 78.7 kΩ.

### Output Offset

Intel's specification requires that at no load the nominal output voltage of the regulator be offset to a lower value than the nominal voltage corresponding to the VID code. The offset is set by a constant current source flowing out

of the FB pin ( $I_{FB}$ ) and flowing through  $R_B$ . The value of  $R_B$  can be found using Equation 10:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}}$$

$$R_B = \frac{1.5V - 1.480V}{15\mu A} = 1.33k\Omega \quad (10)$$

The closest standard 1% resistor value is 1.33 kΩ.

### C<sub>OUT</sub> Selection

The required output decoupling for the regulator is typically recommended by Intel for various processors and platforms. One can also use some simple design guidelines to determine what is required. These guidelines are based on having both bulk and ceramic capacitors in the system.

The first thing is to select the total amount of ceramic capacitance. This is based on the number and type of capacitor to be used. The best location for ceramics is inside the socket, with 12 to 18 of size 1206 being the physical limit. Others can be placed along the outer edge of the socket as well.

Combined ceramic values of 200 - 300 μF are recommended, usually made up of multiple 10 μF or 22 μF capacitors. Select the number of ceramics and find the total ceramic capacitance ( $C_Z$ ).

Next, there is an upper limit imposed on the total amount of bulk capacitance ( $C_X$ ) when one considers the VID on-the-fly voltage stepping of the output (voltage step  $V_V$  in time  $t_V$ ) and a lower limit based on meeting the critical capacitance for load release for a given maximum load step  $I_{MAX}$ :

$$C_{X(MIN)} \geq \left( \frac{L \times I_{MAX}}{n \times R_O \times V_{VID}} - C_Z \right) \times \frac{R_X + R_O}{2 \times R_O} \quad (11)$$

$$C_{X(MAX)} \leq \left( \frac{V_{VID} \times t_V^2}{V_V \times L} - C_Z \right) \times \frac{R_X + R_O}{2 \times R_O} \quad (12)$$

where  $R_X$  is the ESR of the bulk capacitor bank. However, to meet the transient specification,  $R_X$  cannot be greater than 3 times  $R_O$ . If the  $C_{X(MIN)}$  is larger than  $C_{X(MAX)}$ , the system will not meet the VID on-the-fly specification and may require the use of a smaller inductor or more phases (and may have to increase the switching frequency to keep the output ripple the same).

For our example, twelve 22 μF 1206 MLC capacitors ( $C_Z = 264 \mu F$ ) were used. The VID-on-the-fly step change is 12.5 mV in 5 μs. Solving for the bulk capacitance, assuming that  $R_X = R_O$ , yields:

$$C_{X(MIN)} \geq \left( \frac{300nH \times 65A}{3 \times 1.5m\Omega \times 1.5V} - 264\mu F \right) \times 1 = 2.63mF$$

$$C_{X(MAX)} \leq \left( \frac{1.5V \times 5\mu s^2}{12.5mV \times 300nH} - 264\mu F \right) \times 1 = 9.74mF$$

Using ten 560 μF OSCONs with an ESR of 12 mΩ each yields  $C_X = 5.6 mF$  with an  $R_X = 1.2m\Omega$  (making the new

limits on  $C_X$  2.4 mF to 8.8 mF, which is still within the acceptable range).

One last check should be made to ensure that the ESL of the bulk capacitors ( $L_X$ ) is low enough to limit the initial high-frequency transient spike. This be tested using:

$$\begin{aligned} L_X &\leq C_Z \times R_O^2 \\ L_X &\leq 264\mu\text{F} \times 1.5\text{m}\Omega^2 = 594\text{pH} \end{aligned} \quad (13)$$

In this example,  $L_X$  is 400 pH for the ten OSCSON capacitors, which satisfies this limitation. If the  $L_X$  of the chosen bulk capacitor bank is too large, the number of MLC capacitors must be increased.

One should note for this multi-mode control technique, all-ceramic designs can be used as long as the conditions of Equations 11, 12 and 13 are satisfied.

### Power MOSFETs

For this example, the N-channel power MOSFETs have been selected for one high-side switch and two low-side switches per phase. The main selection parameters for the power MOSFETs are  $V_{GS(TH)}$ ,  $Q_G$ ,  $C_{iss}$ ,  $C_{rss}$  and  $R_{DS(ON)}$ . The minimum gate drive voltage (the supply voltage to the ADP3418) dictates whether standard threshold or logic-level threshold MOSFETs must be used. With  $V_{GATE} \sim 10$  V, logic-level threshold MOSFETs ( $V_{GS(TH)} < 2.5$  V) are recommended.

The maximum output current  $I_O$  determines the  $R_{DS(ON)}$  requirement for the low-side (synchronous) MOSFETs. With the ADP3168, currents are balanced between phases, thus the current in each low-side MOSFET is the output current divided by the total number of MOSFETs ( $n_{SF}$ ). With conduction losses being dominant, the following expression shows the total power being dissipated in each synchronous MOSFET in terms of the ripple current per phase ( $I_r$ ) and average total output current ( $I_O$ );

$$P_{SF} = (1 - D) \times \left[ \left( \frac{I_O}{n_{SF}} \right)^2 + \frac{1}{12} \times \left( \frac{n \times I_R}{n_{SF}} \right)^2 \right] \times R_{DS(SF)} \quad (14)$$

Knowing the maximum output current being designed for and the maximum allowed power dissipation, one can find the required  $R_{DS(ON)}$  for the MOSFET. For D-PAK MOSFETs up to an ambient temperature of 50°C, a safe limit for  $P_{SF}$  is 1 W (assuming 2 D-paks) at 120°C junction temperature. Thus, for our example (65 A maximum), we find  $R_{DS(SF)}$  (per MOSFET)  $< 8.7$  mΩ. This  $R_{DS(SF)}$  is also at a junction temperature of about 120°C, so we need to make sure we account for this when making this selection.

Another important factor for the synchronous MOSFET is the input capacitance and feedback capacitance. The ratio of the feedback to input needs to be small (less than 10% is recommended) to prevent accidental turn-on of the synchronous MOSFETs when the switch node goes high.

Also, the time to switch the synchronous MOSFETs off should not exceed the non-overlap dead time of the MOSFET driver (40 ns typical for the ADP3418). The output impedance of the driver is about 2 Ω and the typical MOSFET input gate resistances are about 1 - 2 Ω, so a total gate capacitance of less than 6000 pF should be

adhered to. Since there are two MOSFETs in parallel, we should limit the input capacitance for each synchronous MOSFET to 3000 pF.

The high-side (main) MOSFET has to be able to handle two main power dissipation components; conduction and switching losses. The switching loss is related to the amount of time it takes for the main MOSFET to turn on and off, and to the current and voltage that are being switched. Basing the switching speed on the rise and fall time of the gate driver impedance and MOSFET input capacitance, the following expression provides an approximate value for the switching loss per main MOSFET, where  $n_{MF}$  is the total number of main MOSFETs:

$$P_{S(MF)} = 2 \times f_{SW} \times \frac{V_{CC} \times I_O}{n_{MF}} \times R_G \times \frac{n_{MF}}{n} \times C_{iss} \quad (15)$$

Here,  $R_G$  is the total gate resistance (2 Ω for the ADP3418 and about 1 Ω for typical high speed switching MOSFETs, making  $R_G = 3$  Ω) and  $C_{iss}$  is the input capacitance of the main MOSFET. It is interesting to note that adding more main MOSFETs ( $n_{MF}$ ) does not really help the switching loss per MOSFET since the additional gate capacitance slows down switching. The best thing to reduce switching loss is to use lower gate capacitance devices.

The conduction loss of the main MOSFET is given by the following, where  $R_{DS(MF)}$  is the ON-resistance of the MOSFET:

$$P_{C(MF)} = D \times \left[ \left( \frac{I_O}{n_{MF}} \right)^2 + \frac{1}{12} \times \left( \frac{n \times I_R}{n_{MF}} \right)^2 \right] \times R_{DS(MF)} \quad (16)$$

Typically, for main MOSFETs, one wants the highest speed (low  $C_{iss}$ ) device, but these usually have higher ON-resistance. One must select a device that meets the total power dissipation (about 1.5 W for a single D-PAK) when combining the switching and conduction losses.

For our example, we have selected an Infineon IPD12N03L as the main MOSFET (three total;  $n_{MF} = 3$ ), with a  $C_{iss} = 1460$  pF (max) and  $R_{DS(MF)} = 14$  mΩ (max at  $T_j = 120^\circ\text{C}$ ) and an Infineon IPD06N03L as the synchronous MOSFET (six total;  $n_{SF} = 6$ ), with  $C_{iss} = 2370$  pF (max) and  $R_{DS(SF)} = 8.3$  mΩ (max at  $T_j = 120^\circ\text{C}$ ). The synchronous MOSFET  $C_{iss}$  is less than 3000 pF, satisfying that requirement. Solving for the power dissipation per MOSFET at  $I_O = 65$  A and  $I_R = 13$  A yields 900 mW for each synchronous MOSFET and 1.6 W for each main MOSFET. These numbers work well considering there is usually more PCB area available for each main MOSFET versus each synchronous MOSFET.

One last thing to look at is the power dissipation in the driver for each phase. This is best described in terms of the  $Q_G$  for the MOSFETs and is given by the following, where  $Q_{GMF}$  is the total gate charge for each main MOSFET and  $Q_{GSF}$  is the total gate charge for each synchronous MOSFET:

$$P_{DRV} = \left[ \frac{f_{SW}}{2 \times n} \times (n_{MF} \times Q_{GMF} + n_{SF} \times Q_{GSF}) + I_{CC} \right] \times V_{CC} \quad (17)$$

Also shown is the standby dissipation factor ( $I_{CC}$  times the  $V_{CC}$ ) for the driver. For the ADP3418, the maximum dissipation should be less than 400 mW. For our example,

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with  $I_{CC} = 7 \text{ mA}$ ,  $Q_{GMF} = 22.8 \text{ nC}$  and  $Q_{GSF} = 34.3 \text{ nC}$ , we find 260 mW in each driver, which is below the 400 mW dissipation limit.

### Ramp Resistor Selection

The ramp resistor ( $R_R$ ) is used for setting the size of the internal PWM ramp. The value of this resistor is chosen to provide the best combination of thermal balance, stability, and transient response. The following expression is used for determining the optimum value:

$$R_R = \frac{A_R \times L}{3 \times A_D \times R_{DS} \times C_R}$$

$$R_R = \frac{0.2 \times 300\text{nH}}{3 \times 5 \times 3.5\text{m}\Omega \times 5\text{pF}} = 228.6\text{k}\Omega \quad (18)$$

where  $A_R$  is the internal ramp amplifier gain,  $A_D$  is the current balancing amplifier gain,  $R_{DS}$  is the total low-side MOSFET ON-resistance, and  $C_R$  is the internal ramp capacitor value. The closest standard 1% resistor value is 226 k $\Omega$ .

The internal ramp voltage magnitude can be calculated using:

$$V_R = \frac{A_R \times (1-D) \times V_{VID}}{R_R \times C_R \times f_{SW}}$$

$$V_R = \frac{0.2 \times (1-0.125) \times 1.5\text{V}}{226\text{k}\Omega \times 5\text{pF} \times 330\text{kHz}} = 0.7\text{V} \quad (19)$$

The size of the internal ramp can be made larger or smaller. If it is made larger, stability and transient response will improve, but thermal balance will degrade. Likewise, if the ramp is made smaller, thermal balance will improve at the sacrifice of transient response and stability. The factor of three in the denominator of equation 18 sets a ramp size that gives an optimal balance for good stability, transient response, and thermal balance.

### Current Limit Set Point

To select the current limit set point, we need to find the resistor value for  $R_{LIM}$ . The current limit threshold for the ADP3168 is set with a 3V source ( $V_{LIM}$ ) across  $R_{LIM}$  with a gain of 10 mV/ $\mu\text{A}$  ( $A_{LIM}$ ).  $R_{LIM}$  can be found using the following:

$$R_{LIM} = \frac{A_{LIM} \times V_{LIM}}{I_{LIM} \times R_O} \quad (20)$$

Here,  $I_{LIM}$  is the average current limit for the output of the supply. For our example, choosing 90 A for  $I_{LIM}$ , we find  $R_{LIM}$  to be 222.2 k $\Omega$ , for which we chose 221 k $\Omega$  as the nearest 1% value.

The per phase current limit described earlier has its limit determined by the following:

$$I_{PHLIM} \cong \frac{V_{COMP(MAX)} - V_R - V_{BIAS}}{A_D \times R_{DS(MAX)}} \quad (21)$$

For the ADP3168, the maximum COMP voltage ( $V_{COMP(MAX)}$ ) is 3.3 V, the COMP pin bias voltage ( $V_{BIAS}$ ) is 1.2V, and the current balancing amplifier gain ( $A_D$ ) is 5. Using  $V_R$  of 0.7 V, and  $R_{DS(MAX)}$  of 5.3 m $\Omega$  (low-side ON-resistance at 150 $^\circ\text{C}$ ), we find a per-phase limit of 52 A.

This limit can be adjusted by changing the ramp voltage  $V_R$ . But make sure not to set the per-phase limit lower than the average per-phase current ( $I_{LIM}/n$ ).

### Feedback Loop Compensation Design

Optimized compensation of the ADP3168 allows the best possible response of the regulator's output to a load change. The basis for determining the optimum compensation is to make the regulator and output decoupling appear as an output impedance that is entirely resistive over the widest possible frequency range, including DC, and equal to the droop resistance ( $R_O$ ). With the resistive output impedance, the output voltage will droop in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output decoupling.

With the multi-mode feedback structure of the ADP3168, one needs to set the feedback compensation to make the converter's output impedance working in parallel with the output decoupling meet this goal. There are several poles and zeros created by the output inductor and decoupling capacitors (output filter) that need to be compensated for.

A type-three compensator on the voltage feedback is adequate for proper compensation of the output filter. The expressions given below are simplified for ease of use. A design spreadsheet is available for doing the exact math involved for the designer who wishes to achieve more accurate values for the compensator components based on the system design.

The first step is to compute the time constants for all of the poles and zeros in the system:

$$R_e = n \times R_O + A_D \times R_{DS} + R_L \times \frac{V_R}{V_{VID}}$$

$$R_e = 3 \times 1.5\text{m}\Omega + 5 \times 3.5\text{m}\Omega + 1.6\text{m}\Omega \times \frac{0.7\text{V}}{1.5\text{V}} \quad (22)$$

$$R_e = 22.7\text{m}\Omega$$

$$T_a = C_X \times (R_O - R') + \frac{L_X}{R_O}$$

$$T_a = 5.6\text{mF} \times (1.5\text{m}\Omega - 0.6\text{m}\Omega) + \frac{400\text{pH}}{1.5\text{m}\Omega} = 5.3\mu\text{s} \quad (23)$$

$$T_b = (R_X + R' - R_O) \times C_X$$

$$T_b = (1.2\text{m}\Omega + 0.6\text{m}\Omega - 1.5\text{m}\Omega) \times 5.6\text{mF} = 1.68\mu\text{s} \quad (24)$$

$$T_c = \frac{V_R \times L}{V_{VID} \times R_e}$$

$$T_c = \frac{0.7\text{V} \times 300\text{nH}}{1.5\text{V} \times 22.7\text{m}\Omega} = 6.2\mu\text{s} \quad (25)$$

$$T_d = \frac{C_X \times L_X}{T_a} \times \left(1 + \frac{R_X}{R_O}\right)$$

$$T_d = \frac{5.6\text{mF} \times 400\text{pH}}{5.3\mu\text{s}} \times \left(1 + \frac{1.2\text{m}\Omega}{1.5\text{m}\Omega}\right) = 761\text{ns} \quad (26)$$

where, for the ADP3168,  $R'$  is the PCB resistance from the bulk capacitors to the ceramics and where  $R_{DS}$  is *approximately* the total low-side MOSFET ON-resistance

per phase at 25°C. For this example,  $A_D$  is 5,  $V_R$  equals 1 V,  $R'$  is approximately 0.6 mΩ (assuming a 4-layer motherboard) and  $L_X$  is 400 pH for the ten OSCSON capacitors.

The compensation values can then be solved for using the following:

$$C_A = \frac{n \times R_O \times T_a}{R_c \times R_B} \quad (27)$$

$$C_A = \frac{3 \times 1.5\text{m}\Omega \times 5.3\mu\text{s}}{22.7\text{m}\Omega \times 1.33\text{k}\Omega} = 790\text{pF} \quad (27)$$

$$R_A = \frac{T_c}{C_A} = \frac{6.2\mu\text{s}}{790\text{pF}} = 7.85\text{k}\Omega \quad (28)$$

$$C_B = \frac{T_b}{R_B} = \frac{1.68\mu\text{s}}{1.33\text{k}\Omega} = 1.26\text{nF} \quad (29)$$

$$C_{FB} = \frac{T_d}{R_A} = \frac{76\text{lns}}{7.85\text{k}\Omega} = 96.9\text{pF} \quad (30)$$

Choosing the closest standard values for these components yields:  $C_A = 820$  pF,  $R_A = 7.87$  kΩ,  $C_B = 1.2$  nF, and  $C_{FB} = 100$  pF. These make a good starting point.

Using the design spreadsheet will yield more optimal compensation values; from the spreadsheet,  $C_A = 680$  pF,  $R_A = 5.49$  kΩ,  $C_B = 1.2$  nF, and  $C_{FB} = 68$  pF.

Figure 7 shows the typical transient response using each set of compensation values. It can be seen that both do an adequate job, with the spreadsheet values performing slightly better.

#### $C_{IN}$ Selection and Input Current di/dt Reduction

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to  $n \times V_{OUT}/V_{IN}$  and an amplitude of one-nth of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{Crms} = D \times I_O \times \sqrt{\frac{1}{n \times D} - 1} \quad (31)$$

$$I_{Crms} = .125 \times 65\text{A} \times \sqrt{\frac{1}{3 \times .125} - 1} = 10.5\text{A}$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 2200 μF, 16 V Nichicon capacitors with a ripple current rating of 3.5 A each.

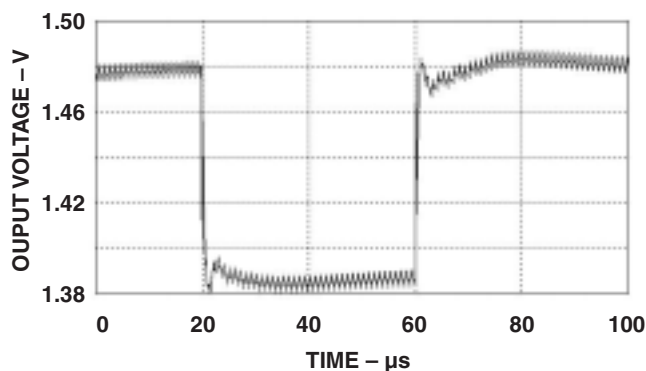
To reduce the input-current di/dt to below the recommended maximum of 0.1 A/μs, an additional small inductor ( $L > 1$  μH @ 15 A) should be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

#### LAYOUT AND COMPONENT PLACEMENT

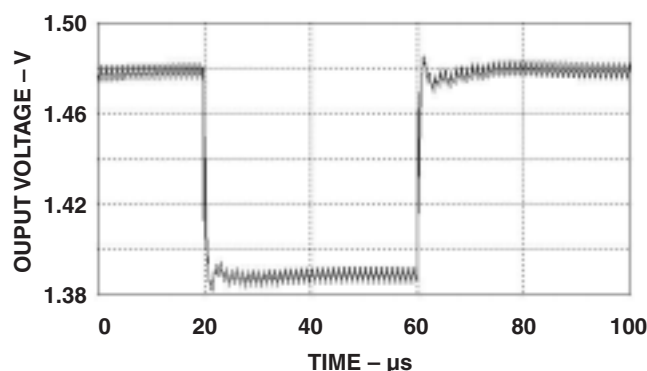
The following guidelines are recommended for optimal performance of a switching regulator in a PC system. Key layout issues are illustrated in Figure 8.

##### General Recommendations

1. For good results, at least a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input, and output power, and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the output voltage sense lines of the ADP3168) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces



(a)



(b)

Figure 7. Comparison of Transient Response of Compensation Components Chose Using (a) Simplified Calculations, and (b) Spreadsheet Detailed Equations.



## ADP3168

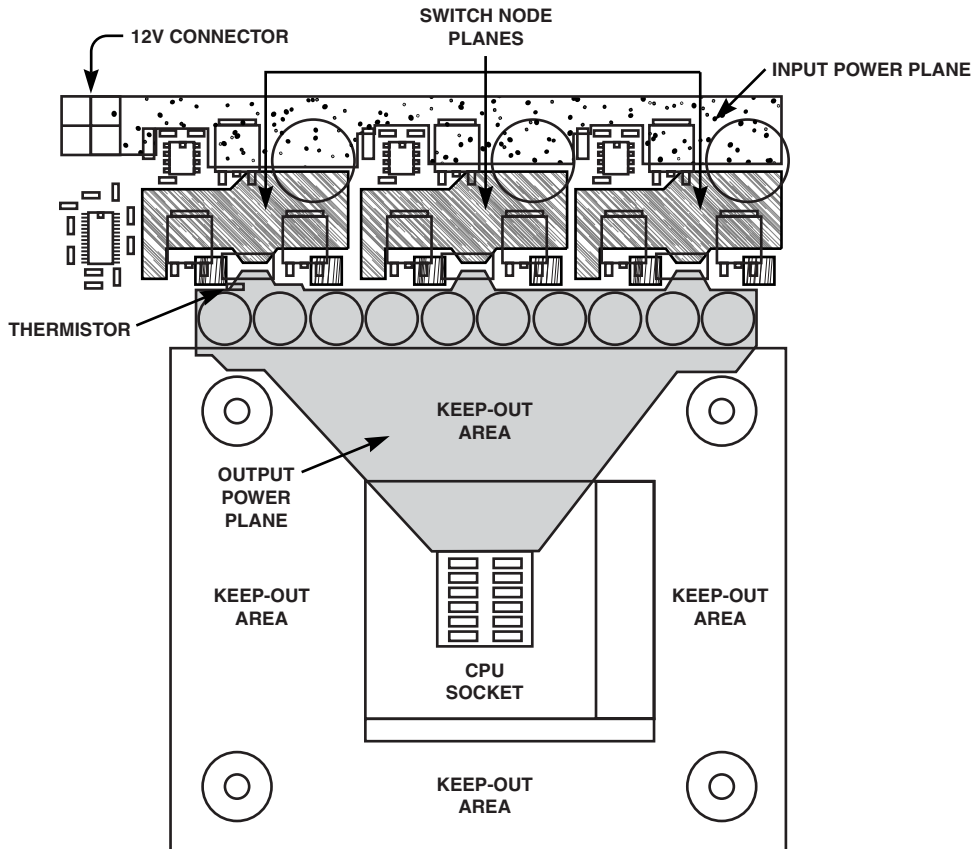


Figure 8. Layout Recommendations

of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

4. An analog ground plane should be used around and under the ADP3168 for referencing the components associated with the controller to. This plane should be tied to the nearest output decoupling capacitor ground and should not tie to any other power circuitry to prevent power currents from flowing in it.
5. The components around the ADP3168 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. Refer to Figure 6 for more details on layout for the CSSUM node.
6. The output capacitors should be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.
7. Avoid crossing any signal lines over the switching power path loop, described below.

#### Power Circuitry

8. The switching power path should be routed on the PCB to encompass the shortest possible length in order to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.
9. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat

to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, the largest possible pad area should be used.

10. The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.
11. For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

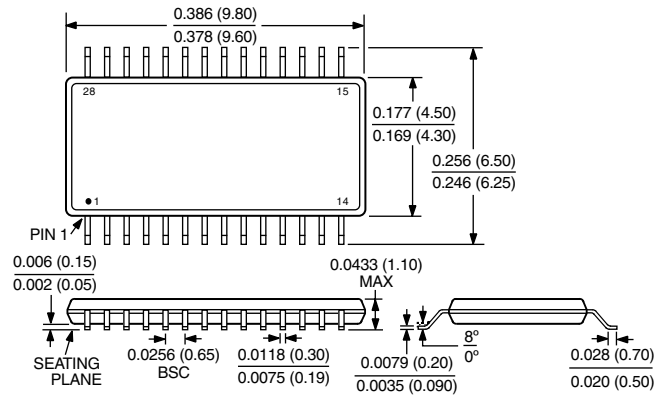
#### **Signal Circuitry**

12. The output voltage is sensed and regulated between the FB pin and the FBRTN pin (which connects to the signal ground at the load). In order to avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB and FBRTN traces should be routed adjacent to each other atop the power ground plane back to the controller.
13. The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

ADP3168

**OUTLINE DIMENSIONS**  
 Dimensions shown in inches and (mm).

**28-Lead TSSOP**  
**RU-28**



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