Intel® 855PM Chipset Memory Controller Hub (MCH) DDR 200/266 MHz

Datasheet

March 2003

Order Number: 252613-001

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Revision History

Document No.	Rev. No.	Description	Date
252613	001	Initial release	March 2003

Intel® 855PM MCH

Product Features

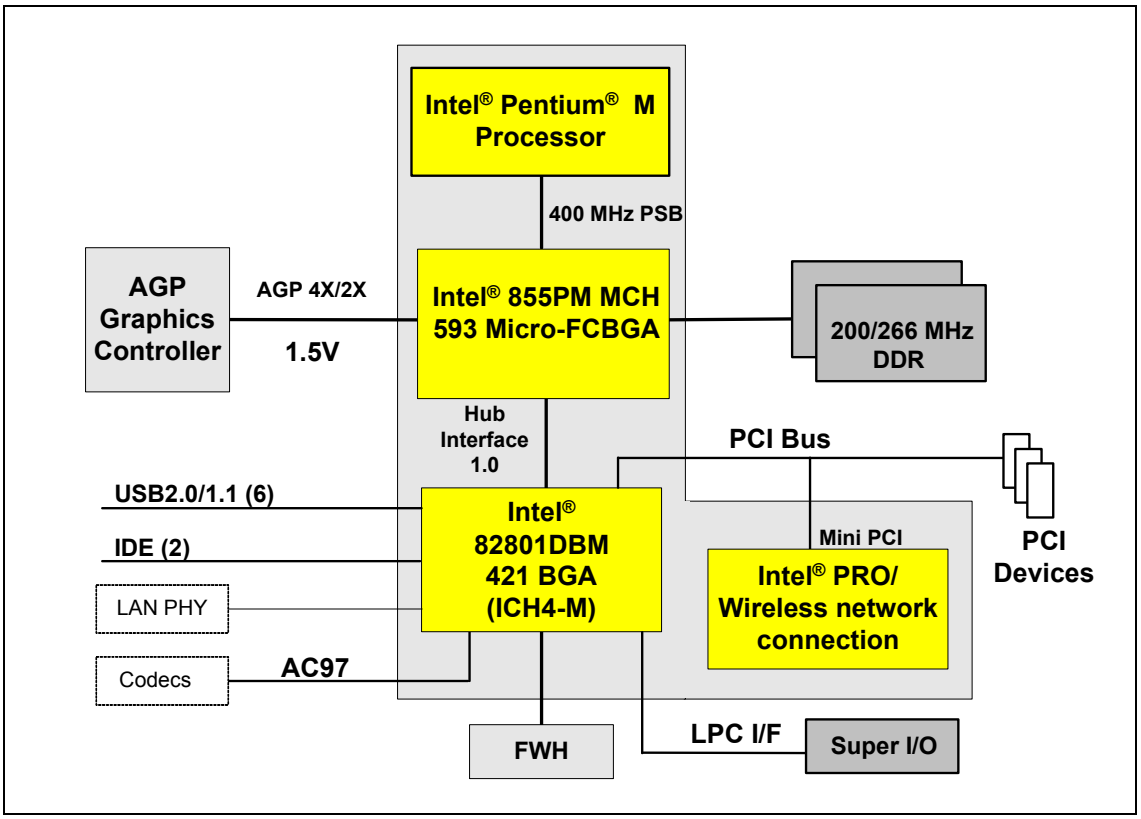
- Processor/Host Bus Support
  - —Supports the Intel® Pentium® M processor
  - —2x Address, 4x Data
  - —Supports system bus at 400 MT/s
  - — Supports host bus Dynamic Bus Inversion (DBI)
  - —Supports 32-bit host bus addressing
  - —12 deep In-Order Queue
  - — AGTL+ bus driver technology with integrated GTL termination resistors and low voltage operation (1.05 V)
  - — Support for DPWR# signal to Intel® Pentium® M processor for PSB power management
- Memory System
  - —Directly supports one DDR channel, 64b wide (72b with ECC)
  - — Supports 200-MHz and 266-MHz DDR devices
  - — Supports 64-Mb, 128-Mb, 256-Mb, and 512-Mb technologies for x16 devices and x8 devices.
  - — All supported devices have four banks
  - — Configurable optional ECC operation (single bit Error Correction and multiple bit Error Detection)
  - — Supports up to 16 simultaneous open pages
  - — Supports page sizes of 2 kB, 4 kB, 8 kB, and 16 kB. Page size is individually selected for every row.
  - — Thermal throttling scheme to selectively throttle reads and/or writes. Throttling can be triggered by preset read/write bandwidth limits.
  - — For DDR, Max of two, double-sided SO-DIMMs (four rows populated) with unbuffered PC1600/PC2100 DDR (with or without ECC)
  - — By using stacked 512-Mb technology, the largest memory capacity possible is 2.0 GB
- System Interrupts
  - —Supports 8259 and processor system bus interrupt delivery mechanism
  - — Supports interrupts signaled as upstream Memory Writes from AGP/PCI (PCI semantics only) and hub interface
  - —MSI sent to the CPU through the System
- Accelerated Graphics Port (AGP) Interface
  - — Supports a single AGP device (either through a connector or on the motherboard)
  - —AGP Support
  - —Supports AGP 2.0 including 1x, 2x, and 4x AGP data transfers and 2x/4x Fast Write protocol
  - —Supports only 1.5-V AGP electricals
  - —32 deep AGP request queue
  - —PCI semantic (FRAME# initiated) accesses to DRAM are snooped
  - —AGP semantic (PIPE# and SBA) accesses to DRAM are not snooped
  - —High priority access support
  - —Hierarchical PCI configuration mechanism
  - —Delayed transaction support for AGP-to-DRAM FRAME# semantic reads that can not be serviced immediately
  - —32-bit upstream address support for inbound AGP and PCI cycles
  - —32-bit downstream address support for outbound PCI and Fast Write cycles
  - —AGP Busy/Stop Protocol
  - —AGP Clamping and Sense Amp Control
- Hub Interface to ICH4-M
  - —266 MB/s point-to-point hub interface to ICH4-M
  - —66-MHz base clock
  - —Supports the following traffic types to the ICH4-M
    - —Hub interface-to-AGP memory writes
    - —Hub interface-to-DRAM
    - —CPU-to-hub interface
    - —Messaging
      - —MSI Interrupt messages
      - —Power Management state change
      - —SMI, SCI, and SERR error indication
- Power Management
  - —SMRAM space remapping to A0000h (128 kB)
  - —Supports extended SMRAM space above 256 MB, additional 128k/256k/512k/1 MB TSEG from Top of Memory, cacheable (cacheability controlled by CPU)
  - —APM Rev 1.2 compliant power management
  - —Suspend to System Memory

Bus
— From IOxAPIC in ICH4-M
— Supports peer MSI between hub interface and AGP
— Provides redirection for upstream interrupts to the System Bus

— ACPI 1.0b, 2.0 Support
— Enhanced Intel SpeedStep® Technology Support
— Cache coherency with CPU in sleep mode
— Dynamic Memory Power-down

- Package
  - — Package options
  - — 593-pin Micro-FCBGA (37.5 x 37.5 mm)

Simplified Block Diagram



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1. Introduction

Intel® Centrino™ mobile technology with integrated wireless LAN capabilities was designed specifically for wireless notebook PCs – delivering outstanding mobile performance and enabling extended battery life and thinner, lighter designs.*

The Intel® 855PM Memory Controller Hub (MCH) is an Intel® Centrino™ mobile technology component. The MCH manages the flow of information between its four interfaces: the processor side bus (communication with the Intel® Pentium® M processor), memory interface, AGP interface, and hub interface. The MCH arbitrates between the four interfaces when each initiates an operation. The Intel® 855PM memory controller hub (MCH) is designed for use with the Intel® Pentium® M processor. The MCH supports data coherency via snooping and must perform address translation for access to AGP Aperture memory. To increase system performance, the MCH incorporates several queues.

The Intel® 855PM MCH may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. This information will be available in Specification Updates.

* Wireless connectivity and some features may require you to purchase additional software, services or external hardware. Availability of public wireless LAN access points limited. System performance measured by MobileMark* 2002. System performance, battery life, wireless performance and functionality will vary depending on your specific hardware and software configurations. See http://www.intel.com/products/centrino/more_info for more information.

1.1. Reference Documents

Document	Document Number/Location
Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide	www.developer.intel.com
Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet	www.developer.intel.com
Intel® Pentium® M Processor Datasheet	www.developer.intel.com
Intel® DDR200 JEDEC Specification Addendum, Revision 1.0	www.developer.intel.com
Intel® DDR266 JEDEC Specification Addendum, Revision 0.9	www.developer.intel.com
JEDEC Double Data Rate (DDR) SDRAM Specification, Revision 2.0	www.jedec.org
JEDEC PC2100 DDR SDRAM Un-buffered SO-DIMM Reference Design Specification (includes PC1600 DDR SDRAM)	www.jedec.org
Accelerated Graphics Port Interface Specification Rev 2.0	http://www.agpforum.org/
PCI Local Bus Specification Rev. 2.2	www.pcisig.com
PCI-PCI Bridge Specification Rev. 1.0	www.pcisig.com
PCI Bus Power Management Interface Specification Rev. 1.0	www.pcisig.com
Advanced Configuration and Power Interface Specification (ACPI) Rev. 1.0b	www.teleport.com/~acpi/

NOTE: See *Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide* for an expanded set of related documents.

1.2. Terminology

Term	Description
MCH	The Mobile Memory Controller Hub component that contains the processor interface, DRAM controller, and AGP interface. It communicates with the I/O controller hub (ICH4-M) and other IO controller hubs over proprietary interconnect called the hub interface.
ICH4-M	The Mobile I/O Controller Hub 4-M component that contains the primary PCI interface, LPC interface, USB, ATA-100, AC'97, and other IO functions. It communicates with the Intel® 855PM MCH over a proprietary interconnect called the hub interface.
Host	This term is used synonymously with processor.
Core -	The internal base logic in the MCH.
System Bus	Processor-to-MCH interface. The Enhanced Mode of the Scalable Bus supports source synchronous transfers for address and data, and system bus interrupt delivery. The Intel® Pentium® M processor implements a subset of Enhanced mode.
Hub interface	The proprietary hub interconnect that ties the MCH to the ICH4-M. In this document hub interface cycles originating from or destined for the primary PCI interface on the ICH4-M are generally referred to as hub interface cycles.
Accelerated Graphics Port (AGP)	Refers to the AGP interface that is in the MCH. It supports AGP 2.0 compliant components only with 1.5-V signaling level. PIPE# and SBA addressing cycles and their associated data phases are generally referred to as AGP transactions. FRAME# cycles over the AGP bus are generally referred to as AGP/PCI transactions.
PCI_A	The physical PCI bus, driven directly by the ICH4-M component. It supports 5-V, 32-bit, 33-MHz PCI 2.2 compliant components. Communication between PCI_A and MCH occurs over hub interface. **NOTE**: Even though it is referred to as PCI_A it is not PCI Bus #0 from a configuration standpoint.
Full Reset	A Full MCH Reset is defined in this document when RSTIN# is asserted.
System Bus	Synonymous with Host or Processor System Bus
GART	Graphics Aperture Re-map Table. This table contains the page re-map information used during AGP aperture address translations.
GTLB	Graphics Translation Look-aside Buffer. A cache used to store frequently used GART entries.
DBI	Dynamic Bus inversion
MSI	Message Signaled Interrupts. MSI's allow a device to request interrupt service via a standard Memory Write transaction instead of through a hardware signal.
IPI	Inter Processor Interrupt

1.3. System Architecture

The Intel® 855PM Memory Controller Hub (MCH) component provides the processor interface, DRAM interface, AGP interface, and hub interface in an Intel® 855PM chipset platform.

The Intel® 855PM MCH is in a 593-pin Micro-FCBGA package and contains the following functionality:

- The Intel® 855PM MCH is optimized for the Intel® Pentium® M processor
- Supports a single channel of DDR memory
- Contains advanced power management logic
- Supports single Intel® Pentium® M processor configurations at 400 MT/s
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- Up to 2.0 GB (with stacked 512-Mb technology and two SO-DIMMs) of PC1600/2100 DDR with ECC
- 1.5-V AGP interface with up to 4x SBA/PIPE# mode data transfer and up to 4x fast write capability
- 1.8-V, 8-bit, 66-MHz 4x hub interface to ICH4-M
- Deeper Sleep state support
- Enhanced Intel SpeedStep® technology
- Distributed arbitration for highly concurrent operation

1.4. Processor Host Interface

The Intel® 855PM MCH is optimized for the Intel® Pentium® M processor. Some of the key features for this interface are:

- Source synchronous double pumped address
- Source synchronous quad pumped data
- System bus interrupt and side-band signal delivery

The MCH supports a 64-B cache line size. Only one processor is supported at a system bus frequency of 400 MT/s. The MCH integrates AGTL+ termination resistors on all of the AGTL+ signals. The MCH supports 32-bit host addresses, allowing the CPU to access the entire 4 GB of the MCH memory address space.

The MCH has a 12-deep, In-Order Queue to support up to 12 outstanding pipelined address requests on the host bus. The MCH drives DPWR# signal to Intel® Pentium® M processor, which can then disable its sense amps. The MCH supports two outstanding defer cycles at a time; however, only one to any particular IO interface. Host initiated I/O cycles are positively decoded to AGP/PCI or MCH configuration space and subtractively decoded to the hub interface. Host initiated memory cycles are positively decoded to AGP/PCI or DRAM. AGP semantic memory accesses initiated from AGP/PCI to DRAM are not snooped on the host bus. Memory accesses initiated from AGP/PCI using PCI semantics and from the hub interface to DRAM will be snooped on the System bus. Memory accesses whose

addresses lie within the AGP aperture are translated using the AGP address translation table, regardless of the originating interface.

1.4.1. Host Bus Error Checking

The Intel® 855PM MCH does not generate, nor check parity for Data, Address/Request, and Response signals on the processor bus.

1.5. DRAM Interface

The Intel® 855PM MCH directly supports one channel of PC1600/2100 SO-DIMM DDR memory. The Intel® 855PM MCH memory interface supports DDR devices with densities of 64-Mb, 128-Mb, 256-Mb, and 512-Mb technology. The maximum memory support is two stacked, double-sided SO-DIMMs (4 rows populated). The Intel® 855PM MCH memory interface also supports variable page sizes of 2 kB, 4 kB, 8 kB, and 16 kB. Page size is individually selected for every row and a maximum of 16 pages may be opened simultaneously.

Table 1. DDR Memory Capacity

Technology	Width	System Memory Capacity	System Memory Capacity with Stacked Memory
64 Mb	16	128 MB	-
128 Mb	16	256 MB	-
256 Mb	16	512 MB	-
512 Mb	16	1 GB	-
64 Mb	8	128 MB	256 MB
128 Mb	8	256 MB	512 MB
256 Mb	8	512 MB	1 GB
512 Mb	8	1 GB	2 GB

The memory interface provides optional ECC error checking for DRAM data integrity. During DRAM writes, ECC is generated on a QWORD (64 bit) basis. Because the Intel® 855PM MCH stores only entire cache lines in its internal buffers, partial QWORD writes initially cause a read of the underlying data, and their write-back into memory is no different from that of a complete cache line. During DRAM reads and the read of the data that underlies partial writes, the MCH supports detection of single-bit and multiple-bit errors, and will correct single bit errors when correction is enabled.

Intel® 855PM MCH DDR memory interface supports thermal throttling scheme to selectively throttle reads and/or writes. Throttling can be triggered either by on-die thermal sensor, or by preset read/write bandwidth limits. Read throttle can also be triggered by an external input pin. The memory controller logic supports aggressive dynamic row power down features (CKE#) to help reduce power. It also supports Address and Control lines Tri-stating when DRAM is in active power down or self refresh.

Note: Table 2 describes the memory configurations logically supported by Intel® 855PM MCH. Not all of these configurations will be validated on the reference platform.

Table 2. DDR Device Configurations

SO-DIMM Capacity	SO-DIMM Organization	Density	DDR Organization	# of Components	Package Type	# of Physical Banks	# of Banks in DDR	# Address Bits (row/col)
32 MB	4M x 64	64Mbit	4M x 16	4	66 lead TSOP	1	4	12/8
64 MB	8M x 64	64 Mbit	4M x 16	8	66 lead TSOP	2	4	12/8
64 MB	8M x 64	128 Mbit	8M x 16	4	66 lead TSOP	1	4	12/9
64 MB	8M x 72	128 Mbit	8M x 16	5	66 lead TSOP	1	4	12/9
128 MB	16M x 64	128 Mbit	8M x 16	8	66 lead TSOP	2	4	12/9
128 MB	16M x 64	256 Mbit	16M x 16	4	66 lead TSOP	1	4	13/9
128 MB	16M x 72	256 Mbit	16M x 16	5	66 lead TSOP	1	4	13/9
256 MB	32M x 64	256 Mbit	16M x 16	8	66 lead TSOP	2	4	13/9
256 MB	32M x 64	512 Mbit	32M x 16	4	66 lead TSOP	1	4	13/10
256 MB	32M x 72	512 Mbit	32M x 16	5	66 lead TSOP	1	4	13/10
512 MB	64M x 64	512 Mbit	32M x 16	8	66 lead TSOP	2	4	13/10
64 MB	8M x 64	64 Mbit	8M x 8	8	66 lead TSOP	1	4	12/9
128 MB	16M x 64	128 Mbit	16M x 8	8	66 lead TSOP	1	4	12/10
256 MB	32M x 64	256 Mbit	32M x 8	8	66 lead TSOP	1	4	13/10
512 MB	64M x 64	512 Mbit	64M x 8	8	66 lead TSOP	1	4	13/11

1.6. AGP Interface

A single AGP component or connector (not both) is supported by the Intel® 855PM MCH AGP interface. The AGP buffers operate only in 1.5-V mode. They are not 3.3-V safe.

The AGP interface supports 1x/2x/4x AGP signaling and 2x/4x Fast Writes. AGP semantic cycles to DRAM are not snooped on the host bus. PCI semantic cycles to DRAM are snooped on the host bus. The MCH supports PIPE# or SBA[7:0] AGP address mechanisms, but not both simultaneously. Either the PIPE# or the SBA[7:0] mechanism must be selected during system initialization. Both upstream and downstream addressing is limited to 32 bits for AGP and AGP/PCI transactions. The MCH contains a 32-deep AGP request queue. High priority accesses are supported. All accesses from the AGP/PCI interface that fall within the Graphics Aperture address range pass through an address translation mechanism with a fully associative 20 entry TLB. Accesses between AGP and hub interface are limited to memory writes originating from the hub interface destined for AGP. The AGP interface is clocked from a dedicated 66-MHz clock (66IN). The AGP-to-host/core interface is asynchronous.

The AGP interface should be powered-off or tri-stated without voltage on the interface during ACPI S3 or APM Suspend to RAM state.

Refer to the *Accelerated Graphics Port Interface Specification Rev 2.0* for more information.

1.7. Hub Interface

An 8-bit hub interface connects the MCH to the ICH4-M. All communication between the MCH and the ICH4-M occurs over the hub interface. The hub interface runs at 66 MHz/266 MB/s. Aside from the obvious traffic types, the following communication also occur over hub interface:

- Interrupt related messages
- Power management events as messages
- SMI, SCI, and SERR error indication messages

It is assumed that the hub interface is always connected to an ICH4-M. This is a proprietary interconnect between the MCH and the ICH4-M.

1.8. MCH Clocking

The MCH has the following clock input pins:

- Differential BCLK[1:0] for the host interface
- 66-MHz clock input for the AGP and hub interface

A Clock Synthesizer chip is responsible for generating the system Host clocks, AGP and hub interface clocks, PCI clocks, and DRAM clocks. The Host target speed is 400 MT/s. The AGP and hub interface runs at a constant 66-MHz base frequency. The hub interface runs at 4x, while AGP transfers may be 1x, 2x, or 4x.

The following table indicate the frequency ratios between the various interfaces that the MCH supports.

Table 3. MCH Clock Ratio Table

Interface	Speed	CPU System Bus Frequency Ratio
System Memory	DDR 200 MHz	1:1 Synchronous
	DDR 266 MHz	3:4 Synchronous
AGP	66 MHz	Asynchronous
Hub interface	66 MHz	Asynchronous

1.9. System Interrupts

The Intel® 855PM MCH supports both 8259 and Processor System Bus interrupt delivery mechanisms. The serial APIC interrupt mechanism is not supported.

The 8259 support consists of flushing inbound hub interface write buffers when an Interrupt Acknowledge cycle is forwarded from the system bus to the hub interface.

The Intel® 855PM MCH supports the Intel® Pentium 4 processor interrupt delivery mechanism. IOxAPIC and PCI MSI interrupts are generated as Memory Writes. The MCH decodes upstream Memory Writes to the range 0FEE0_0000h - 0FEEF_FFFFh from AGP and the hub interface as message based interrupts. The MCH forwards the Memory Writes, along with the associated write data, to the system bus as an Interrupt Message transaction. Note that since this address does not decode as part of main memory, the write cycle and the write data does not get forwarded to DRAM via the write buffer. The Intel® 855PM MCH provides the response and TRDY# for all Interrupt Message cycles including the ones originating from the MCH. The Intel® 855PM MCH supports interrupt re-direction for upstream interrupt memory writes.

For message based interrupts, system write buffer coherency is maintained by relying on strict ordering of Memory Writes. The Intel® 855PM MCH ensures that all Memory Writes received from a given interface prior to an interrupt message Memory Write are delivered to the system bus for snooping in the same order that they occur on the given interface.

2. Signal Description

This section provides a detailed description of Intel® 855PM MCH signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in the System Reset section.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
s/t/s	Sustained Tristate. This pin is driven to its inactive state prior to tri-stating.
as/t/s	Active Sustained Tristate. This applies to some of the hub interface signals. This pin is weakly driven to its last driven value.

The signal description also includes the type of buffer used for the particular signal:

AGTL+	Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The Intel® 855PM MCH integrates AGTL+ termination resistors. The Intel® 855PM MCH integrates AGTL+ termination resistors, and supports V_{CCP} of 1.05 V ± 5%
AGP	AGP interface signals. These signals are compatible with AGP 2.0 1.5-V Signaling Environment DC and AC Specifications. The buffers are not 3.3-V tolerant.
CMOS	CMOS buffers.
Ref	Voltage reference signal.

Note: System address and data bus signals are logically inverted signals. In other words, the actual values are inverted of what appears on the system bus. This must be taken into account and the addresses and data bus signals must be inverted inside the Intel® 855PM MCH. All processor control signals follow normal convention. A 0 indicates an active level (low voltage) if the signal is followed by "#" symbol, and a 1 indicates an active level (high voltage) if the signal has no "#" suffix.

2.1. Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Processor System Bus (Vccp).

Table 4. Host Interface Signal Descriptions

Signal Name	Type	Description
ADS#	I/O AGTL+	**Address Strobe:** The system bus owner asserts ADS# to indicate the first of two cycles of a request phase. The MCH can assert this signal for snoop cycles and interrupt messages.
BNR#	I/O AGTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
BPRI#	O AGTL+	**Bus Priority Request:** The MCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
BR0#	I/O AGTL+	**Bus Request 0#:** The MCH pulls the processor bus' BR0# signal low during CPURST#. The signal is sampled by the processor on the active-to-inactive transition of CPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. BR0# should be tristated after the hold time requirement has been satisfied.
CPURST#	O AGTL+	**CPU Reset:** The CPURST# pin is an output from the MCH. The MCH asserts CPURST# while RSTIN# (PCIRST# from ICH4-M) is asserted and for approximately 1 ms after RSTIN# is deasserted. The CPURST# allows the processor's to begin execution in a known state.
DBSY#	I/O AGTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O AGTL+	**Defer Response:** Signals that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
DPWR#	O AGTL+	**Data Power:** Asserted by MCH to indicate that a data return cycle is pending within 2 HCLK cycles or more. CPU should use this signal during a read-cycle to activate the data input buffers and sense-amps in preparation for DRDY# and the related data.
DBI[3:0]#	I/O AGTL+ 4x	**Dynamic Bus Inversion:** Driven along with the HD[63:0]# signals. Indicates if the associated signals are inverted or not. DBI[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **DBI[x]#** **Data Bits** DBI3#HD[63:48]# DBI2#HD[47:32]# DBI1#HD[31:16]# DBI0#HD[15:0]#
DRDY#	I/O AGTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2x	**Host Address Bus:** HA[31:3]# connect to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of hub interface and AGP/Secondary PCI initiators. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.

Signal Name	Type	Description
HADSTB[1:0]#	I/O AGTL+ 2x	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** **Address Bits** HADSTB0# HA[16:3]#, HREQ[4:0]# HADSTB1# HA[31:17]#
HD[63:0]#	I/O AGTL+ 4x	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus.
HDSTBP[3:0]# **HDSTBN[3:0]#**	I/O AGTL+ 4x	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer HD[63:0]# and DINV[3:0]# at the 4x transfer rate. **Strobe** **Data Bits** HDSTBP3#, HDSTBN3# HD[63:48]#, DINV3# HDSTBP2#, HDSTBN2# HD[47:32]#, DINV2# HDSTBP1#, HDSTBN1# HD[31:16]#, DINV1# HDSTBP0#, HDSTBN0# HD[15:0]#, DINV0#
HIT#	I/O AGTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	I/O AGTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and ADS#, until the negation of HLOCK# must be atomic, i.e. no hub interface or AGP snoopable access to DRAM are allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+ 2x	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the MCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	O AGTL+	**Response Status:** Indicates type of response according to the following the table: **RS[2:0]** **Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by MCH) 100 Hard Failure (not driven by MCH) 101 No data response 110 Implicit Write back 111 Normal data response

2.2. DDR Interface

Note: Unless otherwise specified, the voltage level for all signals in this interface is 2.5 Volts, and must be powered from the auxiliary well (i.e., must maintain power during S0 through S3 states).

Table 5. DDR Interface Descriptions

Signal Name	Type	Description
SCS#[3:0]	O CMOS	**Chip Select:** These pins select the particular DDR components during the active state. **NOTE:** There is one SCS# per DDR-SDRAM Physical SO-DIMM device row. These signals can be toggled on every rising System Memory Clock edge.
SMA[12:0]	O CMOS	**Multiplexed Memory Address:** These signals are used to provide the multiplexed row and column address to DDR.
SBS[1:0]	O CMOS	**Memory Bank Address:** These signals define the banks that are selected within each DDR row. The SMA and SBS signals combine to address every possible location within a DDR device.
SRAS#	O CMOS	**DDR Row Address Strobe:** SRAS# may be heavily loaded and requires 2 DDR clock cycles for setup time to the DDRs: Used with SCAS# and SWE# (along with SCS#) to define the DRAM commands.
SCAS#	O CMOS	**DDR Column Address Strobe:** SCAS# may be heavily loaded and requires 2 DDR clock cycles for setup time to the DDRs. Used with SRAS# and SWE# (along with SCS#) to define the DRAM commands.
SWE#	I/O CMOS	**Write Enable:** Used with SCAS# and SRAS# (along with SCS#) to define the DRAM commands. SWE# is asserted during writes to DDR. SWE# may be heavily loaded and requires 2 DDR clock cycles for setup time to the DDRs.
SDQ[71:0]	I/O CMOS 2X	**Data Lines:** These signals are used to interface to the DDR data bus (includes 8 check bit signals for ECC).
SDQS[8:0]	I/O CMOS	**Data Strobes:** There is an associated data strobe (DQS) for each data strobe (DQ) and check bit (CB) group. SDQS8 -> SDQ[71:64] SDQS7 -> SDQ[63:56] SDQS6 -> SDQ[55:48] SDQS5 -> SDQ[47:40] SDQS4 -> SDQ[39:32] SDQS3 -> SDQ[31:24] SDQS2 -> SDQ[23:16] SDQS1 -> SDQ[15:8] SDQS0 -> SDQ[7:0]
SCKE[3:0]	O CMOS	**Clock Enable:** These pins are used to signal a self-refresh or power down command to a DDR array when entering system suspend. SCKE is also used to dynamically power down inactive DDR rows. There is one SCKE per DDR row. These signals can be toggled on every rising SCLK edge.
RCVENOUT#	O CMOS	**Clock Output:** Used to emulate source-synch clocking for reads. Connects to RCVENIN#.
RCVENIN#	I CMOS	**Clock Input:** Used to emulate source-synch clocking for reads. Connects to RCVENOUT#.

2.3. Hub Interface Signals

Note: Unless otherwise specified, the voltage level for all signals in this interface is 1.8 Volts.

Table 6. Hub Interface Signal Descriptions

Signal Name	Type	Description
HI_[10:0]	I/O CMOS	**Hub Interface Signals:** Signals used for the hub interface.
HI_STB	I/O CMOS	**Hub Interface Strobe:** One of two differential strobe signals used to transmit or receive packet data over hub interface.
HI_STB#	I/O CMOS	**Hub Interface Strobe Complement:** One of two differential strobe signals used to transmit or receive packet data over hub interface.

2.4. AGP Interface Signals

Note: Unless otherwise specified, the voltage level for all signals in this interface is 1.5 Volts (VCC1_5).

2.4.1. AGP Addressing Signals

Table 7. AGP Addressing Signal Descriptions

Signal Name	Type	Description
PIPE#	I AGP	**Pipelined Read:** This signal is asserted by the AGP master to indicate a full width address is to be enqueued on by the target using the AD bus. One address is placed in the AGP request queue on each rising clock edge while PIPE# is asserted. When PIPE# is deasserted no new requests are queued across the AD bus. **During SBA Operation:** This signal is **not used** if SBA (Side Band Addressing) is selected. **During FRAME# Operation:** This signal is **not used** during AGP FRAME# operation. **PIPE#** is a sustained tri-state signal from masters (graphics controller), and is an input to the MCH.
SBA[7:0]	I AGP	**Side-band Address:** These signals are used by the AGP master (graphics controller) to pass address and command to the MCH The SBA bus and AD bus operate independently. That is, transactions can proceed on the SBA bus and the AD bus simultaneously. **During PIPE# Operation:** These signals are **not used** during PIPE# operation. **During FRAME# Operation:** These signals are **not used** during AGP FRAME# operation. **NOTE:** When sideband addressing is disabled, these signals are isolated (no external/internal pull-ups are required).

The above table contains two mechanisms to queue requests by the AGP master. Note that the master can only use one mechanism. The master may not switch methods without a full reset of the system. When PIPE# is used to queue addresses the master is not allowed to queue addresses using the SBA bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master will continue to use the mechanism selected until the master is reset (and

reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset.

2.4.2. AGP Flow Control Signals

Table 8. AGP Flow Control Signals

Signal Name	Type	Description
RBF#	I AGP	**Read Buffer Full:** Read buffer full indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted the MCH is not allowed to initiate the return low priority read data. That is, the MCH can finish returning the data for the request currently being serviced. RBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept return read data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.
WBF#	I AGP	**Write-Buffer Full:** indicates if the master is ready to accept Fast Write data from the MCH. When WBF# is asserted the MCH is not allowed to drive Fast Write data to the AGP master. WBF# is only sampled at the beginning of a cycle. If the AGP master is always ready to accept fast write data then it is not required to implement this signal. **During FRAME# Operation:** This signal is not used during AGP FRAME# operation.

2.4.3. AGP Status Signals

Table 9. AGP Status Signal Descriptions

Signal Name	Type	Description		
ST[2:0]	O AGP	**Status:** Provides information from the arbiter to an AGP Master on what it may do. ST[2:0] only have meaning to the master when its GNT# is asserted. When GNT# is deasserted these signals have no meaning and must be ignored.	**ST[2:0**	**Meaning**
			000	Previously requested low priority read data is being returned to the master
			001	Previously requested high priority read data is being returned to the master
			010	The master is to provide low priority write data for a previously queued write command
			011	The master is to provide high priority write data for a previously queued write command.
			100	Reserved
			101	Reserved
			110	Reserved
			110	The master has been given permission to start a bus transaction. The master may queue AGP requests by asserting PIPE# or start a PCI transaction by asserting FRAME#.

2.4.4. AGP Strobes

Table 10. AGP Strobe Descriptions

Signal Name	Type	Description
AD_STB0	I/O (s/t/s) AGP	**Address/Data Bus Strobe-0:** provides timing for 2x and 4x data on AD[15:0] and C/BE[1:0]# signals. The agent that is providing the data will drive this signal.
AD_STB0#	I/O (s/t/s) AGP	**Address/Data Bus Strobe-0 Complement:** With AD STB0, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals. The agent that is providing the data will drive this signal.
AD_STB1	I/O (s/t/s) AGP	**Address/Data Bus Strobe-1:** Provides timing for 2x and 4x data on AD[31:16] and C/BE[3:2]# signals. The agent that is providing the data will drive this signal.
AD_STB1#	I/O (s/t/s) AGP	**Address/Data Bus Strobe-1 Complement:** With AD STB1, forms a differential strobe pair that provides timing information for the AD[15:0] and C/BE[1:0]# signals in 4X mode. The agent that is providing the data will drive this signal.
SB_STB	I AGP	**Sideband Strobe:** Provides timing for 2x and 4x data on the SBA[7:0] bus. It is driven by the AGP master after the system has been configured for 2x or 4x sideband address mode.
SB_STB#	I AGP	**Sideband Strobe Complement:** The differential complement to the SB_STB signal. It is used to provide timing 4x mode.

2.4.5. AGP/PCI Signals-Semantics

For transactions on the AGP interface carried using AGP FRAME# protocol these signals operate similarly to their semantics in the PCI 2.1 specification, as defined below.

Table 11. AGP/PCI Signals-Semantics Descriptions

Signal Name	Type	Description
G_FRAME#	I/O s/t/s AGP	**G_FRAME:** Frame. **During PIPE# and SBA Operation:** Not used by AGP SBA and PIPE# operations. **During Fast Write Operation:** Used to frame transactions as an output during Fast Writes. **During FRAME# Operation:** G_FRAME# is an output when the MCH acts as an initiator on the AGP Interface. G_FRAME# is asserted by the MCH to indicate the beginning and duration of an access. G_FRAME# is an input when the MCH acts as a FRAME#-based AGP target. As a FRAME#-based AGP target, the MCH latches the C/BE[3:0]# and the AD[31:0] signals on the first clock edge on which MCH samples FRAME# active.
G_IRDY#	I/O s/t/s AGP	**G_IRDY#: Initiator Ready.** **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_IRDY# is an output when MCH acts as a FRAME#-based AGP initiator and an input when the MCH acts as a FRAME#-based AGP target. The assertion of G_IRDY# indicates the current FRAME#-based AGP bus initiator's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_IRDY# indicates that the AGP-compliant master is ready to provide all write data for the current transaction. Once G_IRDY# is asserted for a write operation, the master is not allowed to insert wait states. The master is never allowed to insert a wait state during the initial data transfer (32 bytes) of a write transaction. However, it may insert wait states after each 32-byte block is transferred.
G_TRDY#	I/O s/t/s AGP	**G_TRDY#:** Target Ready. **During PIPE# and SBA Operation:** Not used while enqueueing requests via AGP SBA and PIPE#, but used during the data phase of PIPE# and SBA transactions. **During FRAME# Operation:** G_TRDY# is an input when the MCH acts as an AGP initiator and is an output when the MCH acts as a FRAME#-based AGP target. The assertion of G_TRDY# indicates the target's ability to complete the current data phase of the transaction. **During Fast Write Operation:** In Fast Write mode, G_TRDY# indicates the AGP-compliant target is ready to receive write data for the entire transaction (when the transfer size is less than or equal to 32 bytes) or is ready to transfer the initial or subsequent block (32 bytes) of data when the transfer size is greater than 32 bytes. The target is allowed to insert wait states after each block (32 bytes) is transferred on write transactions.
G_STOP#	I/O s/t/s AGP	**G_STOP#:** Stop. **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_STOP# is an input when the MCH acts as a FRAME#-based AGP initiator and is an output when the MCH acts as a FRAME#-based AGP target. G_STOP# is used for disconnect, retry, and abort sequences on the AGP interface.

Signal Name	Type	Description
G_DEVSEL#	I/O s/t/s AGP	**G_ DEVSEL#: Device Select.** **During PIPE# and SBA Operation:** This signal is not used during PIPE# or SBA operation. **During FRAME# Operation:** G_DEVSEL#, when asserted, indicates that a FRAME#-based AGP target device has decoded its address as the target of the current access. The MCH asserts G_DEVSEL# based on the SDRAM address range being accessed by a PCI initiator. As an input, G_DEVSEL# indicates whether the AGP master has recognized a PCI cycle to it.
G_REQ#	I AGP	**G_REQ#: Request.** **During SBA Operation:** This signal is not used during SBA operation. **During PIPE# and FRAME# Operation:** G_REQ#, when asserted, indicates that the AGP master is requesting use of the AGP interface to run a FRAME#- or PIPE#-based operation.
G_GNT#	O AGP	**G_GNT#: Grant.** **During SBA, PIPE# and FRAME# Operation:** G_GNT#, along with the information on the ST[2:0] signals (status bus), indicates how the AGP interface will be used next. Refer to the *AGP Interface Specification, Revision 2.0* for further explanation of the ST[2:0] values and their meanings.
G_AD[31:0]	I/O AGP	**G_AD[31:0]: Address/Data Bus.** **During PIPE# and FRAME# Operation:** The G_AD[31:0] signals are used to transfer both address and data information on the AGP interface. **During SBA Operation:** The G_AD[31:0] signals are used to transfer data on the AGP interface.
G_CBE[3:0]#	I/O AGP	**Command/Byte Enable.** **During FRAME# Operation:** During the address phase of a transaction, the G_CBE[3:0]# signals define the bus command. During the data phase, the G_CBE[3:0]# signals are used as byte enables. The byte enables determine which byte lanes carry meaningful data. The commands issued on the G_CBE# signals during FRAME#-based AGP transactions are the same G_CBE# command described in the PCI 2.2 specification. **During PIPE# Operation:** When an address is enqueued using PIPE#, the C/BE# signals carry command information. Refer to the *AGP 2.0 Interface Specification, Revision 2.0* for the definition of these commands. The command encoding used during PIPE#-based AGP is *different* than the command encoding used during FRAME#-based AGP cycles (or standard PCI cycles on a PCI bus). **During SBA Operation:** These signals are not used during SBA operation.
G_PAR	I/O AGP	**Parity.** **During FRAME# Operation:** G_PAR is driven by the MCH when it acts as a FRAME#-based AGP initiator during address and data phases for a write cycle, and during the address phase for a read cycle. G_PAR is driven by the MCH when it acts as a FRAME#-based AGP target during each data phase of a FRAME#-based AGP memory read cycle. Even parity is generated across G_AD[31:0] and G_CBE[3:0]#. **During SBA and PIPE# Operation:** This signal is not used during SBA and PIPE# operation.

PCIRST# from the ICH4-M is assumed to be connected to RSTIN# and is used to reset AGP interface logic within the MCH. The AGP agent will also typically use PCIRST# provided by the ICH4-M as an input to reset its internal logic.

2.5. Clocks, Reset, and Miscellaneous

Table 12. Clocks, Reset, and Miscellaneous Signal Descriptions

Signal Name	Type	Description
BCLK **BCLK#**	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the Host clock domain.
66IN	I CMOS	**66 MHz Clock In:** This pin receives a 66-MHz clock from the clock synthesizer. This clock is used by AGP/PCI and hub interface clock domains. **NOTE:** That this clock input is 3.3-V tolerant.
SCK[5:0]	O CMOS	**SDRAM Differential Clock (DDR):** These signals deliver a source synchronous clock to the SO-DIMMs. There are three per SO-DIMM.
SCK#[5:0]	O CMOS	**SDRAM Inverted Differential Clock (DDR):** These signals are the complement to the SCK[5:0] signals. There are three per SO-DIMM.
RSTIN#	I CMOS	**Reset In:** When asserted this signal will asynchronously reset the MCH logic. This signal is connected to the PCIRST# output of the ICH4-M. All AGP/PCI output and bi-directional signals will also tri-state compliant to PCI Rev 2.0 and 2.1 specifications. **NOTE:** That this input needs to be 3.3-V tolerant.
TESTIN#	I CMOS	**Test Input:** This pin is used for manufacturing and board level test purposes. **NOTE:** This signal has an internal pullup resistor.
DPSLP#	I CMOS	**Deep Sleep Input:** This signal comes from the ICH4-M device, providing an indication of C3 and Deeper Sleep (C4) state entry to the CPU. **NOTE:** that this input is low-voltage CMOS, operating on the PSB Vccp power plane.
ETS#	I CMOS	**External Thermal Sensor Input:** This signal is an active low input to the MCH, which is used to monitor status of external thermal sensor activity, is enabled. The MCH can be optionally programmed to send a SERR, SCI, or SMI message to ICH4-M upon the triggering of this signal.

2.6. Voltage References, PLL Power

Table 13. Voltage References, PLL Power Descriptions

Signal Name	Type	Description
HLRCOMP	I/O CMOS	**Compensation for hub interface:** This signal is used to calibrate the hub interface I/O buffers.
GRCOMP	I/O CMOS	**Compensation for AGP:** This signal is used to calibrate AGP buffers.
HRCOMP[1:0]	I/O CMOS	**Compensation for Host:** This signal is used to calibrate the Host AGTL+ I/O buffers.
SMRCOMP	I/O CMOS	**System Memory RCOMP**
HVREF[4:0]		**Host Reference Voltage.** Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface
SMVREF[1:0]		**DDR Reference Voltage:** Reference voltage input for DQ, DQS, and RCVENIN#.
HI_REF		**Hub Interface Reference:** Reference voltage input for the hub interface.
AGPREF		**AGP Reference:** Reference voltage input for the AGP interface.
HSWNG[1:0]		**Host Reference Voltage:** Reference voltage input for the compensation logic.
VCC1_2		**The 1.2 V Power input pins**
VCC1_8		**The 1.8 V Power input pins**
VCCSM		**The DRAM Power input pins.** 2.5 V for DDR.
VCC1_5		**The power supply input for the AGP I/O supply (1.5 V)**
VCCGA, VCCHA		**PLL power input pins. (1.8 V)**
VCCP		**The AGTL+ bus termination voltage inputs (1.05 V)**
VSS		**GROUND**

The following table shows the value of the RCOMP resistor and the termination point for each interface's RCOMP signal.

Note: These values are based on the board impedance assumption of 55 Ohm ± 15%.

Table 14. RCOMP Resistor Value Recommendations

Interface	RCOMP R	RCOMP Term
Host PSB	27.4 Ohm ± 1%	VSS
AGP	36.5 Ohm ± 1%	VSS
Hub Interface	39.4 Ohm ± 1%	VCC1_8
SM DDR	30.1 Ohm ± 1%	V1.25 (1.25 V Vtt for DDR)

2.7. Reset States and Pull-up/Pull-downs

This section describes the expected states of the MCH I/O buffers. These tables only refer to the contributions on the interface from the MCH and do NOT reflect any external influence (such as external pullup/pulldown resistors or external drivers).

Legend :

Term H/L:	Normal termination devices are turned on high/low
Pwrdn:	Power down
Drive H/L:	Strong Drive high/low
Tri/High-Z:	High Impedance
IN:	Input buffer Enabled
PU, PD/PL:	Weak internal pull-up, Weak internal pull down
(Strap):	Strap input sampled during assertion or on the deassertion edge of RSTIN#

Table 15. Host Signals

	Buffer Type/IO	Signal Type	State During RSTIN# Assertion	State After RSTIN# Deassertion	C3/C4	S1	S3	S4	S5
HA[31:3]#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HD[63:0]#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HADSTB[1:0]#	AGTL+	I/0	Term H	Term H					
HDSTBP[3:]0]#	AGTL+	I/O	Term H	Term H					
HDSTBN[3:]0]#	AGTL+	I/O	Term H	Term H					
ADS#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
BNR#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
BPRI#	AGTL+	O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
BR0#	AGTL+	O	Term H	Term H					
DBI[3:0]#	AGTL+	I/O	Term H	Term H					
DBSY#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
DEFER#	AGTL+	O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
DPWR#	AGTL+	O	TERM H	TERM H					
DRDY#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HIT#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HITM#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HLOCK#	AGTL+	I	Term H	Term H	N/a	N/a	N/a	N/a	N/a
HREQ[4:0]#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
HTRDY#	AGTL+	I/O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
RS[2:0]#	AGTL+	O	Term H	Term H	Term H	Term H	Pwrdn	Pwrdn	Pwrdn
CPURST#	AGTL+	O	Drive L	Term H after 1 ms	Term H	Term H	Pwrdn	Pwrdn	Pwrdn

Table 16. DDR Signals

	Buffer Type/IO	Signal Type	State During RSTIN# Assertion	State After RSTIN# Deassertion	C3/C4	S1	S3	S4	S5
SCK/SCK# [5:0]	CMOS	O	TRI	TRI | DRIVE	Don't care	Don't care	Don't care	Pwrdn	Pwrdn
SCKE[3:0]	CMOS	O	DRIVE L	DRIVE L	Low	Low	Low	Pwrdn	Pwrdn
SDQ[71:0]	CMOS	I/O	PU	PU	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SDQS[8:0]	CMOS	I/O	TRI	TRI	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
RCVENIN#	CMOS	I	IN	IN	IN | Hi	IN | Hi	Don't care	Pwrdn	Pwrdn
RCVENOUT#	CMOS	O	TRI	Drive H	TRI | Hi	Drive H | Hi	Hi-Z	Pwrdn	Pwrdn
SBS[1:0]	CMOS	O	TRI	TRI | DRIVE	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SRAS#	CMOS	O	TRI	TRI | DRIVE	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SWE#	CMOS	O	TRI	TRI | DRIVE	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SCAS#	CMOS	O	TRI	TRI | DRIVE	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SMA[12:0]	CMOS	O	TRI	TRI | DRIVE	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn
SCS#[3:0]	CMOS	O	TRI	TRI | Drive H	Hi-Z	Hi-Z	Hi-Z	Pwrdn	Pwrdn

Table 17. AGP Signals

	Buffer Type IO	Signal Type	State During RSTIN# Assertion	State After RSTIN# Deassertion	Pull Up/Pull Down	C3/C4	S1	S3	S4	S5
PIPE#	CMOS	I	PU	PU	4.5 k Int Pullup	H	H	Pwrdn	Pwrdn	Pwrdn
SBA[7:0]	CMOS	I	PU (Strap)	PU	4.5 k Int Pullup	High	High	Pwrdn	Pwrdn	Pwrdn
RBF#	CMOS	I	PU (Strap)	PU	4.5 k Int Pullup	High	High	Pwrdn	Pwrdn	Pwrdn
WBF#	CMOS	I	PU (Strap)	PU	4.5 k Int Pullup	High	High	Pwrdn	Pwrdn	Pwrdn
ST[2:0]	CMOS	O	PU (Strap)	DRIVE L	4.5 k Int Pullup	Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn
AD_STB0	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
AD_STB0#	CMOS	I/O	PD	PD	4.5 k Int Pulldwn	PL	PL	Pwrdn	Pwrdn	Pwrdn
AD_STB1	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
AD_STB1#	CMOS	I/O	PD	PD	4.5 k Int Pulldwn	PD	PD	Pwrdn	Pwrdn	Pwrdn
SB_STB	CMOS	I	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
SB_STB#	CMOS	I	PD	PD	4.5 k Int Pulldwn	PD	PD	Pwrdn	Pwrdn	Pwrdn
G_FRAME#	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_IRDY#	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_TRDY#	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_STOP#	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_DEVSEL#	CMOS	I/O	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_REQ#	CMOS	I	PU	PU	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_GNT#	CMOS	O	PU (Strap)	DRIVE H	4.5 k Int Pullup	PU	PU	Pwrdn	Pwrdn	Pwrdn
G_AD[31:0]	CMOS	I/O	TRI	TRI		Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn
G_C/BE[3:0]#	CMOS	I/O	TRI	TRI		Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn
G_PAR	CMOS	I/O	TRI	TRI		Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn

Table 18. Clock/Miscellaneous Signals

	Buffer Type/IO	Signal Type	State During RSTIN# Assertion	State After RSTIN# Deassertion	C3/C4	S1	S3	S4	S5
BCLK/#	CMOS	I	IN	IN	Running	Stopped (Low)	Pwrdn	Pwrdn	Pwrdn
66IN	CMOS	I	IN	IN	Running	Stopped (Low)	Pwrdn	Pwrdn	Pwrdn
RSTIN#	CMOS	I	IN	IN	High	High	Low	Pwrdn	Pwrdn
ETS#	CMOS	I	Hi-Z	Hi-Z					
GRCOMP	CMOS	I/O	TRI	TRI after RCOMP	Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn
HLRCOMP	CMOS	I/O	TRI	TRI after RCOMP	Hi-Z	Hi-Z	Pwrdn	Pwrdn	Pwrdn
HRCOMP[1:0]	CMOS	I/O	TRI	TRI after RCOMP					
HSWNG[1:0]	CMOS		IN	IN					
TESTIN#	CMOS	I	IN PU	IN PU					

Table 19. Hub Interface Signals

	Buffer Type/IO	Signal Type	State During RSTIN# Assertion	State After RSTIN# Deassertion	Pull Up/Pull Down	C3/C4	S1	S3	S4	S5
HI_STB	CMOS	I/O	PD	PD	N/A	N/A	N/A	Pwrdn	Pwrdn	Pwrdn
HI_STB#	CMOS	I/O	PU	PU	N/A	N/A	N/A	Pwrdn	Pwrdn	Pwrdn
HI_[10:0]	CMOS	I/O	N/A	N/A	N/A	N/A	N/A	Pwrdn	Pwrdn	Pwrdn

Note: Initialization software sometimes enables SBA on the target (MCH) before enabling SBA on the master. The MCH begins looking for valid SBA accesses as soon as its SBA enable bit is turned on. Since the SBA bus is floating if the master has not yet been enabled, the MCH may erroneously sample a valid address. Due to the 4x signaling and motherboard space restriction, adding external pullups is not an acceptable solution. Therefore, the MCH implements internal SBA pullups. The value of the internal resistors will be in the range of 4-16 kΩ.

In addition, the MCH integrates internal pull-ups (in the same 4-16 kΩ range) on all Sustained Tri-State types (such as FRAME#, IRDY#, TRDY#, STOP#, DEVSEL#). Pullups are also integrated for the AD and SBA strobes (pull-downs on the strobe complements), and a few others that have traditionally been pulled up to reduce risk (such as RBF#, WBF#, G_GNT#, GREQ#, PIPE#). The integration of these resistors eliminates the need for ANY pull-ups or pull-downs on the AGP interface (except for RCOMP), which reduces motherboard cost and routing congestion.

3. Register Description

3.1. Conceptual Overview of the Platform Configuration Structure

The Intel® 855PM MCH and ICH4-M are physically connected by hub interface A. From a configuration standpoint, the hub interface A is PCI bus #0. As a result, all devices internal to the MCH and ICH4-M appear to be on PCI bus #0. The system's primary PCI expansion bus is physically attached to the ICH4-M and from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. Note that the primary PCI bus is referred to as PCI_A in this document and is not PCI bus #0 from a configuration standpoint. The AGP appears to system software to be a real PCI bus behind PCI-to-PCI bridges resident as devices on PCI bus #0.

The MCH contains two PCI devices within a single physical component. The configuration registers for the two devices are mapped as devices residing on PCI bus #0.

- Device 0: Host-hub interface Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI bus #0. Physically Device 0 contains the standard PCI registers, DRAM registers, the Graphics Aperture controller, and other MCH specific registers.
- Device 1: Host-AGP Bridge. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus #0. Physically Device 1 contains the standard PCI-to-PCI bridge registers and the standard AGP/PCI configuration registers (including the AGP I/O and memory address mapping).
- Device 6: Device #6 is a device that contains a few power management registers. For Device #6 configuration space to be visible, MCHTST Register in Device #0 space Bit 1 (D6EN bit) should be set.

Table 20 shows the Device # assignment for the various internal MCH devices.

Table 20. Device Number Assignment

MCH Function	Bus #0, Device#
DRAM Controller/8 bit HI_A Controller	Device #0
Host-to-AGP Bridge (virtual P2P)	Device #1
Power Management Registers	Device #6

A physical PCI bus #0 does not exist. The hub interface, and the internal devices in the Intel® 855PM MCH and ICH4-M, logically constitute PCI Bus #0 to configuration software.

3.2. Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to eight functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by

a mapping mechanism implemented within the MCH. The PCI specification defines two mechanisms to access configuration space, Mechanism #1 and Mechanism #2. The MCH supports only Mechanism #1.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a Dword I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the CPU's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers, hub interface, or AGP.

3.3. Routing Configuration Accesses

The MCH supports two bus interfaces: the hub interface and AGP. PCI configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing PCI configuration cycles to the proper interface. PCI configuration cycles to the ICH4-M internal devices, and Primary PCI (including downstream devices) are routed to the ICH4-M via the hub interface. AGP configuration cycles are routed to AGP. The AGP interface is treated as a separate PCI bus from the configuration point of view. Routing of configuration AGP is controlled via the standard PCI-PCI bridge mechanism using information contained within the PRIMARY BUS NUMBER, the SECONDARY BUS NUMBER, and the SUBORDINATE BUS NUMBER registers of the corresponding PCI-PCI bridge device.

A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles on one of the buses is described in the following section.

3.3.1. PCI Bus #0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus #0 device.

- The Host-HI Bridge entity within the MCH is hardwired as Device #0 on PCI Bus #0.
- The Host-AGP Bridge entity within the MCH is hardwired as Device #1 on PCI Bus #0.

Configuration cycles to any of the MCH's internal devices are confined to the MCH and not sent over hub interface. Accesses to disabled MCH internal devices will be forwarded over the hub interface as Type 0 Configuration cycles.

3.3.2. Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and is less than the value in the Host-AGP device's SECONDARY BUS NUMBER register, or greater than the value in the Host-AGP device's SUBORDINATE BUS NUMBER register, the MCH will generate a Type 1 hub interface Configuration cycle. The ICH4-M compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its P2P bridges to determine if the configuration cycle is meant for Primary PCI or a downstream PCI bus.

3.3.3. AGP Configuration Mechanism

From the chipset configuration perspective, AGP is seen as a PCI bus interface residing on a Secondary Bus side of the "virtual" PCI-PCI bridges referred to as the MCH Host-AGP bridge. On the Primary Bus side, the "virtual" PCI-PCI bridge is attached to PCI Bus #0. Therefore, the PRIMARY BUS NUMBER register is hardwired to 0. The "virtual" PCI-PCI bridge entity converts Type #1 PCI Bus Configuration cycles on PCI Bus #0 into Type 0 or Type 1 configuration cycles on the AGP interface. Type 1 configuration cycles on PCI Bus #0 that have a BUS NUMBER that matches the SECONDARY BUS NUMBER of the MCH's "virtual" Host-to-PCI_B/AGP bridge will be translated into Type 0 configuration cycles on the AGP interface.

If the Bus Number is non-zero, greater than the value programmed into the SECONDARY BUS NUMBER register, and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER register, the MCH will generate a Type 1 PCI configuration cycle on AGP.

3.4. MCH Register Introduction

The MCH contains two sets of software accessible registers, accessed via the Host CPU I/O address space: control registers I/O mapped into the CPU I/O space (they control access to PCI) and AGP configuration space (see Section 3.5).

Internal configuration registers residing within the MCH are partitioned into four logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host-HI Bridge functionality (i.e. DRAM configuration, other chip-set operating parameters and optional features). The second register block is dedicated to Host-AGP Bridge functions (controls AGP interface configurations and operating parameters).

The MCH supports PCI configuration space accesses using the mechanism denoted as Configuration Mechanism #1 in the PCI specification.

The MCH internal registers (I/O Mapped and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a Dword. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field).

Reserved Bits:

Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved." Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.

Reserved Registers:

In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host-HI Bridge entity that are marked either "Reserved" or "Intel Reserved." When a "Reserved" register location is read, a random value is returned. ("Reserved" registers can be 8-bit, 16-bit, or 32-bit in size.) Writes to "Intel Reserved" registers may cause system failure. Reads to "Intel Reserved" registers may return a non-zero value.

Default Value Upon Reset:

Upon a full Reset, the MCH sets all of its internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

3.5. I/O Mapped Registers

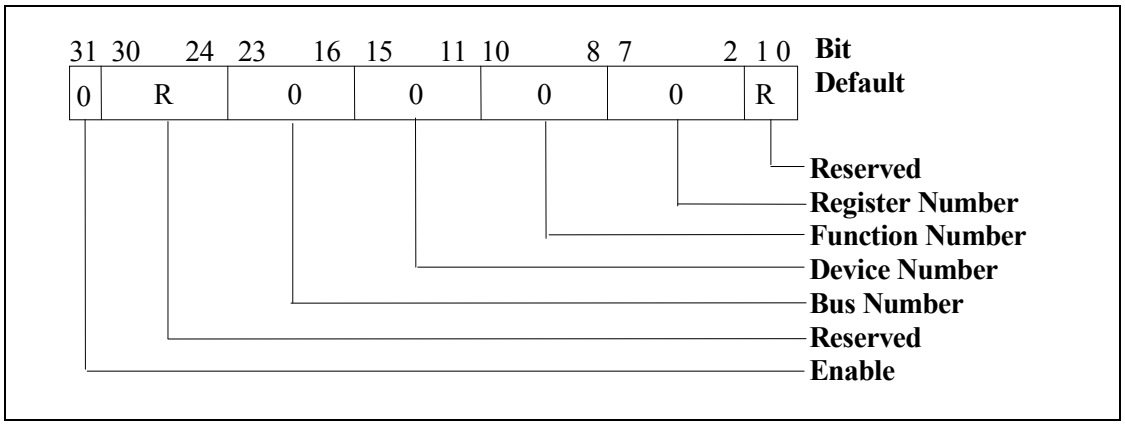
The MCH contains two registers that reside in the CPU I/O address space: the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.5.1. CONFIG_ADDRESS – Configuration Address Register

I/O Address: 0CF8h Accessed as a Dword
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a Dword. A Byte or Word reference will "pass through" the Configuration Address Register and the hub interface, onto the PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Figure 1. Configuration Address Register



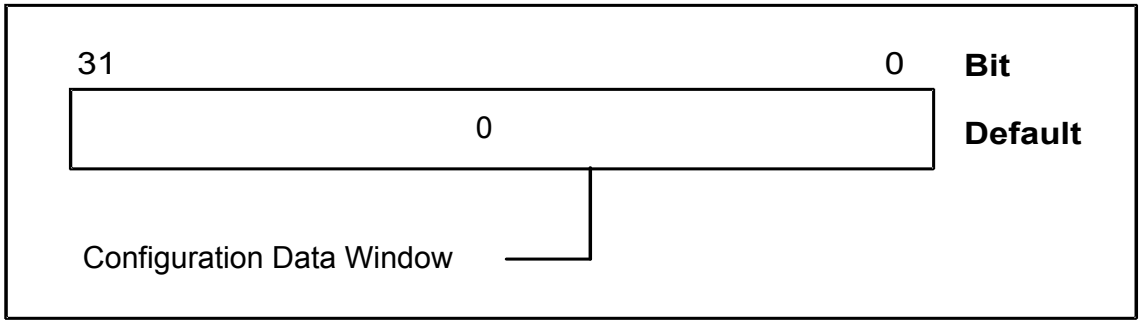
Bit	Descriptions
31	**Configuration Enable (CFGE):** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	**Reserved (These bits are read only and have a value of 0).**
23:16	**Bus Number:** When the Bus Number is programmed to 00h the target of the Configuration cycle is a hub interface agent (MCH, ICH4-M, etc.). The Configuration cycle is forwarded to hub interface if the Bus Number is programmed to 00h and the MCH is not the target (the device number is >= 2). If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register of device #1, a Type 0 PCI configuration cycle will be generated on AGP. If the Bus Number is non-zero, greater than the value in the SECONDARY BUS NUMBER register of device #1 and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER Register of device #1 a Type 1 PCI configuration cycle will be generated on AGP. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device #1's SECONDARY BUS NUMBER or SUBORDINATE BUS NUMBER Register, then a hub interface Type 1 Configuration Cycle is generated.
15:11	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00 the MCH decodes the Device Number field. The MCH is always Device Number 0 for the Host-hub interface bridge entity and Device Number 1 for the Host-AGP entity. Therefore, when the Bus Number =0 and the Device Number=0-1 the internal MCH devices are selected. If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register a Type 0 PCI configuration cycle will be generated on AGP. The MCH will decode the Device Number field[15:11] and assert the appropriate GAD signal as an IDSEL. For PCI-to-PCI Bridge translation, one of the 16 IDSELs is generated. When bit [15] = 0 bits [14:11] are decoded to assert a signal AD[31:16] IDSEL. GAD16 is asserted to access Device #0, GAD17 for Device #1 and so forth up to Device #15 for which will assert AD31. All device numbers higher than 15 cause a type 0 configuration access with no IDSEL asserted, which will result in a Master Abort reported in the MCH's "virtual" PCI-PCI bridge registers. For Bus Numbers resulting in hub interface configuration cycles, the MCH propagates the device number field as A[15:11]. For bus numbers resulting in AGP type 1 configuration cycles, the device number is propagated as GAD[15:11].
10:8	**Function Number:** This field is mapped to GAD[10:8] during AGP Configuration cycles and A[10:8] during hub interface configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal Devices if the function number is not equal to 0.
7:2	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to GAD[7:2] during AGP Configuration cycles and A[7:2] during hub interface Configuration cycles.
1:0	**Reserved**

3.5.2. CONFIG_DATA - Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Figure 2. Configuration Data Register



Bit	Descriptions
31:0	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1 any I/O access that to the CONFIG_DATA register will be mapped to configuration space using the contents of CONFIG_ADDRESS.

3.6. Memory Mapped Register Space

All system memory control functions have been consolidated into a new memory mapped address region within Device 0 Function 0. This space will be accessed using a new Base Address Register (BAR) located At Dev 0 Func 0 Offset 14h. By default this BAR will be invisible (i.e., Read-Only zeros). However, there is an enable bit (MCHTST[22] offset F4h) that turns this register into a normal BAR that requests 4 kB of address space. It is expected that this address space will only be enabled temporarily by system BIOS, then disabled to hide it from the operating system.

Note: All accesses to these Memory Mapped registers must be made as a single DWORD (4 bytes) or less. Access must be aligned on a natural boundary.

The high-level breakout of these RCOMP memory-mapped registers is provided below.

Table 21. MCH Memory Mapped Register (MMR) Space - Device #0

Address Offset	Register Symbol	Register Name	Default Value	Access
20-23h	SMRCTL	System Memory RCOMP Control Register	00000000h	RO, R/W
2Ch	DRAMWIDTH	DRAM Width Register	00h	RO, R/W
2E-2Fh	DCLKDIS	DRAM Clock Control Disable Register	03FFh	RO, R/W
30h	DQCMDSTR	Strength Control Register for DQ and CMD Signal Groups	00h	RO, R/W
31h	CKESTR	Strength Control Register for CKE Signal Group	00h	RO, R/W
32h	CSBSTR	Strength Control Register for CS# Signal Group	00h	RO, R/W
33h	CKSTR	Strength Control Register for CK Signal Group (CK / CK#)	00h	RO, R/W
34h	RCVENSTR	Strength Control Register for RCVENOUT# Signals	00h	RO, R/W
35h	CGREDSTR	Strength Control Register for CMD Group Reduced Strength Signals	00h	RO, R/W

3.6.1. SMRCTL – System Memory RCOMP Control Register– Device #0

Offset: **20-23h**
Default: **00000000h**
Access: **Read Only, Read/Write**
Size: **32 bits**

This register controls the System Memory RCOMP feature.

Bit	Description
32:12	**Reserved**
11	**RCOMP Lock Bit:** Once this bit is set, any further writes to this memory mapped space will be ignored.
10:9	**Reserved**
8	**Force SM RCOMP Measurement Cycle:** A 0->1 transition on this signal initiates an RCOMP Measurement cycle on the System Memory interface.
7:2	**Reserved**
1:0	**SM Digital Filter Length:** Selects the length of the digital filter to be used for sampling the RCOMP value. A larger value for this filter length increases the noise immunity of the RCOMP evaluation. SMRCTL[1:0] 00 4 sample filter (default) 01 8 sample filter 10 16 sample filter 11 32 sample filter

3.6.2. DRAMWIDTH – DRAM Width Register

Address Offset: 2Ch
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register determines the width of DDR-SDRAM devices populated in each row of memory.

Bit	Descriptions
7:2	Reserved.
1	**SO-DIMM 1 Width:** Width of devices in Row 2 and/or Row 3 0 = 16-bit wide devices, or Unpopulated (default) 1 = 8-bit wide devices
0	**SO-DIMM 0 Width:** Width of devices in Row 0 and/or Row 1 0 = 16-bit wide devices, or Unpopulated (default) 1 = 8-bit wide devices

Note: Since there are multiple clock signals assigned to each row of an SO-DIMM, it is important to clarify exactly which SO-DIMM width field affects which clock signal:

SO-DIMM Parameters	DDR Clocks Affected
0	SCK/SCK# [2:0]
1	SCK/SCK# [5:3]

3.6.3. DCLKDIS – DRAM Clock Control Disable Register

Address Offset: 2E-2Fh
Default Value: 03FFh
Access: Read Only, Read/Write
Size: 16 bits

This register can be used to individually disable each System Memory Clock signal, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated SO-DIMMs. It can also be used to individually disable CS/CKE per memory row for unpopulated rows.

BIOS should enable the appropriate clocks after setting RCOMP parameters and allowing at least one RCOMP cycle to be completed.

Clock routing and use notes:

For the examples below it is assumed that the motherboard routes the clocks from Intel® 855PM MCH to the SO-DIMMs mapping them in the following manner:

Intel® 855PM MCH Pin	DDR SO-DIMM
SCK0 and SCK#0	SCK0 and SCK#0 pair on SO-DIMM 0
SCK1 and SCK#1	SCK1 and SCK#1 pair on SO-DIMM 0

SCK2 and SCK#2	SCK2 and SCK#2 pair on SO-DIMM 0
SCK3 and SCK#3	SCK0 and SCK#0 pair on SO-DIMM 1
SCK4 and SCK#4	SCK1 and SCK#1 pair on SO-DIMM 1
SCK5 and SCK#5	SCK2 and SCK#2 pair on SO-DIMM 1

Note: If the motherboard routes clocks from Intel® 855PM MCH to the SO-DIMMs in any other manner than described above (swapping pins, etc), it is the responsibility of the BIOS and/or OEM to program the appropriate clocks according to these guidelines.

Clocks for unpopulated SO-DIMMs should be disabled.

Clock pairs (SCKn/SCK#n) must be routed as a pair! If clock pin swapping is done it must be done in pairs since the enables below will enable pairs.

In DDR SO-DIMMs there are three clock pins. Non-ECC SO-DIMMs only use SCK[1:0]. Assuming the clock configuration above, it may be possible to not enable SCK[2] and SCK[5] for non-ECC SO-DIMMs. Disabling the unnecessary clocks will result in power savings and reduced EMI/noise.

Bit	Descriptions
15:10	**Reserved**
9	**Row 3 CS/CKE Disable** 0: Row 3 CS/CKE are controlled normally 1: Row 3 is not populated and CS/CKE are not driven (tri-stated)
8	**Row 2 CS/CKE Disable** 0: Row 2 CS/CKE are controlled normally 1: Row 2 is not populated and CS/CKE are not driven (tri-stated)
7	**Row 1 CS/CKE Disable** 0: Row 1 CS/CKE are controlled normally 1: Row 1 is not populated and CS/CKE are not driven (tri-stated)
6	**Row 0 CS/CKE Disable** 0: Row 0 CS/CKE are controlled normally 1: Row 0 is not populated and CS/CKE are not driven (tri-stated)
5	**Disables SCK5 and SCK#5** 0: Clock enabled 1: Clock disabled (tri-stated)
4	**Disables SCK4 and SCK#4** 0: Clock enabled 1: Clock disabled (tri-stated)
3	**Disables SCK3 and SCK#3** 0: Clock enabled 1: Clock disabled (tri-stated)
2	**Disables SCK2 and SCK#2** 0: Clock enabled 1: Clock disabled (tri-stated)
1	**Disables SCK1 and SCK#1** 0: Clock enabled 1: Clock disabled (tri-stated)
0	**Disables SCK0 and SCK#0** 0: Clock enabled 1: Clock disabled (tri-stated)

3.6.4. DQCMDSTR – Strength Control Register for DQ and CMD Signal Groups

Address Offset: 30h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the drive strength of the I/O buffers for the DQ/DQS and CMD signal groups.

Bit	Descriptions
7	**Reserved.**
6:4	CMD Strength Control (RAS#, CAS#, WE#, MA[12:0], BS[1:0]) **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved
3	**Reserved**
2:0	DQ/DQS Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved

3.6.5. CKESTR – Strength Control Register for CKE Signal Group

Address Offset: 31h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the drive strength of the I/O buffers for the CKE signal group. This group has two possible loadings depending on the width of SDRAM devices used in each Row of memory (x8 or x16). The proper strength can be independently programmed for each configuration. The actual strength used for each signal is determined by the Width Select register (offset 4Dh).

Bit	Descriptions
7	**Reserved**
6:4	CKE x16 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved
3	**Reserved**
2:0	CKE x8 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved

3.6.6. CSBSTR – Strength Control Register for CS# Signal Group

Address Offset: **32h**
Default Value: **00h**
Access: **Read Only, Read/Write**
Size: **8 bits**

This register controls the drive strength of the I/O buffers for the CS# signal group. This group has two possible loadings depending on the width of SDRAM devices used in each Row of memory (x8 or x16). The proper strength can be independently programmed for each configuration. The actual strength used for each signal is determined by the Width Select register (offset 4Dh).

Bit	Descriptions
7	**Reserved.**
6:4	CS# x16 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved
3	**Reserved**
2:0	CS# x8 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved

3.6.7. CKSTR – Strength Control Register for CK Signal Group (CK / CK#)

Address Offset: 33h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the drive strength of the I/O buffers for the CK signal group, which includes both the CK and CK# signals. This group has two possible loadings depending on the width of SDRAM devices used in each Row of memory (x8 or x16). The proper strength can be independently programmed for each configuration. The actual strength used for each signal is determined by the Width Select register (offset 4Dh).

Bit	Descriptions
7	**Reserved**
6:4	CK x16 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved
3	**Reserved**
2:0	CK x8 Strength Control: Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved

3.6.8. RCVENSTR – Strength Control Register for RCVENOUT# Signals

Address Offset: 34h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the drive strength of the I/O buffers for the Receive Enable Out (RCVENOUT#) signal.

Bit	Descriptions
7:3	**Reserved**
2:0	**RCVEnOut# Strength Control:** Sets drive strength as shown below: **000** = 0.75 X (default) **001** = 1.00 X **010** = 1.25 X **011** = 1.50 X **100** = 2.00 X **101** = 2.50 X **110** = 3.00 X **111** = Reserved

3.6.9. CGREDSTR – Strength Control Register for CMD Group Reduced Strength Signals

Address Offset: 35h
Default Value: 00h
Access: Read Only, Read/Write
Size: 8 bits

This register controls the drive strength of the I/O buffers for the command group (MA[12:0], BS[1:0], RAS#, CAS#, WE#) I/O buffers.

Bit	Descriptions
7:3	**Reserved**
2:0	**Command Group Reduced Strength Control:** Sets drive strength as shown below: 000 = 0.75 X (default) 001 = 1.00 X 010 = 1.25 X 011 = 1.50 X 100 = 2.00 X 101 = 2.50 X 110 = 3.00 X 111 = 0.50 X

3.7. Host-Hub Interface Bridge Device Registers – Device #0

Table 22 shows the access attributes for the configuration space. An "s" in the Default Value field means that a strap determines the power-up default value for that bit. **Error! Reference source not found.** below summarizes the MCH configuration space for Device #0.

Table 22. Nomenclature for Access Attributes

RO	**Read Only:** If a register is read only, writes to this register have no effect.
R/W	**Read/Write:** A register with this attribute can be read and written.
R/W/L	**Read/Write/Lock:** A register with this attribute can be read, written, and Lock.
R/WC	Read/**Write Clear:** A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.
R/WO	**Read/Write Once:** A register bit with this attribute can be written to only once after power up. After the first write, the bit becomes read only.
L	**Lock:** A register bit with this attribute becomes Read Only after a lock bit is set.

Table 23. MCH Configuration Space - Device #0

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID	Vendor Identification	8086h	RO
02-03h	DID	Device Identification	3340h	RO
04-05h	PCICMD	PCI Command Register	0006h	RO, R/W
06-07h	PCISTS	PCI Status Register	0090h	RO, R/WC
08h	RID	Revision Identification	00h	RO
09h		Reserved		
0Ah	SUBC	Sub-Class Code	00h	RO
0Bh	BCC	Base Class Code	06h	RO
0Ch		Reserved		
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh		Reserved		
10-13h	APBASE	Aperture Base Configuration	00000008h	RO, R/W
14-17h	SMRBASE	SM RCOMP Base Address Register	00000000h	RO, R/W
18-2Bh		Reserved		
2C-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E-2Fh	SID	Subsystem Identification	0000h	R/WO
30-33h		Reserved		
34h	CAPPTR	Capabilities Pointer	E4h	RO
35-50h		Reserved		
51h	AGPM	AGP Miscellaneous Config	00h	RW
52-5Bh		Reserved		
5C-5Eh	DQSMRG	DQS Margining Control Register	2F00h	R/W
5Fh		Reserved		
60-63h	DRB[0:3]	DRAM Row Boundary Registers	00000000h	R/W
64-6Fh		Reserved		
70-71h	DRA[0:3]	DRAM Row Attribute Registers	0000h	R/W
72-77h		Reserved		
78-7Bh	DRT	DRAM Timing Register	00000010h	R/W
7C-7Fh	DRC	DRAM Controller Mode Register	10000001h	R/W, RO
80-81h	DRDCTL	DRAM Timing Control Register	0000h	RW
82h	DORC	DRAM Opportunistic Refresh Control	80h	RW
83h	DQSCTL	DQS Control Register	0Ah	RW
83h		Reserved		
84-85h	ECCDIAG	ECC Detection/Correction Diagnostic	0000h	RW

Address Offset	Register Symbol	Register Name	Default Value	Access
86h	DERRSYN	DRAM Error Syndrome Register	00h	RO
87h	DES	DRAM Error Status Register	00h	RO
88-8Bh		Reserved		
8C-8Fh	DEAP	DRAM Error Address Pointer Register	00000000h	RO
90-96h	PAM[0:6]	Programmable Attribute Map Registers	00000000000 000h	RO, R/W
97h	FDHC	Fixed DRAM Hole Control Register	00h	RO, R/W
98-9Ch		Reserved		
9Dh	SMRAM	System Management RAM Control Register	02h	RO, R/W
9Eh	ESMRAMC	Extended System Mgmt RAM Control Register	38h	RO, R/W, RWC
9Fh		Reserved		
A0-A3h	ACAPID	AGP Capability Identifier	00200002h	RO
A4-A7h	AGPSTAT	AGP Status Register	1F000217h	RO
A8-ABh	AGPCMD	AGP Command Register	00000000h	RO, R/W
AC-AFh		Reserved		
B0-B3h	AGPCTRL	AGP Control Register	00000000h	RO, R/W
B4h	APSIZE	Aperture Size	00h	RO, R/W
B5-B7h		Reserved		
B8-BBh	ATTBASE	Aperture Translation Table Base Register	00000000h	RO, R/W
BCh	AMTT	AGP MTT Control Register	00h	RO, R/W
BDh	LPTT	AGP Low Priority Transaction Timer Register	00h	RO, R/W
BE-C3h		Reserved		
C4-C5h	TOM	Top of Low Memory Register	0100h	R/W
C6-C7h	MCHCFG	MCH Configuration Register	0001h	RO, R/W
C8-C9h	ERRSTS	Error Status Register	0000h	RO, R/W
CA-CBh	ERRCMD	Error Command Register	0000h	RO, R/W
CC-CDh	SMICMD	SMI Command Register	0000h	RO, R/W
CE-CFh	SCICMD	SCI Command Register	0000h	RO, R/W
D0-DBh		Reserved		
DCh	WCCTL	Write Cache Control	00h	RO. R/W
DE-DDh		Reserved		
DE-DFh	SKPD	Scratchpad Data Register	0000h	RO, R/W
E0-E3h		Reserved		
E4-E7h	CAPID	Product Specific Capability Identifier	F104_A009h	RO
E7-F3h		Reserved		
F4-F7h	MCHTST	MCH Test Register	8020_F874h	RO, R/W

Address Offset	Register Symbol	Register Name	Default Value	Access
F8-FFh		Reserved		

3.7.1. VID – Vendor Identification Register – Device#0

Address Offset: 00 - 01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.7.2. DID – Device Identification Register – Device#0

Address Offset: 02 - 03h
Default Value: 33 40h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the MCH Host-hub interface Bridge Function #0.

3.7.3. PCICMD – PCI Command Register – Device #0

Address Offset: 04-05h
Default: 0006h
Access: Read/Write, Read Only
Size 16 bits

Since MCH Device #0 does not physically reside on PCI0 many of the bits are not implemented.

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back (RO):** This bit controls whether or not the master can do fast back-to-back write cycle to different targets. Since device #0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no effect.
8	**SERR Enable (SERRE) (R/W):** This bit is a global enable bit for Device #0 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR# condition by sending an SERR message to the ICH4-M. If this bit is set to a 1, the MCH is enabled to generate SERR messages over hub interface for specific Device #0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is reset to 0, then the SERR message is not generated by the MCH for Device #0. **NOTE:** This bit only controls SERR message for the Device #0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices.
7	**Address/Data Stepping (RO):** Address/data stepping is not implemented in the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	**Parity Error Enable (PERRE) (R/W):** PERR# is not implemented by the MCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
5	**VGA Palette Snoop (RO):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	**Memory Write and Invalidate Enable(MWIE) (RO):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
3	**Special Cycle Enable(SCE) (RO):** The MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	**Bus Master Enable (BME) (RO):** The MCH is always enabled as a master on hub interface A. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	**Memory Access Enable (MAE) (RO):** The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	**I/O Access Enable (IOAE) (RO):** This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.

3.7.4. PCISTS – PCI Status Register – Device #0

Address Offset: 06-07h
Default Value: 0090h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #0's on the hub interface. Since MCH Device #0 is the Host-to-hub interface A bridge, many of the bits are not implemented.

Bit	Description
15	**Reserved**
14	**Signaled System Error (SSE) (R/WC):** This bit is set to 1 when MCH Device #0 generates an SERR message over hub interface for any enabled Device #0 error condition. Device #0 error conditions are enabled in the PCICMD and ERRCMD registers. Device #0 error flags are read/reset from the PCISTS or ERRSTS registers. Software sets SSE to 0 by writing a 1 to this bit.
13	**Received Master Abort Status (RMAS) (R/WC);** This bit is set when the MCH generates a hub interface request that receives a Master Abort completion packet or Master Abort Special Cycle. Software clears this bit by writing a 1 to it.
12	**Received Target Abort Status (RTAS) (R/WC):** This bit is set when the MCH generates a hub interface request that receives a Target Abort completion packet or Target Abort Special Cycle. Software clears this bit by writing a 1 to it.
11	**Signaled Target Abort Status (STAS) (RO):** The MCH will not generate a Target Abort hub interface completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	**DEVSEL Timing (DEVT):** Hub interface does not comprehend DEVSEL# protocol. These bits are hardwired to 00. Writes to these bit positions have no effect.
8	**Master Data Parity Error Detected (DPD) (RO):** PERR signaling and messaging are not implemented by the MCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to this bit position have no effect.
6:5	**Reserved**
4	**Capability List (CLIST) (RO):** This bit is set to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the AGP Capability standard register resides.
3:0	**Reserved**

3.7.5. RID – Revision Identification Register – Device #0

Address Offset: 08h
Default Value: 03h
Access: Read Only
Size: 8 bits

This register contains the revision number of the MCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number:** This is an 8-bit value that indicates the revision identification number for the MCH Device #0. For the production stepping, this value is 03h.

3.7.6. SUBC – Sub-Class Code Register – Device #0

Address Offset: 0Ah
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the MCH Device #0. This code is 00h indicating a Host Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. The code is 00h indicating a Host Bridge.

3.7.7. BCC – Base Class Code Register – Device #0

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the MCH Device #0. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the MCH. This code has the value 06h, indicating a Bridge device.

3.7.8. MLT – Master Latency Timer Register – Device #0

Address Offset: 0Dh
Default Value: 00h
Access: Read Only
Size: 8 bits

The hub interface does not comprehend the concept of Master Latency Timer. Therefore, this register is not implemented.

Bit	Description
7:0	These bits are hardwired to 0. Writes have no effect.

3.7.9. HDR – Header Type Register – Device #0

Offset: 0Eh
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space.

Bit	Description
7:0	This read only field always returns 0 when read and writes have no effect.

3.7.10. APBASE – Aperture Base Configuration Register – Device #0

Offset: 10-13h
Default: 0000_0008h
Access: Read/Write, Read Only
Size: 32 bits

The APBASE is a standard PCI Base Address register that is used to set the base of the Graphics Aperture. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0 or behave as hardwired to 0). To allow for flexibility (of the aperture), an additional register called APSIZE is used as a "back-end" register to control which bits of the APBASE will behave as hardwired to 0. This register will be programmed by the MCH specific BIOS code that will run before any of the generic configuration software is run.

Note: The bit 9 of the MCHCFG register is used to prevent accesses to the aperture range before this register is initialized by the configuration software and the appropriate translation table structure has been established in the main memory.

Bit	Description
31:28	**Upper Programmable Base Address (R/W):** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits [31:28] of the base address in the CPU's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write. Default = 0000
27:22	**Middle "Hardwired"/Programmable Base Address:** These bits are part of the aperture base set by configuration software to locate the base address of the graphics aperture. They correspond to bits [27:4] of the base address in the CPU's address space that will cause a graphics aperture translation to be inserted into the path of any memory read or write. These bits can behave as though they were hardwired to 0 if programmed to do so by the APSIZE bits of the APSIZE register. This will cause configuration software to understand that the granularity of the graphics aperture base address is either finer or coarser, depending upon the bits set by MCH-specific configuration software in APSIZE.
21:4	**Lower "Hardwired":** This forces minimum aperture size selected by this register to be 4 MB.
3	**Prefetchable (RO).** This bit is hardwired to 1 to identify the Graphics Aperture range as prefetchable as per the PCI Specification for the base address registers. *There are no side effects on reads, the device returns all bytes on reads regardless of the byte enables, and the MCH may merge processor writes into this range without causing errors.*
2:1	**Type (RO):** These bits determine addressing type and they are hardwired to 00 to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space.
0	**Memory Space Indicator (RO):** Hardwired to 0 to identify aperture range as a memory range.

3.7.11. SMRBASE – System Memory RCOMP Base Address Register – Device #0

Offset: 14-17h
Default: 0000_0000h
Access: Read/Write, Read Only
Size: 32 bits

The SMRBASE is a standard PCI Base Address register that is used to set the base of the Memory Mapped registers used to control the System Memory I/O buffers. The standard PCI Configuration mechanism defines the base address configuration register such that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0). The actual behavior of this register depends on the SMRCOMP MMR Enable bit in the MCHTST register (Device 0 Offset F4h) bit 22. When MCHTST[22] is set, this register behaves like a standard PCI BAR requesting 4 kB of address space. When MCHTST[22] is clear, this register is hardwired to all zeros, effectively disabling the BAR and the corresponding SM MMR region.

Bit	Description
31:12	**Upper Programmable Base Address (UPBITS):** These bits are part of the SM MMR region, normally set by configuration software to locate the base address of the region. The actual behavior of this field depends on the SM MMR Enable bit in the MCHTST register (bit 22) as defined above. When MCHTST[22] = 1, these bits are Read/Write. When MCHTST[22] = 0, these bits are Read-Only as zeros.
11:4	**Lower Bits (LOWBITS):** These bits are hardwired to 0. This forces the size of the memory region to be 4 kB.
3	**Prefetchable (PF):** This bit is hardwired to 0 to indicate that the System Memory MMR region is NON-Prefetchable.
2:1	**Addressing Type (TYPE):** These bits determine addressing type and they are hardwired to 00 to indicate that address range defined by the upper bits of this register can be located anywhere in the 32-bit address space as per the PCI specification for base address registers.
0	**Memory Space Indicator (MSPACE):** Hardwired to 0 to identify the aperture range as a memory range as per the specification for PCI base address registers.

3.7.12. SVID – Subsystem Vendor ID – Device #0

Offset: 2C-2Dh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Description
15:0	**Subsystem Vendor ID (R/WO):** The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.7.13. SID – Subsystem ID – Device #0

Offset: 2E-2Fh
Default: 0000h
Access: Read/Write Once
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Description
15:0	**Subsystem ID (R/WO):** The default value is 00h. This field should be programmed during boot-up. After this field is written once, it becomes read only.

3.7.14. CAPPTR – Capabilities Pointer – Device #0

Offset: 34h
Default: E4h
Access: Read Only
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location where the AGP standard registers are located.

Bit	Description
7:0	**Pointer to the start of AGP standard register block:** This pointer tells software where it can find the beginning of the AGP register block. The value in this field is E4h.

3.7.15. AGPM – AGP Miscellaneous Configuration – Device #0

Offset: 51h
Default: 00h
Access: Read/Write
Size: 8 bits

Bit	Description
7:2	**Reserved**
1	**Aperture Access Global Enable (APEN):** This bit is used to prevent access to the graphics aperture from any port (CPU, HI_A, or AGP/PCI_B) before the aperture range is established by the configuration software and the appropriate translation table in the main DRAM has been initialized. The default value is 0, so this field must be set after system is fully configured in order to enable aperture accesses.
0	**Reserved**

3.7.16. DQSMRG – DQS Margining Control Register – Device #0

Offset: 5Ch
Default: 2F00h
Access: Read/Writew
Size: 16 bits

This register is used to control various aspects of the DQS Margining scheme.

Bit	Description
15:13	**Reserved**
12:8	**DLL Master Select:** Defines how many DLL taps will be used on the Master. The DLL Master will always be matched to ¼ MCLK period. The default for this value is 0Fh (15 decimal). The maximum value allowed for this field is 00111b. HW will ignore any bits set in the 2 MSB bits.
7:0	**Reserved**

3.7.17. DRB – DRAM Row Boundary Register – Device #0

Offset: 60-63h
Default: 00h 00h 00h 00h
Access: Read/Write
Size: 8 bits

The DRAM Row Boundary Register defines the upper boundary address of each pair of DRAM rows with a granularity of 32 MB. Each row has its own single-byte DRB register. For example, a value of 1 in DRB0 indicates that 32 MB of DRAM has been populated in the first row.

Row0: 60h
Row1: 61h
Row2: 62h
Row3: 63h

DRB0 = Total memory in row0 (in 32 MB increments)

DRB1 = Total memory in row0 + row1 (in 32-MB increments)

DRB2 = Total memory in row0 + row1 + row2 (in 32 MB increments)

DRB3 = Total memory in row0 + row1 + row2 + row3 (in 32 MB increments)

Each Row is represented by a byte. Each byte has the following format.

Bit	Description
7:0	**DRAM Row Boundary Address:** This 8-bit value defines the upper and lower addresses for each DRAM row. This 8-bit value is compared against a set of address lines to determine the upper address limit of a particular row.

3.7.18. DRA – DRAM Row Attribute Register – Device #0

Offset: **70-71h**
Default: **00h 00h**
Access: **Read/Write**
Size: **8 bits**

The **DRAM Row Attribute Register** defines the page sizes to be used when accessing different pairs of rows. Since Intel® 855PM MCH supports only same-type technology on each SO-DIMM, then each pair of rows (0-1, 2-3) have to be of the same technology type. To simplify programming, the "Row Attribute for Row 0", 1-inch field will represent the attributes for SO-DIMM0 (rows 0-1) and "Row Attribute for Row 2,3" will represent the attributes for SO-DIMM1 (rows 2-3). Unused SO-DIMMs should be left with their default value (all zeros) for any SO-DIMM that is unpopulated, as determined by the corresponding DRB registers. Note that Intel® 855PM MCH supports only a total of two SO-DIMMs, or four rows.

Each byte of information in the **DRA** registers describes the page size of a pair of rows:

Row0, 1: 70h

Row2, 3: 71h

7	6 4	3	2 0
R	**Reserved**	R	Row Attribute for Row0,1

7	6 4	3	2 0
R	**Reserved**	R	Row Attribute for Row2,3

Bit	Description
7	**Reserved**
6:4	**Reserved**
3	**Reserved**
2:0	**Row Attribute for both rows per SO-DIMM:** This 3-bit field defines the page size of the corresponding row technology for both sides of the SO-DIMM (regardless if it is a single or double-sided SO-DIMM). 001: 2 kB 010: 4 kB 011: 8 kB 100: 16 kB Others: Reserved

3.7.19. DRT – DRAM Timing Register – Device #0

Offset: 78-7Bh
Default: 0000_0010h
Access: Read/Write
Size: 32 bits

This register controls the timing of the DRAM controller

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>31</td><td>Additional CKE to CS Clock for Read/Write: If set to 1, adds one additional clock between CKE and CS for Read or Write on DDR.</td></tr>
<tr><td>30</td><td>Additional CKE to CS clock for Precharge/Activate: If set to 1, adds one additional clock between CKE and CS for Precharge or Activate on DDR.</td></tr>
<tr><td>29</td><td>Back To Back Write-Read Turn Around: This field determines the number of turnaround clocks on the data bus needs to be inserted between WR and RD commands.
DDR-SDRAM
This field applies to WR-RD pairs to different rows only since WR-RD pair to the same row has sufficient turnaround due to tWTR timing parameter.
Write Command to Read Command to Different Rows (Burst Length 4)
<table>
<tr><td>Config</td><td>DDR (tCL 1.5)</td><td>DDR (tCL 2, 2.5)</td></tr>
<tr><td>DRT[29] = 0 (default)</td><td>4</td><td>3</td></tr>
<tr><td>DRT[29] = 1</td><td>3</td><td>2</td></tr>
</table>
Write Command to Read Command to Different Rows (Burst Length 8)
<table>
<tr><td>Config</td><td>DDR (tCL 1.5)</td><td>DDR (tCL 2, 2.5)</td></tr>
<tr><td>DRT[29] = 0 (default)</td><td>6</td><td>5</td></tr>
<tr><td>DRT[29] = 1</td><td>5</td><td>4</td></tr>
</table>
Recommended BIOS value is 1 for all values of CL. Note that write to read delays are automatically 1 clock larger with Cas latency 1.5 than for Cas latency 2 or 2.5 with the same setting of DRT[29].</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>28</td><td>
Back-To-Back Read-Write Turn Around: This field controls the turnaround time on the DQ bus for RD-WR pairs.
Read Command to Write Command (Burst Length 4)
<table>
<tr><td colspan="2">Config</td><td>DDR</td></tr>
<tr><td>DRT[28] = 0 (default)</td><td>MRGCNT = 0 (default)</td><td>5</td></tr>
<tr><td>DRT[28] = 0 (default)</td><td>MRGCNT = 1</td><td>6</td></tr>
<tr><td>DRT[28] = 1</td><td>MRGCNT = 0 (default)</td><td>4</td></tr>
<tr><td>DRT[28] = 1</td><td>MRGCNT = 1</td><td>6</td></tr>
</table>
Read Command to Write Command (Burst Length 8)
<table>
<tr><td colspan="2">Config</td><td>DDR</td></tr>
<tr><td>DRT[28] = 0 (default)</td><td>MRGCNT = 0 (default)</td><td>7</td></tr>
<tr><td>DRT[28] = 0 (default)</td><td>MRGCNT = 1</td><td>8</td></tr>
<tr><td>DRT[28] = 1</td><td>MRGCNT = 0 (default)</td><td>6</td></tr>
<tr><td>DRT[28] = 1</td><td>MRGCNT = 1</td><td>8</td></tr>
</table>
Note that Turn-Around of 5 clocks is required (independent of loading) when CL=2.5, for DDR. Furthermore, the total turn around time may be increased by 1 MCLK by setting bit 14 of the DQS Margining Control Register (Dev 0 Offset 5Ch).
Recommended BIOS value is 0 for CL=2.5 and 1 for CL=1.5 and 2.
</td></tr>
<tr><td>27</td><td>
Back-To-Back Read Turn Around: This field controls the turnaround time on the DQ bus for RD-RD sequence to different rows.
Read Command to Read Command with Different Row and Bank (Burst Length 4)
<table>
<tr><td>Config</td><td>DDR</td></tr>
<tr><td>DRT[27] = 0 (default)</td><td>4</td></tr>
<tr><td>DRT[27] = 1</td><td>3</td></tr>
</table>
Read Command to Read Command with Different Row and Bank (Burst Length 8)
<table>
<tr><td>Config</td><td>DDR</td></tr>
<tr><td>DRT[27] = 0 (default)</td><td>6</td></tr>
<tr><td>DRT[27] = 1</td><td>5</td></tr>
</table>
The bigger turn-around is used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.
Recommended BIOS value is 1 for all configurations.
</td></tr>
</table>

Bit	Description
26:24	**Read Delay (tRD):** tRD represents the time elapsed from the internal MCLK rising (for which command is sent) until the first 16B of data are available to be returned to the Core clock domain. FOR DDR: The tRD is calculated by adding the following components and rounding the sum to next integer number: • ½ clock: time from internal MCLK rising (for which command is driven) to CK (command clock) rising. CAS latency: 1.5, 2, 2.5 Un-buffered SO-DIMM Total external propagation delay (flight time to and from SO-DIMM). ½ clock (5nS): time between the arrival of even an odd data, from DRAM. Refer to detailed analysis in following table. The range is based on min-max, rounded up to nearest integer calculations: 3 – 8 clocks. The following tRD values are supported: Encoding tRD 000: 9 DRAM common clocks 001: 8 DRAM common clocks 010: 7 DRAM common clocks 011: 6 DRAM common clocks 100: 5 DRAM common clocks 101: 4 DRAM common clocks 110: 3 DRAM common clocks others: reserved Note that clock domain crossing delay is not taken into account in tRD calculations. It reflects only the static delay as measured in the DUNIT, at DRAM clock domain. A DUNIT internal signal is used to cross into clock-domain, synchronized to core clock domain, to indicate data arrival. The delay of cross clocking is dynamic, i.e. varies with clock phases. Recommended BIOS value for this field is TBD.
23:20	**Reserved**
19	**No wake for DDR page closes:** When this bit is 1 page, close operations due to timeouts will only be done during the data phase of normal read/write accesses when no operations are present. If this bit is 0 (Default), page close operations due to timeouts may be done at any point when no new memory requests are pending.
18:16	**Page-Close Counter:** This field enables proactive timed page closure and determines the timeout from the last activity until the page is closed. Countdown is performed in core-clocks (MCH main clock). MCH will initiate page closure opportunistically after the counter expires, i.e. if the memory interface is active and idle due to data transactions. 000: Timed page closure is disabled. No proactive page-closure is done 001: Pages are tagged for closure 4-7 clocks after the last transaction to a row 010: Pages are tagged for closure 8-15 clocks after the last transaction to a row 011: Pages are tagged for closure 16-31 clocks after the last transaction to a row 100: Pages are tagged for closure 64-127 clocks after the last transaction to a row 101: Pages are tagged for closure 128-255 clocks after the last transaction to a row 110: Pages are tagged for closure 192-383 clocks after the last transaction to a row 111: Pages are tagged for closure 255-510 clocks after the last transaction to a row
15:11	**Reserved**

Bit	Description
11	**DQS Slave DLL Dynamic Management:** Determines if the memory controller disables the Slave DLLs when no memory-read transactions are pending. This is a power saving feature. When set to 1, the slave-DLLs will be disabled after the last read is done, and reactivated before the next read is due. When set to 0, the slave-DLLs will be continuously active during C0-C2 states.
10:9	**Activate to Precharge delay (tRAS):** This bit controls the number of DRAM clocks for tRAS. **00** 7 Clocks **01** 6 Clocks **10** 5 Clocks **11** Reserved
8:6	**Reserved**
5:4	**CAS# Latency (tCL):** **Encoding** **DDR CL** 00: 2.5 01: 2 (default) 10: 1.5 11: Reserved
3	**Reserved**
2	**DRAM RAS# to CAS# Delay (tRCD):** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. **Encoding** **tRCD** 0: 3 DRAM Clocks 1: 2 DRAM Clocks
1	**Reserved**
0	**DRAM RAS# Precharge (tRP):** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same row. **Encoding** **tRP** 0: 3 DRAM Clocks 1: 2 DRAM Clocks

3.7.20. DRC – DRAM Controller Mode Register – Device #0

Offset: 7C-7Fh
Default: 1000_0001h
Access: Read/Write
Size: 32 bits

Bit	Description
31:30	**Revision Number (REV):** Reflects the revision number of the format used for DDR register definition. Currently, this field must be 00, since this (rev 00) is the only existing version of the specification.
29	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28	**Dynamic Power-down mode Enable:** When set, the DRAM controller will put pair of rows into power down mode when all banks are pre-charged (closed). For DDR, row active power-down will be done at the end of a transaction if no more transactions are pending for that row. Once a bank is accessed, the relevant pair of rows is taken out of Power Down mode. The entry into power down mode is performed by de-activation of CKE. The exit is performed by activation of CKE. 0: DRAM Power-down disabled 1: DRAM Power-down enabled
27:24	**Reserved**
23	**Reduced Command Drive Delay:** Only used when DRC[22] enables the reduced drive strength. Defines how long a new value must be driven on a command bit before the reduced strength will be engaged. When this bit is set to 0 (default) a new value will be driven for 2 clocks with the normal strength before using the reduced strength. When this bit is set to 1 a new value will be driven for 3 clocks with the normal strength before using the reduced strength.
22	**Reduced Command Drive Enable:** Enables reduced strength drive. When this bit is set to 1, the memory controller will use different strength values specified in device 0 MMR registers 0x35 and as the strength of the output buffer for any command bits (MA[13:0], BS[1:0], RAS#, CAS#, WE#) that have not changed for 2 or 3 cycles (as specified by DRC[23]) after they are initially driven. When this bit is 0 (default), the strength is always specified by the normal command signal strength.
21	**DRAM Data Integrity Mode (DDIM):** These bits select one of two DRAM data integrity modes. **DDIM Operation** **0:** Non-ECC mode **1:** Error checking with correction.
20	**Reserved.**
19:18	**DRB Granularity (DRBG):** The value in the DRBG field sets the meaning given to the values in the set of DRB registers. **00:** Numbers in DRB registers represent 32 MB quantities **Other:** Reserved
17	**Reserved**
16	**Disable SCK Tri-State in C3/S1-m:** If set to 1, SCK for populated rows will be held low during C3/S1-m. If left as 0, SCK for populated rows will be tri-stated in C3/S1-m.
15:14	**Reserved**
13	**Dynamic CS disable:** 1: CS to a device whose CKE is deasserted to be tri-stated in C0. 0: CS is enabled and disabled as necessary (always driven)

Bit	Description
12	**SM Interface Tristate Enable:** When set, the MCH will tristate the address and control lines to the DDR if all rows have been put in active power down or self refresh.
11	**Reserved**
10:8	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. **000:** Refresh disabled **001:** Refresh enabled. Refresh interval 15.6 μsec **010:** Refresh enabled. Refresh interval 7.8 μsec **011:** Refresh enabled. Refresh interval 64 μsec **111:** Reserved Other: ***Reserved*** This bit-field has a special test function. When a value of 000 is written, the refresh counter is preset to its known value. This function is added for testing purposes, it allows test program to align refresh events with the test and thus improve failure repeatability. Otherwise SW should never write 000 to this field as disabling Refresh (entering self-refresh mode) is always exclusively under HW control.
7	**Reserved**
6:4	**Mode Select (SMS):** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. **000**: Post Reset state – When the MCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the MCH asserts all CKE signals. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During suspend, MCH internal signal triggers DRAM controller to flush pending commands and enter all rows into Self-Refresh mode. As part of resume sequence, MCH will be reset – which will clear this bit field to 000 and maintain CKE signals deasserted. After internal reset is deasserted, CKE signals remain deasserted until this field is written to a value different than 000. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), MCH internal signal triggers DRAM controller to flush pending commands and enter all rows into Self-Refresh mode. During exit to normal mode, MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. **001:** NOP Command Enable – All CPU cycles to DRAM result in a NOP command on the DRAM interface. **010:** All Banks Pre-charge Enable – All CPU cycles to DRAM result in an “all banks precharge” command on the DRAM interface. **011:** Mode Register Set Enable – All CPU cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to memory address lines in order to specify the command sent. Host address lines [15:3] are mapped to MA[12:0]. **100:** Extended Mode Register Set Enable – All processor cycles to SDRAM result in an “extended mode register set” command on the DRAM interface (DDR only). Host address lines are mapped to DDR address lines in order to specify the command sent. Host address lines [15:3] are mapped to MA[12:0]. **101: Reserved** **110:** CBR Refresh Enable – In this mode all CPU cycles to DRAM result in a CBR cycle on the DDR interface **111:** Normal operation
3:1	**Reserved**
0	**DT:** DRAM Type (hardwired to 1 to indicate DDR SDRAM)

3.7.21. DRDCTL – DRAM Read Timing Control Register – Device #0

Offset: 80-81h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:9	**Reserved**
8:4	**RCVEN/RDCLK Fine Tune Timing Control:** This field selects the number of delays added in the RCVEN output path. This delay is added in series to the whole and quarter MCLK delays which are programmed in bits [1:0] and [3:2]. This field is used for DIMM0, and also DIMM1 if DRDCTL[15] is not set. Maximum value for this field is 00111.
3:2	**RCVEN/RDCLK Quarter-Clock Timing Control:** This field selects the number of 200 MHz/266 MHz phase delays that is added in the RCVEN output path. This delay is added in serial to the 10/7.5 nS delay which is programmed in bits[1:0]. 00: 5.0 ns / 3.75 ns 01: 7.5 ns / 5.625 ns 10: 10.0 ns/ 7.5 ns 11: 12.5 ns/ 9.375 ns This bit field is programmed by BIOS, based on CAS latency.
1:0	**RCVEN/RDCLK Timing Control:** This field selects the number of 100 MHz/133 MHz clock delay from the rising edge of the clock of which READ command is driven to the internal clock of which RCVEN output is driven 00: 1 clocks (10/7.5 ns) 01: 2 clocks (20/15 ns) 10: 3 clocks (30/22.5 ns) This bit field will be set by BIOS based on SO-DIMM configurations (including CAS latency).

3.7.22. DORC – DRAM Opportunistic Refresh Control Register – Device #0

Offset: 82h
Default: 80h
Access: Read/Write
Size: 8 bits

Intel® 855PM MCH contains a 4b refresh counter that allows the counting of up to 16 refreshes. Using the counter, refresh requests can be queued when the DRAM interface is busy performing cycles. When the number of outstanding refreshes reaches the high watermark they are all performed in a burst.

Bit	Description
7:4	**High Watermark:** When the refresh-counter reaches or exceeds the value in the high watermark field, the DRAM controller performs all pending refreshes in a burst. This value times the refresh rate must not exceed tRASmax (typically 120 µs). Note that current DDR-SDRAM components require DLL refresh every 9 refresh periods. As a result, High Watermark for DDR must be set to the lowest of either 8, or the value, which meets the tRASmax criteria. The default setting of the high watermark is 8h.
3:0	**Reserved**

3.7.23. DQSCTL – DQS Control Register – Device #0

Offset: 83h
Default: 0Ah
Access: Read/Write
Size: 8 bits

Bit	Description
7:5	**Reserved**
4:0	**DQS Delay (DQSDLY):** This five-bit field specifies the delay which will be added to DQS so that read data has sufficient setup and hold time. This field affects DQS on reads only. The DDR DRAMs drive data for MCLK Period / 2 (5 ns for DDR200, 3.75 ns for DDR266). DQS edges are driven at the same time as data is driven. Therefore DQS must be delayed by some amount so that it can be used to sample DQ. Valid values for this field are 00000-00111. All other values are reserved.

3.7.24. ECCDIAG - ECC Diagnostic Control Register – Device #0

Offset: 84h
Default: 0000h
Access: Read/Write
Size: 16 bits

The ECC diagnostic register is used to test the ECC detection and correction hardware in MCH.

Bit	Description
15	**ECC diagnostic enable:** When set to 1, the ECC bit invert vector is used to invert selected ECC bits, during writes to DRAM. Otherwise, the diagnostic feature is turned off.
14:8	**Reserved**
7:0	**ECC bit invert vector:** This vector operates individually for every ECC bit in the selected 64b ECC block, during write to DRAM. For all k between 0 and 7, when bit (k) set to 1, the value for the k ECC bit (which corresponds with the k data byte lane) is inverted. Otherwise, the value for the k ECC bit is not affected.

3.7.25. DERRSYN – DRAM Error Syndrome Register – Device #0

Address Offset: 86h
Default Value: 00h
Access: Read Only
Size: 8 bits

This register is used to report the ECC syndromes for each quadword of a 32B-aligned data quantity read from the DRAM array.

Bit	Description
7:0	**DRAM ECC Syndrome (DECCSYN) (RO):** After a DRAM ECC error, hardware loads this field with a syndrome that describes the set of bits found to be in error. Note that this field is locked from the time that it is loaded up to the time when the error flag is cleared by software. If the first error was a single bit, correctable error, then a subsequent multiple bit error will overwrite this field. In all other cases, an error that occurs after the first error and before the error flag has been cleared by software will escape recording.

3.7.26. DES – DRAM Error Status Register – Device #0

Address Offset: 87h
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the address of the 32-B block on which DRAM ECC error(s) was detected.

Bit	Description
7:4	**Reserved**
3:2	**QW Indicator:** This field indicates the QuadWord of data that actually caused the ECC error, within the 32 Byte chunk of data pointed to by the DEAP register. The encoding is: 00 = First QuadWord 01 = Second QuadWord 10 = Third QuadWord 11 = Fourth QuadWord Note that this field represents the order that the data was read from DRAM, which is not necessarily the order of the QuadWord within the 32-Byte chunk of memory (due to X86 burst ordering). If ECC errors exist on multiple quadwords of data only the earliest one will be indicated.
1	**Error Type:** This bit reports whether the error reported is a single bit or a multiple bit error. If a multiple bit error occurs after a single bit error has already been captured, this field will be updated to a 1, and the QW Indicator field, the DESYN and DEAP registers will all be updated to reflect this new multibit error. 0 = Single-bit Error (or no error) Detected 1 = Multi-bit (uncorrectable) Error Detected
0	**Error Occurred:** This bit is set if an ECC error has been detected. The type of error can be determined by the Error Type field (above). The syndrome and address of the error can be determined in the DRAM Error Syndrome and DRAM Error Address Pointer registers defined below. Once set, this bit can only be cleared by clearing the appropriate fields of the Error Status Register (Device 0, Offset C8h, bits 1:0). 0 = No ECC Errors Detected 1 = At least one ECC Error Detected

3.7.27. DEAP – DRAM Error Address Pointer Register – Device #0

Address Offset: 8C-8Fh
Default Value: 0000_0000h
Access: Read Only
Size: 32 bits

This register stores the DRAM address of the 32B-aligned data unit on which DRAM ECC error(s) was detected.

Bit	Description
31:28	**Reserved**
27:1	**Error Address Pointer (EAP) (RO):** This field is used to store address bits A[31:5] of the 32B-aligned data unit of main memory of which an error (single bit or multi-bit error) has occurred. Note that the value of this bit field represents the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and doesn't change as a result of a new error until the error field is cleared by software.
0	**Reserved**

3.7.28. PAM[0:6] – Programmable Attribute Map Registers – Device #0

Address Offset: 90-96h
Default Value: 00h
Attribute: Read/Write, Read Only
Size: 8 bits

This register controls the read, write and shadowing attributes of the BIOS area from 0F0000h-0FFFFFh. The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 640 kbytes to 1 Mbytes address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to host initiator only access to the PAM areas. MCH will forward to main memory any AGP, PCI, or hub interface A initiated accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the host (CPU) read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI0.

WE - Write Enable. When WE = 1, the host (CPU) write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI0.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 Kbytes in size. Each of these regions has a 4-bit field. The four bits that control each region have the same encoding and are defined in the following table.

Table 24. Control Signals for Various Memory Segments

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	**Disabled.** DRAM is disabled and all accesses are directed to the hub interface A. The MCH does not respond as a PCI target for any read or write access to this area.
X	X	0	1	**Read Only.** Reads are forwarded to DRAM and writes are forwarded to the hub interface A for termination. This write protects the corresponding memory segment. The MCH will respond as an AGP or the hub interface A target for read accesses but not for any write accesses.
X	X	1	0	**Write Only.** Writes are forwarded to DRAM and reads are forwarded to the hub interface for termination. The MCH will respond as an AGP or hub interface. A target for write accesses but not for any read accesses.
X	X	1	1	**Read/Write.** This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by the MCH and forwarded to DRAM. The MCH will respond as an AGP or the hub interface A target for both read and write accesses.

At the time that a hub interface or AGP accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

As an example, consider BIOS that is implemented on the expansion bus. During the initialization process, the BIOS can be shadowed in main memory to increase the system performance. When BIOS is shadowed in main memory, it should be copied to the same address location. To shadow the BIOS, the attributes for that address range should be set to write only. The BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After the BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus. Figure 3 and Table 25 below shows the PAM registers and the associated attribute bits.

Figure 3. PAM Register Attributes

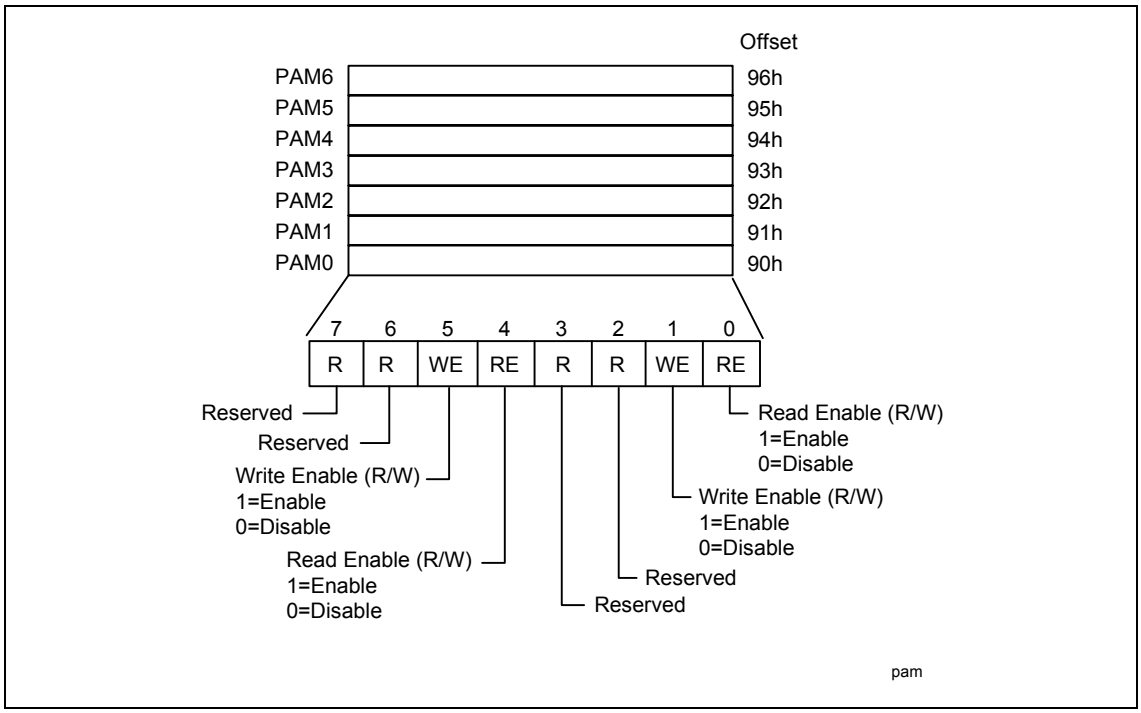


Table 25. PAM Register Details

PAM Reg	Attribute Bits				BIOS Area (Memory Segment)	Offset
PAM0[3:0]	Reserved				-	90h
PAM0[7:4]	R	R	WE	RE	0F0000h - 0FFFFFh	90h
PAM1[3:0]	R	R	WE	RE	0C0000h - 0C3FFFh	91h
PAM1[7:4]	R	R	WE	RE	0C4000h - 0C7FFFh	91h
PAM2[3:0]	R	R	WE	RE	0C8000h - 0CBFFFh	92h
PAM2[7:4]	R	R	WE	RE	0CC000h- 0CFFFFh	92h
PAM3[3:0]	R	R	WE	RE	0D0000h- 0D3FFFh	93h
PAM3[7:4]	R	R	WE	RE	0D4000h- 0D7FFFh	93h
PAM4[3:0]	R	R	WE	RE	0D8000h- 0DBFFFh	94h
PAM4[7:4]	R	R	WE	RE	0DC000h- 0DFFFFh	94h
PAM5[3:0]	R	R	WE	RE	0E0000h- 0E3FFFh	95h
PAM5[7:4]	R	R	WE	RE	0E4000h- 0E7FFFh	95h
PAM6[3:0]	R	R	WE	RE	0E8000h- 0EBFFFh	96h
PAM6[7:4]	R	R	WE	RE	0EC000h- 0EFFFFh	96h

For details on overall system address mapping scheme see the Address Decoding section of this document.

DOS Application Area (00000h-9FFFh)

The DOS area is 640 kB in size and it is further divided into two parts. The 512- kB area at 0 to 7FFFFh is always mapped to the main memory controlled by the MCH, while the 128- kB address range from 080000 to 09FFFFh can be mapped to PCI0 or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI0) via MCH FDHC configuration register.

Video Buffer Area (A0000h-BFFFFh)

Attribute bits do not control this 128-kB area. The host -initiated cycles in this region are always forwarded to either PCI0 or AGP unless this range is accessed in SMM mode. Routing of accesses is controlled by the Legacy VGA control mechanism of the “virtual” PCI-PCI bridge device embedded within the MCH.

This area can be programmed as SMM area via the SMRAM register. When used as a SMM space this range cannot be accessed from the hub interface or AGP.

Expansion Area (C0000h-DFFFFh)

This 128-kB area is divided into eight 16-kB segments, which can be assigned with different attributes via PAM control register as defined by Table 25.

Extended System BIOS Area (E0000h-EFFFFh)

This 64-kB area is divided into four 16-kB segments which can be assigned with different attributes via PAM control register as defined by Table 25.

System BIOS Area (F0000h-FFFFFh)

This area is a single 64-kB segment, which can be assigned with different attributes via PAM control register as defined by Table 25.

3.7.29. FDHC – Fixed DRAM Hole Control Register – Device #0

Address Offset: 97h
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

This 8-bit register controls a fixed DRAM hole: 15-16 MB.

Bit	Description
7	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to ICH4-M through the hub interface. The hub interface cycles matching an enabled hole will be ignored by the MCH. Note that a selected hole is not re-mapped. Bits[7] Hole Enabled 0 None 1 15M-16M (1 MB)
6:0	**Reserved**

3.7.30. SMRAM – System Management RAM Control Register – Device #0

Address Offset: 9Dh
Default Value: 02h
Access: Read/Write, Read Only, Lock
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Description
7	**Reserved**
6	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. When D_LCK is set to a 1, D_OPEN is reset to 0 and becomes read only.
5	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference “through” SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become “Read Only”. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions is enabled, providing 128 kB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode). To enable Extended SMRAM function this bit has to be set to 1. Once D_LCK is set, this bit becomes read only.
2:0	**Compatible SMM Space Base Segment (C_BASE_SEG) (RO):** This field indicates the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space, otherwise the access is forwarded to the hub interface. C_BASE_SEG is hardwired to 010 to indicate that the MCH supports the SMM space at A0000h-BFFFFh.

3.7.31. ESMRAMC – Extended System Mgmt RAM Control Register – Device #0

Address Offset: 9Eh
Default Value: 38h
Access: Read Only, Read/Write, Read/Write Clear, Lock
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MByte.

Note: When Extended SMRAM is used, the maximum amount of DRAM accessible is limited to 256 MB.

Bit	Description
7	**Enable High SMRAM H_SMRAM_EN (H_SMRAME):** Controls the SMM memory space location (i.e. above 1 MByte or below 1 MByte) When G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses from FEDA_0000h to FEDB_FFFFh are remapped to DRAM address 000A0000h to 000BFFFFh. Once D_LCK is set, this bit becomes read only.
6	**Invalid SMRAM Access E_SMRAM_ERR (E_SMERR):** This bit is set when host accesses the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it
5	**SMRAM Cacheable (SM_CACHE):** This bit is hardwired to 1.
4	**L1 Cache Enable for SMRAM SMRAM_L1_EN (SM_L1):** This bit is hardwired to 1.
3	**L2 Cache Enable for SMRAM SMRAM_L2_EN (SM_L2):** This bit is hardwired to 1.
2:1	**TSEG Size TSEG_SZ[1-0] (T_SZ):** Selects the size of the TSEG memory block if enabled. This memory is taken from the top of DRAM space (i.e. TOM - TSEG_SZ), which is no longer claimed by the memory controller (all accesses to this space are sent to the hub interface if TSEG_EN is set). This field decodes as follows: **TSEG_SZ[1,0] Description** 00 (TOM-128K) to TOM 01 (TOM-256K) to TOM 10 (TOM-512K) to TOM 11 (TOM-1M) to TOM Once D_LCK is set, this bit becomes read only.
0	**TSEG Enable TSEG_EN (T_EN):** Enabling of SMRAM memory (TSEG, 128 kbytes, 256 kbytes, 512 Kbytes or 1 Mbytes of additional SMRAM memory) for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Once D_LCK is set, this bit becomes read only.

3.7.32. ACAPID – AGP Capability Identifier Register – Device #0

Address Offset: A0-A3h
Default Value: 0020_0002h
Access: Read Only
Size: 32 bits

This register provides standard identifier for AGP capability.

Bit	Description
31:24	**Reserved**
23:20	**Major AGP Revision Number (MAJREV):** These bits provide a major revision number of AGP specification to which this version of MCH conforms. This field is hardwired to value of “0010b” (i.e. implying Rev 2.x).
19:16	**Minor AGP Revision Number (MINREV):** These bits provide a minor revision number of AGP specification to which this version of MCH conforms. This number is hardwired to value of “0000” (i.e. implying Rev x.0). Together with major revision number, this field identifies MCH as an AGP REV 2.0 compliant device.
15:8	**Next Capability Pointer (NCAPTR):** AGP capability is the first and the last capability described via the capability pointer mechanism and therefore these bits are hardwired to 0 to indicate the end of the capability linked list.
7:0	**AGP Capability ID (CAPID):** This field identifies the linked list item as containing AGP registers. This field has a value of 0000_0010b assigned by the PCI SIG.

3.7.33. AGPSTAT – AGP Status Register – Device #0

Address Offset: A4-A7h
Default Value: 1F00_0217h
Access: Read Only
Size: 32 bits

This register reports AGP device capability/status.

Bit	Description
31:24	**Request Queue (RQ):** This field is hardwired to 1Fh to indicate a maximum of 32 outstanding AGP command requests can be handled by the MCH. This field contains the maximum number of AGP command requests the MCH is configured to manage. Default =1Fh to allow a maximum of 32 outstanding AGP command requests.
23:10	**Reserved**
9	**Side Band Addressing Support (SBA):** This bit indicates that the MCH supports side band addressing. It is hardwired to 1.
8:6	**Reserved**
5	**Greater that 4 GB Support (4 GB):** This bit indicates that the MCH does not support addresses greater than 4 gigabytes. It is hardwired to 0.
4	**Fast Write Support (FW):** This bit indicates that the MCH supports Fast Writes from the host to the AGP master. It is hardwired to a 1.
3	**Reserved**
2:0	**Data Rate Support (RATE):** After reset the MCH reports its data transfer rate capability. Bit 0 identifies if AGP device supports 1x data transfer mode, bit 1 identifies if AGP device supports 2x data transfer mode, bit 2 identifies if AGP device supports 4x data transfer mode. 1x, 2x, and 4x data transfer modes are supported by the MCH and therefore this bit field has a Default Value = 111. Note that the selected data transfer mode applies to both AD bus and SBA bus. It also applies to Fast Writes if they are enabled.

3.7.34. AGPCMD – AGP Command Register – Device #0

Address Offset: A8-ABh
Default Value: 0000_0000h
Access: Read/Write, Read Only
Size: 32 bits

This register provides control of the AGP operational parameters.

Bit	Description
31:10	**Reserved**
9	**SBA Enable (SBAEN):** When this bit is set to 1, the side band addressing mechanism is enabled.
8	**AGP Enable (AGPEN):** When this bit is reset to 0, the MCH will ignore all AGP operations, including the sync cycle. Any AGP operations received while this bit is set to 1 will be serviced even if this bit is reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode the command will be issued. When this bit is set to 1 the MCH will respond to AGP operations delivered via PIPE#, or to operations delivered via SBA if the AGP Side Band Enable bit is also set to 1.
7:5	**Reserved**
4	**FW Enable (FWEN):** When this bit is set, the MCH will use the Fast Write protocol for Memory Write transactions from the MCH to the AGP master. Fast Writes will occur at the data transfer rate selected by the data rate bits (2:0) in this register. When this bit is cleared, or when the data rate bits are set to 1x mode, the Memory Write transactions from the MCH to the AGP master use standard PCI protocol.
3	**Reserved**
2:0	**Data Rate (DRATE):** The settings of these bits determine the AGP data transfer rate. One (and only one) bit in this field must be set to indicate the desired data transfer rate. **Encoding Description** 0 0 1 1x transfer mode 0 1 0 2x transfer mode 1 0 0 4x transfer mode Configuration software will update this field by setting only one bit that corresponds to the capability of AGP master (after that capability has been verified by accessing the same functional register within the AGP masters' configuration space). **NOTE:** This field applies to AD and SBA buses. It also applies to Fast Writes if they are enabled.

3.7.35. AGPCTRL – AGP Control Register

Address Offset: B0-B3h
Default Value: 0000_0000h
Access: Read/Write, Read Only
Size: 32 bits

This register provides for additional control of the AGP interface.

Bit	Description
31:8	**Reserved**
7	**GTLB Enable (and GTLB Flush Control) (R/W):** When this bit is set, it enables normal operations of the Graphics Translation Lookaside buffer. If it is zero, the GTLB is flushed by clearing the valid bits associated with each entry. Default=0 (GTLB disabled)
6:1	**Reserved**
0	**Reserved**

3.7.36. APSIZE – Aperture Size – Device #0

Address Offset: B4h
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

This register determines the effective size of the Graphics Aperture used for a particular MCH configuration. This register can be updated by the MCH specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated then a default value will select an aperture of maximum size (i.e. 256 MB). The size of the table that will correspond to a 256-MB aperture is not practical for most applications and therefore, these bits must be programmed to a smaller practical value that will force adequate address range to be requested via APBASE register from the PCI configuration software.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Aperture Size (APSIZE) (R/W):** Each bit in APSIZE[5:0] operates on similarly ordered bits in APBASE[27:22] of the Aperture Base configuration register. When a particular bit of this field is 0 it forces the similarly ordered bit in APBASE[27:22] to behave as "hardwired" to 0. When a particular bit of this field is set to 1 it allows corresponding bit of the APBASE[27:22] to be read/write accessible. Only the following combinations are allowed: 5 4 3 2 1 0 Aperture Size 1 1 1 1 1 1 4 MB 1 1 1 1 1 0 8 MB 1 1 1 1 0 0 16 MB 1 1 1 0 0 0 32 MB 1 1 0 0 0 0 64 MB 1 0 0 0 0 0 128 MB 0 0 0 0 0 0 256 MB Default for APSIZE[5:0]=000000b forces default APBASE[27:22] =000000b (i.e. all bits respond as "hardwired" to 0). This provides maximum aperture size of 256 MB. As another example, programming APSIZE[5:0]=111000b hardwires APBASE[24:22]=000b and while enabling APBASE[27:25] as read/write

3.7.37. ATTBASE – Aperture Translation Table Base Register – Device #0

Address Offset: B8-BBh
Default Value: 0000_0000h
Access: Read/Write, Read Only
Size: 32 bits

This register provides the starting address of the Graphics Aperture Translation Table Base located in the main DRAM. This value is used by the MCH Graphics Aperture address translation logic (including the GTLB logic) to obtain the appropriate address translation entry required during the translation of the aperture address into a corresponding physical DRAM address. The ATTBASE register may be dynamically changed.

Note: The address provided via ATTBASE is 4-kB aligned.

Bit	Description
31:12	**Aperture Translation Table Base (TTABLE):** This field contains a pointer to the base of the translation table used to map memory space addresses in the aperture range to addresses in main memory. **NOTE:** This field should be modified only when the GTLB is disabled.
11:0	**Reserved**

3.7.38. AMTT – AGP Interface Multi-Transaction Timer Register – Device #0

Address Offset: BCh
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

AMTT is an 8-bit register that controls the amount of time that the MCH arbiter allows AGP master to perform multiple back-to-back transactions. The MCH AMTT mechanism is used to optimize the performance of the AGP master (using PCI protocol) that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers). The AMTT mechanism applies to the host-AGP transactions as well and it guarantees to the processor a fair share of the AGP interface bandwidth.

The number of clocks programmed in the AMTT represents the guaranteed time slice (measured in 66-MHz clocks) allotted to the current agent (either AGP master or Host bridge) after which the AGP arbiter will grant the bus to another agent. The default value of AMTT is 00h and disables this function. The AMTT value can be programmed with 8-clock granularity. For example, if the AMTT is programmed to 18h, then the selected value corresponds to the time period of 24 AGP (66 MHz) clocks.

Bit	Description
7:3	**Multi-Transaction Timer Count Value (MTTC):** The number programmed in these bits represents the guaranteed time slice (measured in eight 66-MHz clock granularity) allotted to the current agent (either AGP master or MCH) after which the AGP arbiter will grant the bus to another agent.
2:0	**Reserved**

3.7.39. LPTT – AGP Low Priority Transaction Timer Register – Device #0

Address Offset: BDh
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

LPTT is an 8-bit register similar in a function to AMTT. This register is used to control the minimum tenure on the AGP for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms.

The number of clocks programmed in the LPTT represents the guaranteed time slice (measured in 66-MHz clocks) allotted to the current low priority AGP transaction data transfer state. This does not necessarily apply to a single transaction but it can span over multiple low-priority transactions of the same type. After this time expires the AGP arbiter may grant the bus to another agent if there is a pending request. The LPTT does not apply in the case of high-priority request where ownership is transferred directly to high-priority requesting queue. The default value of LPTT is 00h and disables this function. The LPTT value can be programmed with 8-clock granularity. For example, if the LPTT is programmed to 10h, then the selected value corresponds to the time period of 16 AGP (66 MHz) clocks.

Bit	Description
7:3	**Low Priority Transaction Timer Count Value (LPTTC):** The number of clocks programmed in these bits represents the guaranteed time slice (measured in eight 66-MHz clock granularity) allotted to the current low priority AGP transaction data transfer state).
2:0	**Reserved**

3.7.40. TOM – Top of Low Memory Register – Device #0

Address Offset: C4-C5h
Default Value: 0100h
Access: Read/Write
Size: 16 bits

This register contains the maximum address below 4 GB that should be treated as a memory access. Note that this register must be set to a value of 0100h (16 MB) or greater. Usually it will sit below the areas configured for the hub interface, PCI memory, and the graphics aperture.

Bit	Description
15:4	**Top of Low Memory (TOM):** This register contains the address that corresponds to bits 31 to 20 of the maximum DRAM memory address that lies below 4 GB. Configuration software should set this value to either the maximum amount of memory in the system or to the minimum address allocated for PCI memory or the graphics aperture, whichever is smaller. Programming example: 400h = 1 GB. An access to 4000_0000h or above will be considered above the TOM and therefore not routed to DRAM. It may go to AGP, aperture, or HI.
3:0	**Reserved**

3.7.41. MCHCFG – MCH Configuration Register – Device #0

Offset: C6-C7h
Default: 0001h
Access: Read/Write Once, Read/Write, Read Only
Size: 16 bits

Bit	Description
15:12	**Reserved**
11	**System Memory Frequency Select:** This bit must be programmed prior to memory initialization. 0: System Memory frequency is set to support 200 MHz DDR memory. 1: System Memory frequency is set to support 266 MHz DDR memory.
10:6	**Reserved**
5	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh are forwarded to HI_A. If the VGA enable bit is not set then accesses to IO address range x3BCh-x3BFh are treated just like any other IO accesses i.e. the cycles are forwarded to AGP if the address is within the corresponding IOBASE and IOLIMIT and ISA enable bit is not set, otherwise they are forwarded to HI_A. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to hub interface even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: VGA / MDA / Behavior 0 / 0 / All references to MGA and VGA go to HI_A 0 / 1 / Illegal combination, (DO NOT USE) 1 / 0 / All references to VGA go to device 1. MDA-only references (I/O address 3BF and aliases) will go to HI_A. 1 / 1 / VGA references go to AGP/PCI; MDA References go to HI_A
4:3	**Reserved**
2	**In-Order Queue Depth (IOQD):** This bit reflects the value sampled on HA[7]# on the deassertion of the CPURST#. It indicates the depth of the host bus in-order queue (i.e. level of host bus pipelining). If IOQD is set to 1 (HA[7]# sampled 1 i.e. undriven on the host bus), then the depth of the host bus in-order queue is configured to the maximum allowed by the host bus protocol (i.e. 12). Note that the MCH has an 12 deep IOQ and will assert BNR# on the bus to limit the number of queued bus transactions to 12. If the IOQD bit is set to 0 (HA[7]# is sampled asserted , i.e., 0), then depth of the host bus in-order queue is set to 1 (i.e. no pipelining support on the host bus). Note that HA[7]# is not driven by the MCH during CPURST#. If an IOQ size of 1 is desired, HA[7]# must be driven low during CPURST# by an external source.
1:0	**Reserved**

3.7.42. ERRSTS – Error Status Register – Device #0

Address Offset: C8-C9h
Default Value: 0000h
Access: Read Only, Read/Write Clear
Size: 16 bits

This register is used to report various error conditions via the hub interface messages to ICH4-M. An SERR, SMI, or SCI error message may be generated via the hub interface A on a zero to one transition of any of these flags when enabled in the PCICMD/ERRCMD, SMICMD, or SCICMD registers respectively. These bits are set regardless of whether or not the SERR is enabled and generated.

Bit	Description
15	**DRAM Read Throttle Flag (DRTF) (R/WC):** Hardware sets this bit to report that a DRAM Read Throttling condition has occurred. On transitioning of this DRTF bit from a 0 to a 1 level, the MCH optionally generates a SERR hub interface special cycle, or a SMI hub interface special cycle, or a SCI hub interface special cycle when the corresponding bit 15 is enabled in the ERRCMD, or SMICMD, or SCICMD, respectively. Once this DRTF bit is set, although additional DRAM Read Throttling events may still occur in the MCH, further hub interface message generation is suppressed until this bit is cleared by software. Software clears this bit by writing a 1 to the bit. Once the bit is cleared, hardware will again set the bit on occurrence of the next DRAM Read Throttling event and optionally generate a corresponding hub interface special cycle.
14	**DRAM Write Throttle Flag (DWTF) (R/WC):** Hardware sets this bit to report that a DRAM Write Throttling condition has occurred. On transitioning of this DWTF bit from a 0 to a 1 level, the MCH optionally generates a SERR hub interface special cycle, or a SMI hub interface special cycle, or a SCI hub interface special cycle when the corresponding bit 14 is enabled in the ERRCMD, or SMICMD, or SCICMD, respectively. Once this DWTF bit is set, although additional DRAM Write Throttling events may still occur in the MCH, further hub interface message generation is suppressed until this bit is cleared by software. Software clears this bit by writing a 1 to the bit. Once the bit is cleared, hardware will again set the bit on occurrence of the next DRAM Write Throttling event and optionally generate a corresponding hub interface special cycle.
13:12	**Reserved**
11	**Catastrophic Thermal Sensor Event for SCI/SERR/SMI Enable (CTSEE):** When this bit is set it indicates that a selected MCH Catastrophic Thermal Sensor event occurred. This bit will be set when the thermal event has tripped and after tripping, on the transition below the trip point. Software must write a 1 to clear this status bit
10	**High/Low Thermal Sensor Event for SCI/SERR/SMI Enable (HTSSSE):** When this bit is set it indicates that a High/Low thermal trip (internal or external) event occurred. Software writes a 1 to clear this status bit. Software can distinguish internal or external Trip Event by examining TSSR (Thermal Sensor Status Reg) bit 3 External Trip Indicator (ETI).
9	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set it indicates that a host initiated LOCK cycle targeting non-DRAM memory space occurred. Software must write a 1 to clear this status bit.
8	**PSB Address Above TOM (FSBATOM):** When this bit is set the MCH has detected an address above 4GB or above Top of Memory. Software must write a 1 to clear this bit.
7	**Reserved**
6	**SERR on hub interface A Target Abort (TAHLA):** When this bit is set, the MCH has detected that an MCH originated hub interface A cycle was terminated with a Target Abort completion packet or special cycle. Software must write a 1 to clear this bit.
5	**MCH Detects Unimplemented hub interface Special Cycle (HIAUSC):** When this bit is set the MCH detected an Unimplemented Special Cycle on the hub interface. Software must write a 1 to clear this bit.

Bit	Description
4	**AGP Access Outside of Graphics Aperture Flag (OOGF):** When this bit is set it indicates that an AGP access occurred to an address that is outside of the graphics aperture range. Software must write a 1 to clear this status bit.
3	**Invalid AGP Access Flag (IAAF):** When this bit is set to 1 it indicates that an AGP access was attempted outside of the graphics aperture and either to the 640k-1M range or above top of the memory or illegal aperture access. Software must write a 1 to clear this status bit.
2	**Invalid Graphics Aperture Translation Table Entry (ITTEF):** When this bit is set to 1 it indicates that an invalid translation table entry was returned in response to an AGP access to the graphics aperture. Software must write a 1 to clear this bit.
1	**Multiple-bit DRAM ECC Error Flag (DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set the address and device number that caused the error are logged in the EAP register. Software uses bits [1:0] to detect whether the logged error address is for Single or Multiple-bit error. Once software completes the error processing, a value of 1 is written to this bit field to clear the value (back to 0) and unlock the error logging mechanism.
0	**Single-bit DRAM ECC Error Flag (DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. When this bit is set the address, channel number, and device number that caused the error are logged in the EAP register. Once this bit is set the EAP, CN, DN, and ES fields are locked to further single bit error updates until the processor clears this bit by writing a 1. Software must write a 1 to clear this bit and unlock the error logging mechanism.

3.7.43. ERRCMD – Error Command Register – Device #0

Address Offset: CA-CBh
Default Value: 0000h
Access: Read Only, Read/Write
Size: 16 bits

This register enables various errors to generate an SERR message via the hub interface A. Since the MCH does not have an SERR# signal, SERR messages are passed from the MCH to the ICH4-M over the hub interface. When a bit in this register is set, a SERR message will be generated on hub interface whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Note: An error can generate one and only one error message via the hub interface A. It is software's responsibility to make sure that when an SERR error message is enabled for an error condition, SMI and SCI error messages are disabled for that same error condition.

Bit	Description
15	**SERR on DRAM Read Throttle Condition:** Setting this bit to 1 enables the MCH to generate a SERR hub interface special cycle when bit 15 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Read Throttle event. Clearing this bit to 0 disables SERR hub interface special cycle on occurrence of DRAM Read Throttle.
14	**SERR on DRAM Write Throttle Condition:**Setting this bit to 1 enables the MCH to generate a SERR hub interface special cycle when bit 14 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Write Throttle event. Clearing this bit to 0 disables SERR hub interface special cycle on occurrence of DRAM Write Throttle.
13:12	**Reserved**
11	**SERR on Catastrophic Thermal Sensor Trip (CTSSERR):** When this bit is set to 1 the MCH generates an SERR hub interface special cycle when bit 11 of the ERRSTS is set. When this bit is 0 reporting of this condition via SERR messaging is disabled. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event.
10	**SERR on High/Low Thermal Sensor Trip (HLTSSERR):** When this bit is set to 1 the MCH generates an SERR hub interface special cycle when the bit 10 of the ERRSTS is set. When this bit is 0 reporting of this condition via SERR messaging is disabled. The SERR must not be enabled at the same time as the SMICMD.10 or SCICMD.10, for the High/Low thermal sensor (internal or external) event. Software can distinguish internal or external Trip Event by examining TSSR (Thermal Sensor Status Register) bit 3 External Trip Indicator (ETI).
9	**SERR on Non-DRAM Lock (LCKERR):** When this bit is asserted, the MCH will generate a hub interface A SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM.
8	**SERR on PSB Access Above TOM (HBATOMERR):** When this bit is asserted, the MCH will generate HI SERR special cycle when the CPU generates an access above 4 GB and above the Top of Memory.
7	**Reserved**
6	**SERR on Target Abort on hub interface A Exception (TAHLA_SERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when an MCH originated hub interface A cycle is completed with "Target Abort" completion packet or special cycle status.

Bit	Description
5	**SERR on Detecting Hub Interface A Unimplemented Special Cycle (HIAUSCERR):** When this bit is set to 1 the MCH generates an SERR message over hub interface A when an Unimplemented Special Cycle is received on the hub interface. When this bit is set to 0 the MCH does not generate an SERR message for this event. SERR messaging for Device 0 is globally enabled in the PCICMD register.
4	**SERR on AGP Access Outside of Graphics Aperture (OOGF_SERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when an AGP access occurs to an address outside of the graphics aperture.
3	**SERR on Invalid AGP Access (IAAF_SERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when an AGP access occurs to an address outside of the graphics aperture and either to the 640 k – 1 M range or above the top of memory.
2	**SERR on Invalid Translation Table Entry (ITTEF_SERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when an invalid translation table entry was returned in response to an AGP access to the graphics aperture.
1	**SERR Multiple-Bit DRAM ECC Error (DMERR_SERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when the MCH DRAM controller detects a multiple-bit error. For systems not supporting ECC this bit must be disabled.
0	**SERR on Single-bit ECC Error (DSERR):** When this bit is set, the generation of the hub interface A SERR message is enabled when the MCH DRAM controller detects a single bit error. For systems that do not support ECC this bit must be disabled.

3.7.44. SMICMD – SMI Command Register – Device #0

Address Offset: CC-CDh
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

This register enables various errors to generate a SMI message via the hub interface A.

Note: An error can generate one and only one error message via the hub interface A. It is software's responsibility to make sure that when an SMI error message is enabled for an error condition, SERR and SCI error messages are disabled for that same error condition.

Bit	Description
15	**SMI on DRAM Read Throttle Condition:** Setting this bit to 1 enables the MCH to generate an SMI hub interface special cycle when bit 15 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Read Throttle event. Clearing this bit to 0 disables SMI hub interface special cycle on occurrence of DRAM Read Throttle.
14	**SMI on DRAM Write Throttle Condition:** Setting this bit to 1 enables the MCH to generate an SMI hub interface special cycle when bit 14 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Write Throttle event. Clearing this bit to 0 disables SMI hub interface special cycle on occurrence of DRAM Write Throttle.
13:12	**Reserved**
11	**SMI on Catastrophic Thermal Sensor Trip (CTSSMI):** When this bit is set to 1, an SMI hub interface special cycle is generated by MCH when bit 11 of the ERRSTS register is set. This interrupt must not be enabled at the same time as the ERRCMD bit 11 is set.
10	**SMI on High/Low Thermal Sensor Trip (HLTSSMI):** When this bit is set to 1, the MCH generates an SMI hub interface special cycle when bit 10 of the ERRSTS register is set. When this bit is 0, reporting of this condition via SMI messaging is disabled. The SMI must not be enabled at the same time as the ERRCMD.10 or SCICMD.10, for the High/Low thermal sensor (internal or external) event. Software can distinguish internal or external Trip Event by examining TSSR (Thermal Sensor Status Register) bit 3 External Trip Indicator (ETI).
9:2	**Reserved**
1	**SMI on Multiple-bit DRAM ECC Error (DMERR):** When this bit is set, the generation of the hub interface A SMI message is enabled when the MCH DRAM controller detects a multiple-bit error. For systems not supporting ECC this bit must be disabled.
0	**SMI on Single-bit ECC Error (DSERR):** When this bit is set, the generation of the hub interface A SMI message is enabled when the MCH DRAM controller detects a single bit error. For systems that do not support ECC this bit must be disabled.

3.7.45. SCICMD – SCI Command Register – Device #0

Address Offset: CE-CDh
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

This register enables various errors to generate an SCI message via the hub interface A.

Note: An error can generate one and only one error message via the hub interface A. It is software's responsibility to make sure that when an SCI error message is enabled for an error condition, SERR and SMI error messages are disabled for that same error condition.

Bit	Description
15	**SCI on DRAM Read Throttle Condition:** Setting this bit to 1 enables the MCH to generate an SCI hub interface special cycle when bit 15 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Read Throttle event. Clearing this bit to 0 disables SCI hub interface special cycle on occurrence of DRAM Read Throttle.
14	**SCI on DRAM Write Throttle Condition:** Setting this bit to 1 enables the MCH to generate an SCI hub interface special cycle when bit 14 of the ERRSTS register transitions from 0 to 1 level, indicating occurrence of a DRAM Write Throttle event. Clearing this bit to 0 disables SCI hub interface special cycle on occurrence of DRAM Write Throttle.
13:12	**Reserved**
11	**SCI on Catastrophic Thermal Sensor Trip (CTSSCI):** When this bit is set to 1, an SCI hub interface special cycle is generated by MCH when bit 11 of the ERRSTS register is set.
10	**SCI on High/Low Thermal Sensor Trip (HLTSSCI):** When this bit is set to 1, the MCH generates an SCI hub interface special cycle when bit 10 of the ERRSTS register is set. When this bit is 0, reporting of this condition via SCI messaging is disabled. The SCI must not be enabled at the same time as the ERRCMD.10 or SMICMD.10, for the High/Low thermal sensor (internal or external) event. Software can distinguish internal or external Trip Event by examining TSSR (Thermal Sensor Status Register) bit 3 External Trip Indicator (ETI).
9:2	**Reserved**
1	**SCI on Multiple-Bit DRAM ECC Error (DMERR):** When this bit is set, the generation of the hub interface A SCI message is enabled when the MCH DRAM controller detects a multiple-bit error. For systems not supporting ECC this bit must be disabled.
0	**SCI on Single-bit ECC Error (DSERR):** When this bit is set, the generation of the hub interface A SCI message is enabled when the MCH DRAM controller detects a single bit error. For systems that do not support ECC this bit must be disabled.

3.7.46. WCCTL – Write Cache Control Register – Device #0

Address Offset: DCh
Default Value: 00h
Access: Read/Write
Size: 8 bits

Note: This register provides control of mode select of the Write-Cache flush scheme. It includes two masks of address bits that set based on the smallest SO-DIMM populated in the system.

Bit	Description
7:4	**Reserved**
3:2	**Spatial Flush Mask:** This two bit field allows row-miss or page-hit comparison to be performed on address bits A[12] and/or A[13], in addition to always using A[31:16]. When bit3 is set to 0, A[13] is included in the address compare operation. Otherwise it is masked – not included in the compare operation. When bit2 is set to 0, A[12] is included in the address compare operation. Otherwise it is masked – not included in the compare operation. **Bits 3:2 Smallest page size** 00 4 k or less 01 8 k 10 Reserved 11 16 k Note the “compare operation” has different meaning for row-miss and page-hit, so the mask bit has different meaning as well: In row-miss compare operation, a mask bit prevents the associated address bit from causing a row-miss condition TRUE. In page-hit compare operation, a mask bit prevents the associated address bit from causing a page-hit condition TRUE.
1:0	**Spatial Flush Mode:** This register is used to control the Write Cache flush mode used in the Intel® 855PM MCH. The write cache selects write entries to be flushed to DRAM based on two rules, temporal and spatial: Initial writes or when writes don’t meet spatial rules, are selected to be flushed based on LRU scheme. Otherwise writes to be flushed are selected based on spatial rules. The DDR controller supports two spatial rules: Page Hit: write cache will search for page hit cycles to be next flushed to DRAM. The selection of page hit is performed by comparing the previously flushed write address [33:14] to remaining “valid” writes in the write-cache, by searching for an address hit and by using two mask bit fields – one for A[12] and the other for A[13]. Row Miss: write cache will search for row miss cycles to be next selected in the flush stream. The selection of row miss is performed by comparing the previously flushed write address [33:14] to remaining “valid” writes in the write-cache, by searching for an address miss and by using two mask bit fields – one for A[12] and the other for A[13]. Note that spatial rules are set to optimize DRAM system with 128-Mb technology and 4Mx8b devices, or larger. The setting of this bit field: 00: Page Hit Spatial Flush Mode is enabled (combination of LRU and page hit scheme). 01: Row Miss Spatial Flush Mode is enabled (combination of LRU and row miss scheme). 10: Reserved 11: Spatial Flush Mode is disabled. Writes are flushed based on LRU scheme. 00 is the default mode of this register, to support LRU and page hit flush scheme.

3.7.47. SKPD – Scratchpad Data – Device #0

Address Offset: DE-DFh
Default Value: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:0	**Scratchpad [15:0]:** These bits are simply R/W storage bits that have no effect on the MCH functionality.

3.7.48. CAPID – Product Specific Capability register – Device #0

Address Offset: E4-E7h
Default Value: F104_A009h
Access: Read Only
Size: 32 bits

Bit	Descriptions
31	**Dual Data Rate System Memory Capability:** 1 = Component supports DDR SDRAM memory
30	**Mobile Power Management Capability:** 1 = Component is capable of all Mobile Power Management features 0 = Component is NOT capable of all Mobile Power Management features
29:28	**Reserved**
27:24	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	**CAPID Length:** This field has the value 04h to indicate the structure length (4 bytes).
15:8	**Next Capability Pointer:** This field has the value A0h to point to the next Capability ID in this device (ACAPID – AGP Capability ID register).
7:0	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

3.7.49. MCHTST – MCH Test Register – Device #0

Address Offset: F4-F7h
Default Value: 8020_F874h
Access: Read Only, Read/Write
Size: 32 bits

Bit	Description
31:23	**Reserved**
22	**System Memory MMR Enable:** When set, the SM Memory Mapped Register space and corresponding SMRBAR (Dev 0 Function 0 Offset 14h) is visible. When clear, the SMRBAR is hardwired to all zeros (effectively disabling this memory space).
21:2	**Reserved**
1	**Device #6 Enable (D6EN):** When this bit is 1, Device #6 configuration space is visible. Device #6 is a device that contains a few power management registers. When this bit is 0, Device #6 configuration space is hidden. When hidden, reads to the configuration registers return all 1's just as if the cycle terminated with a Master Abort on PCI.
0	**Reserved**

3.8. AGP Bridge Registers – Device #1

Table 26 shows the access attributes for configuration space for Device #1.

Table 26. Nomenclature for Access Attributes

RO	**Read Only:** If a register is read only, writes to this register have no effect.
R/W	**Read/Write:** A register with this attribute can be read and written.
R/WC	**Read/Write Clear:** A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.

Table 27 summarizes the MCH configuration space.

Table 27. MCH Configuration Space - Device #1

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID1	Vendor Identification	8086h	RO
02-03h	DID1	Device Identification	3341h	RO
04-05h	PCICMD1	PCI Command Register	0000h	RO, R/W
06-07h	PCISTS1	PCI Status Register	00A0h	RO, R/WC
08	RID1	Revision Identification	00h	RO
09		Reserved		
0Ah	SUBC1	Sub-Class Code	04h	RO
0Bh	BCC1	Base Class Code	06h	RO
0Ch		Reserved		
0Dh	MLT1	Master Latency Timer	00h	RO, R/W
0Eh	HDR1	Header Type	01h	RO
0F-17h		Reserved		
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	R/W
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	SMLT1	Secondary Bus Master Latency Timer	00h	RO, R/W
1Ch	IOBASE1	I/O Base Address Register	F0h	RO, R/W
1Dh	IOLIMIT1	I/O Limit Address Register	00h	RO, R/W
1E-1Fh	SSTS1	Secondary Status Register	02A0h	RO, R/WC
20-21h	MBASE1	Memory Base Address Register	FFF0h	RO, R/W
22-23h	MLIMIT1	Memory Limit Address Register	0000h	RO, R/W
24-25h	PMBASE1	Prefetchable Memory Base Address Reg.	FFF0h	RO, R/W
26-27h	PMLIMIT1	Prefetchable Memory Limit Address Reg.	0000h	RO, R/W
28-3Dh		Reserved		
3Eh	BCTRL1	Bridge Control Register	00h	RO, R/W
3Fh		Reserved		
40h	ERRCMD1	Error Command	00h	RO, R/W
41-4Fh		Reserved		
50-57h	DWTC	DRAM Write Throttle Control Register	0000000000000000h	RO, R/W, L
58-5Fh	DRTC	DRAM Read Throttle Control Register	0000000000000000h	RO, R/W, L
60h	TSCR	Thermal Sensor Control Register	00h	RO, R/W, L

Address Offset	Register Symbol	Register Name	Default Value	Access
61h	TSSR	Thermal Sensor Status Register	00h	RO
62-63h		Reserved		
64h	THTS	Thermal Sensor High Temp Set	00h	RO, R/W
65h	TCTS	Thermal Sensor Catastrophic Temp Set	00h	RO, R/W
66h	TCOR	Thermal Calibration Offset Reg	00h	RO, R/W, L
67h		Reserved		
68h	TSHTC	Thermal Sensor HW Throttle Control	00h	RO, R/W
69h		Reserved		
6A-FFh		Reserved		

3.8.1. VID1 – Vendor Identification Register – Device #1

Address Offset: 00 - 01h
Default Value: 8086h
Attribute: Read Only
Size: 16 bits

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.8.2. DID1 – Device Identification Register – Device #1

Address Offset: 02 - 03h
Default Value: 3341h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the MCH device #1. MCH device #1 DID =3341h

3.8.3. PCICMD1 – PCI-PCI Command Register – Device #1

Address Offset: 04-05h
Default: 0000h
Access: Read Only, Read/Write
Size 16 bits

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back (FB2B):** Not Applicable. Hardwired to 0.
8	**SERR Message Enable (SERRE1):** This bit is a global enable bit for Device #1 SERR messaging. The MCH does not have an SERR# signal. The MCH communicates the SERR# condition by sending an SERR message to the ICH4-M. If this bit is set to a 1, the MCH is enabled to generate SERR messages over the hub interface for specific Device #1 error conditions that are individually enabled in the BCTRL register. The error status is reported in the PCISTS1 register. If SERRE1 is reset to 0, then the SERR message is not generated by the MCH for Device #1. **NOTE:** This bit only controls SERR messaging for the Device #1. Device #0 has its own SERRE bit to control error reporting for error conditions occurring on Device #0.
7	**Address/Data Stepping (ADSTEP):** Not applicable. Hardwired to 0.
6	**Parity Error Enable (PERRE1):** Parity checking is not supported on the primary side of this device. Hardwired to 0
5	**Reserved**
4	**Memory Write and Invalidate Enable (MWIE):** This bit is implemented as Read Only and returns a value of 0 when read.
3	**Special Cycle Enable (SCE):** This bit is implemented as Read Only and returns a value of 0 when read.
2	**Bus Master Enable (BME1):** This bit is not functional. It is a RW bit for compatibility with compliance testing software.
1	**Memory Access Enable (MAE1):** This bit must be set to 1 to enable the Memory and Prefetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers. When set to 0 all of device #1's memory space is disabled.
0	**I/O Access Enable (IOAE1):** This bit must be set to1 to enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers. When set to 0 all of device #1's I/O space is disabled.

3.8.4. PCISTS1 – PCI-PCI Status Register – Device #1

Address Offset: 06-07h
Default Value: 00A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with primary side of the "virtual" PCI-PCI bridge embedded within the MCH. Since this device does not physically reside on PCI_A it reports the optimum operating conditions so that it does not restrict the capability of PCI_A.

Bit	Descriptions
15	**Detected Parity Error (DPE1):** Not Applicable - hardwired to 0.
14	**Signaled System Error (SSE1):** This bit is set to 1 when MCH Device #1 generates an SERR message over the hub interface A for any enabled Device #1 error condition. Device #1 error conditions are enabled in the ERRCMD, PCICMD1 and BCTRL1 registers. Device #1 error flags are read/reset from the ERRSTS and SSTS1 register. Software clears this bit by writing a 1 to it.
13	**Received Master Abort Status (RMAS1):** Not Applicable - hardwired to 0.
12	**Received Target Abort Status (RTAS1):** Not Applicable - hardwired to 0.
11	**Signaled Target Abort Status (STAS1):** Not Applicable - hardwired to 0.
10:9	**DEVSEL# Timing (DEVT1):** This bit field is hardwired to "00b" to indicate that the device #1 uses the fastest possible decode.
8	**Data Parity Detected (DPD1):** Not Applicable - hardwired to 0.
7	**Fast Back-to-Back (FB2B1):** This bit is hardwired to 1 to indicate that the AGP port always supports fast back-to-back transactions.
6	**Reserved**
5	**66-MHz Capability (CAP66):** This bit is hardwired to 1 to indicate that the AGP port is 66-MHz capable.
4:0	**Reserved**

3.8.5. RID1 – Revision Identification Register – Device #1

Address Offset: 08h
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the revision number of the MCH device #1. These bits are read only and writes to this register have no effect. For the A-0 Stepping this value is 00h.

Bit	Description
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH device #1.

3.8.6. SUBC1- Sub-Class Code Register – Device #1

Address Offset: 0Ah
Default Value: 04h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the MCH device #1. This code is 04h indicating a PCI-PCI Bridge device. The register is read only.

Bit	Description
7:0	**Sub-Class Code (SUBC1):** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. The code is 04h indicating a Host Bridge.

3.8.7. BCC1 – Base Class Code Register – Device #1

Address Offset: 0Bh
Default Value: 06h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the MCH device #1. This code is 06h indicating a Bridge device. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the Base Class Code for the MCH device #1. This code has the value 06h, indicating a Bridge device.

3.8.8. MLT1 – Master Latency Timer Register – Device #1

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write
Size: 8 bits

This functionality is not applicable. It is described here since these bits should be implemented as a read/write to prevent standard PCI-PCI bridge configuration software from getting "confused."

Bit	Description
7:3	**Not applicable but support read/write operations.** (Reads return previously written data.)
2:0	**Reserved**

3.8.9. HDR1 – Header Type Register – Device #1

Address Offset: 0Eh
Default: 01h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	**This read only field always returns 01h when read.** Writes have no effect.

3.8.10. PBUSN1 – Primary Bus Number Register – Device #1

Address Offset: 18h
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies that "virtual" PCI-PCI Bridge is connected to bus #0.

Bit	Descriptions
7:0	**Bus Number:** Hardwired to 0.

3.8.11. SBUSN1 – Secondary Bus Number Register – Device #1

Address Offset: 19h
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" PCI-PCI bridge i.e. to AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number:** Programmable. Default = 00h.

3.8.12. SUBUSN1 – Subordinate Bus Number Register – Device #1

Address Offset: 1Ah
Default: 00h
Access: Read /Write
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below AGP. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to AGP.

Bit	Descriptions
7:0	**Bus Number:** Programmable. Default = 0.

3.8.13. SMLT1 – Secondary Master Latency Timer Register – Device #1

Address Offset: 1Bh
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

This register controls the bus tenure of the MCH on AGP. MLT is an 8-bit register that controls the amount of time the MCH as an AGP/PCI bus master, can burst data on the AGP Bus. The Count Value is an 8-bit quantity, however MLT[2:0] are reserved and assumed to be 0 when determining the Count Value. The MCH's MLT is used to guarantee to the AGP master a minimum amount of the system resources. When the MCH begins the first AGP FRAME# cycle after being granted the bus, the counter is loaded and enabled to count from the assertion of FRAME#. If the count expires while the MCH's grant is removed (due to AGP master request), then the MCH will lose the use of the bus, and the AGP master agent may be granted the bus. If MCH's bus grant is not removed, the MCH will continue to own the AGP bus regardless of the MLT expiration or idle condition.

Note: The MCH must always properly terminate an AGP transaction with FRAME# negation prior to the final data transfer.

The number of clocks programmed in the MLT represents the guaranteed time slice (measured in 66-MHz AGP clocks) allotted to the MCH, after which it must complete the current data transfer phase and then surrender the bus as soon as its bus grant is removed. For example, if the MLT is programmed to 18h, then the value is 24 AGP clocks. The default value of MLT is 00h and disables this function. When the MLT is disabled, the burst time for the MCH is unlimited (i.e. the MCH can burst forever).

Bit	Description
7:3	**Secondary MLT counter value:** Default=0 i.e. SMLT disabled
2:0	**Reserved**

3.8.14. IOBASE1 – I/O Base Address Register – Device #1

Address Offset: 1Ch
Default Value: F0h
Access: Read/Write, Read Only
Size: 8 bits

This register controls the hosts to AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-kB boundary.

Bit	Description
7:4	**I/O Address Base:** Corresponds to A[15:12] of the I/O address. Default=F0h
3:0	**Reserved**

3.8.15. IOLIMIT1 – I/O Limit Address Register – Device #1

Address Offset: 1Dh
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

This register controls the hosts to AGP I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-kB aligned address block.

Bit	Description
7:4	**I/O Address Limit:** Corresponds to A[15:12] of the I/O address. Default = 0
3:0	**Reserved** (Only 16-bit addressing supported.)

3.8.16. SSTS1 – Secondary PCI-PCI Status Register – Device #1

Address Offset: 1E-1Fh
Default Value: 02A0h
Access: Read Only, Read/Write Clear
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. AGP side) of the "virtual" PCI-PCI bridge embedded within MCH.

Bit	Descriptions
15	**Detected Parity Error (DPE1):** This bit is set to a 1 to indicate MCH's detection of a parity error in the address or data phase of AGP bus transactions. Software sets DPE1 to 0 by writing a 1 to this bit.
14	**Reserved**
13	**Received Master Abort Status (RMAS1):** When the MCH terminates a Host-to-AGP with an unexpected master abort, this bit is set to 1. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS1):** When an MCH-initiated transaction on AGP is terminated with a target abort, RTAS1 is set to 1. Software resets RTAS1 to 0 by writing a 1 to it.
11	**Signaled Target Abort Status (STAS1):** STAS1 is hardwired to a 0, since the MCH does not generate target abort on AGP.
10:9	**DEVSEL# Timing (DEVT1):** This 2-bit field indicates the timing of the DEVSEL# signal when the MCH responds as a target on AGP, and is hardwired to the value 01b (medium) to indicate the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Master Data Parity Error Detected (DPD1):** Hardwired to 0. MCH does not implement G_PERR# signal.
7	**Fast Back-to-Back (FB2B1):** This bit is hardwired to 1, since MCH as a target supports fast back-to-back transactions on AGP.
6	**Reserved**
5	**66 MHz Capable (CAP66):** This bit is hardwired to 1 to indicate that AGP bus is capable of 66-MHz operation.
4:0	**Reserved**

3.8.17. MBASE1 – Memory Base Address Register – Device #1

Address Offset: 20-21h
Default Value: FFF0h
Access: Read/Write, Read Only
Size: 16 bits

This register controls the host to AGP non-prefetchable memory accesses routing based on the following formula:

MEMORY_BASE1=< address =<MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Memory Address Base 1 (MEM_BASE1):** Corresponds to A[31:20] of the memory address.
3:0	**Reserved**

3.8.18. MLIMIT1 – Memory Limit Address Register – Device #1

Address Offset: 22-23h
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

This register controls the host to AGP non-prefetchable memory accesses routing based on the following formula:

MEMORY_BASE1=< address =<MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bit	Description
15:4	**Memory Address Limit 1(MEM_LIMIT1):** Corresponds to A[31:20] of the memory address. Default = 0
3:0	**Reserved**

Note: Memory range covered by MBASE1 and MLIMIT1 registers are used to map non-prefetchable AGP address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE 1 and PMLIMIT1 are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved host-AGP memory access performance.

3.8.19. PMBASE1 – Prefetchable Memory Base Address Register – Device #1

Address Offset: 24-25h
Default Value: FFF0h
Access: Read/Write, Read Only
Size: 16 bits

This register controls the host to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE1=< address =<PREFETCHABLE_MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Prefetchable Memory Address Base 1(PMEM_BASE1):** Corresponds to A[31:20] of the memory address.
3:0	**Reserved**

3.8.20. PMLIMIT1 – Prefetchable Memory Limit Address Register – Device #1

Address Offset: 26-27h
Default Value: 0000h
Access: Read/Write, Read Only
Size: 16 bits

This register controls the host to AGP prefetchable memory accesses routing based on the following formula:

PREFETCHABLE_MEMORY_BASE1=< address =<PREFETCHABLE_MEMORY_LIMIT1

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bit	Description
15:4	**Prefetchable Memory Address Limit 1(PMEM_LIMIT1):** Corresponds to A[31:20] of the memory address. Default=0
3:0	**Reserved**

Note: Prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

3.8.21. BCTRL1 – PCI-PCI Bridge Control Register – Device #1

Address Offset: 3Eh
Default: 00h
Access: Read Only, Read/Write
Size 8 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e. AGP) as well as some bits that affect the overall behavior of the "virtual" PCI-PCI bridge embedded within MCH, e.g. VGA compatible address ranges mapping.

Bit	Descriptions
7	**Fast Back to Back Enable (FB2BEN):** Normally this bit controls whether the bridge will generate Fast Back to Back cycles to different targets. However, since there is only one target allowed on the AGP interface, this bit is not of any use. This bit is hardwired to 0.
6	**Secondary Bus Reset (SRESET):** MCH does not support generation of reset via this bit on the AGP and therefore this bit is hardwired to 0. Note that the only way to perform a hard reset of the AGP is via the system reset either initiated by software or hardware via ICH4-M.
5	**Master Abort Mode (MAMODE):** This bit is hardwired to 0. This means when acting as a master on AGP the MCH will discard data on writes and return all 1s during reads when a Master Abort occurs.
4	**Reserved**
3	**VGA Enable (VGAEN1):** Controls the routing of host initiated transactions targeting VGA compatible I/O and memory address ranges. When this bit is set , the MCH will forward the following host accesses to the AGP: 1) memory accesses in the range 0A0000h to 0BFFFFh 2) I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases - A[15:10] are not decoded) When this bit is set, forwarding of these accesses issued by the host is independent of the I/O address and memory address ranges that are defined by the previously defined base and limit registers. Forwarding of these accesses is also independent of the settings of the bit 2 (ISA Enable) of this register if this bit is 1. If this bit is 0 (default) , then VGA compatible memory and I/O range accesses are not forwarded to AGP but rather they are mapped to primary PCI unless they are mapped to AGP via I/O and memory range registers defined above (IOBASE1, IOLIMIT1, MBASE1, MLIMIT1, PMBASE1, PMLIMIT1). Please refer to the System Address Map section of this document for further information.
2	**ISA Enable (ISAEN):** Modifies the response by the MCH to an I/O access issued by the host that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. When this bit is set to 1 MCH will not forward to AGP any I/O transactions addressing the last 768 bytes in each 1-kB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to AGP these cycles will be forwarded to PCI0 where they can be subtractively or positively claimed by the ISA bridge. If this bit is 0 (default) then all addresses defined by the IOBASE and IOLIMIT for host I/O transactions will be mapped to AGP.
1	**Reserved**

Bit	Descriptions
0	**Parity Error Response Enable (PEREN):** Controls MCH's response to data phase parity errors on AGP. G_PERR# is not implemented by the MCH. However, when this bit is set to 1, address and data parity errors detected on AGP are reported via hub interface SERR# messaging mechanism, if further enabled by SERRE1. If this bit is reset to 0, then address and data parity errors on AGP are not reported via the MCH hub interface SERR# messaging mechanism. Other types of error conditions can still be signaled via SERR# messaging independent of this bit's state.

The bit field definitions for VGAEN and MDAP are detailed in the following table:

VGAEN MDAP	Description
00	All References to MDA and VGA space are routed to HI
01	Illegal combination
10	All VGA references are routed to this bus. MDA references are routed to HI
11	All VGA references are routed to this bus. MDA references are routed to HI

3.8.22. ERRCMD1 – Error Command Register – Device #1

Address Offset: **40h**
Default Value: **00h**
Access: **Read/Write**
Size: **8 bits**

Bit	Description
7:1	**Reserved**
0	**SERR on Receiving Target Abort (SERTA):** When this bit is 1 the MCH generates an SERR message over hub interface A upon receiving a target abort on AGP. When this bit is set to 0, the MCH does not assert an SERR message upon receipt of a target abort on AGP. SERR messaging for Device 1 is globally enabled in the PCICMD1 register.

3.8.23. DWTC – DRAM Write Throttling Control Register – Device #1

Address Offset: 50-57h
Default Value: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64 bits

Bit	Description
63:52	**Reserved**
51:50	**Throttle Lock (TLOCK):** These bits secure the DRAM Thermal Management control registers. The bits default to 0. Once a 1 is written to either bit, the configuration register bits specified in DWTC and DRTC registers become read-only: 00 – **Not locked:** All bits in DWTC or DRTC are writeable. 01 – **Start Mode bits are not locked:** All bits in DWTC and DRTC except for SWT and SRT are locked and become Read Only. 10 – **All bits locked:** All of the bits in the DWTC or DRTC are locked and become Read Only. 11 – **Reserved**
49	**Reserved**
48:41	**Global DRAM Write Sampling Window (GDWSW):** This 8-bit value is multiplied by $4*10^5$ to define the length of time in host clocks over which the number of hexwords (32-Byte chunks) written is counted. If the number of hexwords written during this window exceeds the Global Write Hexword Threshold defined below, then the throttling mechanism will be invoked to limit DRAM writes to a lower bandwidth checked over smaller time windows.
40:28	**Global Write Hexword Threshold (GWHT):** The thirteen-bit value held in this field is multiplied by 2^{15} (32 k) to arrive at the number of hexwords that must be written within the Global DRAM Write Sampling Window in order to cause the throttling mechanism to be invoked.
27:22	**Write Throttle Time (WTT):** This value provides a multiplier between 0 and 63 which specifies how long throttling remains in effect as a number of Global DRAM Write Sampling Windows. For example, if GDWSW is programmed to 1000_0000b and WTT is set to 01_0000b, then throttling will be performed for $8192*10^5$ host clocks seconds once invoked ($128 * 4*10^5$ host clocks * 16).
21:15	**Write Throttle Monitoring Window (WTMW):** The value in this register is padded with 4 0's to specify a window of 0-2047 host clocks with 16-clock granularity. While the throttling mechanism is invoked, DRAM writes are monitored during this window. If the number of hexwords written during the window reaches the Write Throttle Hexword Maximum, then write requests are blocked for the remainder of the window.
14:3	**Write Throttle Hexword Maximum (WTHM):** The Write Throttle Hexword Maximum defines the maximum number of hexwords between 0-4095 which are permitted to be written to DRAM within one Write Throttle Monitoring Window.
2:1	**Write Throttle Mode (WTMode):** **Encoding** – **Description** 00 – Throttling via Counters and Hardware throttle_on signal mechanisms disabled.

Bit	Description	
	01	**Hardware throttle_on signal mechanism is enabled.** In this mode, as long as the throttle_on signal is asserted, write throttling is in effect based on the settings in WTMW and WTHM. When the throttle_on signal is de-asserted, write throttling stops and the counters associated with the WTMW and WTHM are reset. When the hardware throttle_on signal mechanism is not enabled, the throttle_on signal has no effect.
	10	**Counter mechanism controlled through GDWSW and GWHT is enabled**. When the threshold set in GDWSW and GWHT is reached, throttling start/stop cycles occur based on the settings in WTT, WTMW, and WTHM.
	11	**Reserved**
0	**START Write Throttle (SWT):** When this bit is set to 1 write throttling begins based on the settings in WTMW and WTHM, and remains to be in effect until this bit is reset to 0. When this bit is reset to 0, write throttling stops and the counters associated with WTMW and WTHM are reset. Software writes to this bit to start and stop write throttling.	

3.8.24. DRTC – DRAM Read Throttling Control Register – Device #1

Address Offset: 58-5Fh
Default Value: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64 bits

Bit	Description	
63:49	**Reserved**	
48:41	**Global DRAM Read Sampling Window (GDRSW):** This 8-bit value is multiplied by $4*10^5$ to define the length of time in host clocks over which the number of hexwords (32-Byte chunks) read from DRAM is counted. If the number of hexwords read during this window exceeds the Global Read Hexword Threshold defined below, then the throttling mechanism will be invoked to limit DRAM reads to a lower bandwidth checked over smaller time windows.	
40:28	**Read Throttle Time (RTT):** The thirteen-bit value held in this field is multiplied by 2^{15} (32K) to arrive at the number of hexwords that must be read within the Global DRAM Read Sampling Window in order to cause the throttling mechanism to be invoked.	
27:22	**Read Throttle Time (RTT):** This value provides a multiplier between 0 and 63, which specifies how long Counter based read throttling remains in effect as a number of Global DRAM Read Sampling Windows. For example, if GDRSW is programmed to 1000_0000b and RTT is set to 01_0000b, then read throttling will be performed for $8192*10^5$ host clocks seconds once invoked (128 * $4*10^5$ host clocks * 16).	
21:15	**Read Throttle Monitoring Window (RTMW):** The value in this register is padded with 4 0's to specify a window of 0-2047 host clocks with 16-clock granularity. While the throttling mechanism is invoked, DRAM reads are monitored during this window. If the number of hexwords read during the window reaches the Read Throttle Hexword Maximum, then read requests are blocked for the remainder of the window.	
14:3	**Read Throttle Hexword Maximum (RTHM):** The Read Throttle Hexword Maximum defines the maximum number of hexwords between 0-4095, which are permitted to be read from DRAM within one Read Throttle Monitoring Window.	
2:1	**Read Thermal Management Mode (RFTMMode)**	
	Encoding	**Description**
	00	Throttling via Counters and Hardware rd_throttle_on signal mechanisms are disabled
	01	Hardware rd_throttle_on signal mechanism is enabled. In this mode, as long as the rd_throttle_on signal is asserted (by external or internal thermal sensor), read throttling is in effect based on the settings in RTMW and RTHM. When the rd_throttle_on signal is de-asserted, read throttling stops and the counters associated with the RTMW and RTHM are reset. When the hardware rd_throttle_on signal mechanism is not enabled, the rd_throttle_on signal has no effect.
	10	Counter mechanism controlled through GDRSW and GRHT is enabled. When the threshold set in GDRSW and GRHT is reached, throttling start/stop cycles occur based on the settings in RTT, RTMW and RTHM.
	11	**Reserved**

Bit	Description
0	**START Read Throttle (SRT):** When this bit is set to 1 read throttling begins based on the settings in RTMW and RTHM and remains to be in effect until this bit is reset to ‘0.’ When this bit is reset to ‘0,’ read throttling stops and the counters associated with RTMW and RTHM are reset. Software writes to this bit to start and stop read throttling.

3.8.25. TSCR – Thermal Sensor Control Register – Device #1

Address Offset: 60h
Default Value: 00h
Access: Read/Write, Read Only
Size: 8 bits

This register controls the operation of the thermal sensor.

Bit	Description
7	**Thermal Sensor enable (TSE):** This bit enables power to the thermal sensor. 1=enabled. Lockable via TCOR. **NOTE:** that TSHTC hardware throttle controls and catastrophic shutdown should be enabled at least 5us after the thermal sensor is enabled via TSE. The throttle controls and catastrophic shutdown should be disabled before disabling the thermal sensor via TSE.
6	**Reserved**
5:4	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1.0 °C, 2.0 °C, or 3.0 °C is used for hysteresis for the trip points. 00 = digital hysteresis disabled 01 = enabled, offset is 1.0 °C 10 = enabled, offset is 2.0 °C 11 = enabled, offset is 3.0 °C BIOS recommendation is TBD
3:2	**Reserved**
1	**Thermal Sensor output select (TSOS):** This bit muxes between the two comparator outputs 0 = Catastrophic, 1 = Hot. Normally Catastrophic is used. Lockable via TCOR.
0	**Thermal Sensor In Use (TSIU):** Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software which reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it.

3.8.26. TSSR – Thermal Sensor Status Register – Device #1

Address Offset: 61h
Default Value: 00h
Access: Read Only
Size: 8 bits

This read only register provides trip point and other status of the thermal sensor.

Bit	Description
7	**Catastrophic Trip Indicator (CTI):** A 1 indicates that the temperature is above the catastrophic setting.
6	**High Trip Indicator (HTI):** A 1 indicates that the temperature is above the High setting.
5:4	**Reserved**
3	**External Trip Indicator (ETI):** A 1 indicates that an externally monitored temperature has exceeded the programmed setting of an external thermal sensor.
2:0	**Reserved**

3.8.27. THTS – Thermal Sensor High Temperature Setting Register – Device #1

Address Offset: 64h
Default Value: 00h
Access: Read/Write
Size: 8 bits

High trip point setting. This register sets the DAC input value for the High trip point.

Bit	Description
7:0	**High Trip point setting (HTPS):** Sets the DAC input value for the High trip point.

3.8.28. TCTS – Thermal Sensor Catastrophic Temperature Setting Register – Device #1

Address Offset: 65h
Default Value: 00h
Access: Read/Write
Size: 8 bits

Catastrophic trip point setting. This register sets the DAC input value for the catastrophic trip point.

Bit	Description
7:0	**Catastrophic Trip point setting (CTPS):** Sets the DAC input value for Catastrophic. Lockable via TCOR bit 7.

3.8.29. TCOR – Thermal Calibration Offset Register – Device #1

Address Offset: 66h
Default Value: 00h
Access: Read/Write (5:0), Read Only (6), Lock (7)
Size: 8 bits

This register contains the calibration offset input to DAC for the Catastrophic and High trip point values. This register is locked via the Catastrophic Lock bit (bit 7 this register). The initial value for this register is determined by one of two sets of fuses, each of which can be used to provide the proper calibration offset.

Bit	Description
7	**Lock bit for Catastrophic (LBC):**This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7,5:0 of this register and bits 7:0 of TCTS, bit 7 of TSCR.
6	**Calibrated (CAL):**This bit indicates that the Class calibration fuses have been programmed. This bit is Read-Only
5:0	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. This field is Read/Write and can be modified by Software unless it is locked by setting bit 7 of this register.

3.8.30. TSHTC – Thermal Sensor Hardware Throttling Control Register – Device #1

Address Offset: 68h
Default Value: 00h
Access: Read/Write, Lock
Size: 8 bits

The register also selects which thermal zones enable main memory thermal throttling.

Bit	Description
7	**Memory Throttling Selection Catastrophic (MTSC):** This bit determines if Catastrophic thermal trip will enable main memory throttling. The main memory throttling register in PCI config space device #0 is used to enable or disable main memory throttling as a whole. Throttling enabled by the thermal sensor will be the maximum amount provided by the hardware. Lockable by bit 1 of this register. 0 – Catastrophic thermal zone will not cause throttling. 1 – The Catastrophic thermal zone will enable main memory thermal throttling. Read throttle based on the Catastrophic thermal zone can still be disabled by HRTC, Hardware Read Throttle Control (TSHTC[3:2]). *MTSC should be enabled at least 5 µs after the thermal sensor is enabled in TSCR[7].*
6	**External Sensor Event Enable (ESEE):** This bit is a master enable for external thermal sensor based events. 1 - An asserted External Thermal Sensor Trip signal can also cause a SCI, SMI or SERR as well as the Internal Sensor. This setting also enables the input buffer for the external sensor input ETS#. 0 - Only Internal Thermal Sensor Trip can cause an event
5	**Memory Throttling Selection High (MTSH):** This bit determines if High thermal trip will enable main memory throttling. The main memory throttling register in PCI config space device #0 is used to enable or disable main memory throttling as a whole. Throttling enabled by the thermal sensor will be the maximum amount provided by the hardware. Lockable by bit 1 of this register. 0 - The High thermal zone will enable main memory thermal throttling. 1 – High thermal zone will not cause throttling. Read throttle based on the High thermal zone can still be disabled by HRTC, Hardware Read Throttle Control (TSHTC[3:2]). *MTSH should be enabled at least 5 µs after the thermal sensor is enabled in TSCR[7].*
4	**Halt on Catastrophic (HOC):** When this bit is set, all clocks are disabled when the catastrophic sensor trips. A system reset is required to bring the system out of a halt from the thermal sensor. Lockable by bit 1 of this register. *HOC should be enabled at least 5 µs after the thermal sensor is enabled in TSCR[7].*

Bit	Description
3:2	**Hardware Read Throttling Control (HRTC)**. This bit is a master enable for external and internal thermal sensor based hardware **read** throttling. It selects whether automatic Read Throttling is triggered by External, or Internal Thermal Events, or Both. Lockable by bit 1 of this register. Note that throttle based on internal thermal events (read and write) is further controlled by MTSC and MTSH (TSHTC[7] and TSHTC[5]). Enabling internal throttling here will work only if MTSC or MTSH or both are also enabled. 00 - Read Throttle is not activated by External or Internal Thermal Trips (but Write Throttle may still be activated. 01 - Read Throttle via the External Thermal Sensor is Disabled, Internal Sensor is Enabled 10 - Read Throttle via the External Thermal Sensor is Enabled, Internal Sensor is Disabled 11 - Read Throttle activation by either the External or Internal Sensor Thermal Sensor is Enabled *MTSH should be enabled at least 5 µs after the thermal sensor is enabled in TSCR[7] (if using the internal thermal sensor).*
1	**Hardware Throttling Lock Bit (HTL).** This bit locks bits 7 and 5:1 of this register. When this bit is set to a one, the register bits are locked. It may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.
0	**Reserved**

3.9. Power Management Registers – Device #6

Note: For Device #6 configuration space to be visible, MCHTST Register in Device #0 space Bit 1 (D6EN bit) should be set.

Table 28. Nomenclature for Access Attributes

RO	**Read Only:** If a register is read only, writes to this register have no effect.
R/W	**Read/Write:** A register with this attribute can be read and written.
R/WC	**Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of a 1 clears (sets to 0) the corresponding bit and a write of a 0 has no effect.

Table 29 summarizes the MCH configuration space.

Table 29. MCH Configuration Space - Device #6

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID6	Vendor Identification	8086h	RO
02-03h	DID6	Device Identification	3342h	RO
04-05h	PCICMD6	PCI Command Register	0000h	RO
06-07h	PCISTS6	PCI Status Register	0080h	RO
08h	RID6	Revision Identification	00h	RO
09h		Reserved		
0Ah	SUBC6	Sub-Class Code	80h	RO
0Bh	BCC6	Base Class Code	08h	RO
0Ch- 0Dh		Reserved		
0Eh	HDR6	Header Type	00h	RO
10h- 13h	BAR6	Base Address Register	00000000h	RO
78h-7Ah	PMCR	Power Management Control Register	00C000h	RO, R/W, L
7B-91h		Reserved		
92h-93h	PMCER	Power Management Control ExtensionRegister	0002h	RO, R/W, L
94h-FFh		Reserved		

3.9.1. VID6 – Vendor Identification Register – Device #6

Address Offset: **00 - 01h**
Default Value: **8086h**
Attribute: **Read Only**
Size: **16 bits**

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number:** This is a 16-bit value assigned to Intel. Intel VID = 8086h.

3.9.2. DID6 – Device Identification Register – Device #6

Address Offset: 02 - 03h
Default Value: 3342h
Attribute: Read Only
Size: 16 bits

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number:** This is a 16-bit value assigned to the MCH device #6. MCH device #6 DID =3342h

3.9.3. PCICMD6 – PCI Command Register – Device #6

Address Offset: 04-05h
Default: 0000h
Access: Read Only
Size 16 bits

Bit	Descriptions
15:10	**Reserved**
9	**Fast Back-to-Back (FB2B):** This bit is hardwired to 0.
8	**SERR Message Enable (SERRE):** This bit is hardwired to 0.
7	**Address/Data Stepping (ADSTEP):** This bit is hardwired to 0.
6	**Parity Error Enable (PERRE):** This bit is hardwired to 0.
5	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0.
4	**Memory Write and Invalidate Enable (MWIE):** This bit is hardwired to 0.
3	**Special Cycle Enable (SCE):** This bit is hardwired to 0.
2	**Bus Master Enable (BME):** This bit is hardwired to 0.
1	**Memory Access Enable (MAE):** This bit is hardwired to 0.
0	**I/O Access Enable (IOAE):** This bit is hardwired to 0.

3.9.4. PCISTS6 – PCI Status Register – Device #6

Address Offset: 06-07h
Default Value: 0080h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of error events on Device #6, Function #0's PCI interface. Since MCH Device #6 does not physically reside on PCI_0 many of the bits are not implemented.

Bit	Descriptions
15	**Detected Parity Error (DPE1):** Not implemented.
14	**Signaled System Error (SSE1):** Not implemented.
13	**Received Master Abort Status (RMAS1):** Not implemented.
12	**Received Target Abort Status (RTAS1):** Not implemented.
11	**Signaled Target Abort Status (STAS1):** Not implemented.
10:9	**DEVSEL Timing (DEVT):** These bits are hardwired to 00. Writes to these bit positions have no effect.
8	**Data Parity Detected (DPD1):** Not implemented.
7	**Fast Back-to-Back (FB2B1):** This bit is hardwired to 1. Writes to these bit positions have no effect.
6:0	**Reserved**

3.9.5. RID6 – Revision Identification Register – Device #6

Address Offset: 08h
Default Value: 00h
Access: Read Only
Size: 8 bits

This register contains the revision number of the MCH device #6. These bits are read only and writes to this register have no effect. For the A-0 Stepping, this value is 00h.

Bit	Description
7:0	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH Device 6. For the A-0 Stepping, this value is 00h.

3.9.6. SUBC6- Sub-Class Code Register – Device #6

Address Offset: 0Ah
Default Value: 80h
Access: Read Only
Size: 8 bits

This register contains the Sub-Class Code for the MCH device #6.

Bit	Description
7:0	**Sub-Class Code (SUBC):** This is an 8-bit value that indicates the category of Device into which the Test Device falls. The code is 80h indicating other system peripherals.

3.9.7. BCC6 – Base Class Code Register – Device #6

Address Offset: 0Bh
Default Value: 08h
Access: Read Only
Size: 8 bits

This register contains the Base Class Code of the MCH device #6. This register is read only.

Bit	Description
7:0	**Base Class Code (BASEC):** This is an 8-bit value that indicates the category of Device into which the device falls. The code is 08h indicating other system peripherals.

3.9.8. HDR6 – Header Type Register – Device #6

Offset: 0Eh
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Descriptions
7:0	This read only field always returns 01h when read. Writes have no effect.

3.9.9. BAR6 – Base Address Register – Device #6

Address Offset: **10h**
Default Value: **0000_0000h**
Access: **Read Only**
Size: **32 bits**

Base address registers are not implemented on this device since it does not implement Memory or IO space.

Bit	Description
31:0	These bits are hardwired to 0, indicating that this device does not implement either Memory or IO space.

3.9.10. PMCR – Power Management Control Register – Device #6

Address Offset: 78-7A h
Default Value: 00C0_00h
Access: Read Only, Read/Write, Lock
Size: 24 bits

Bit	Description
23:16	**Reserved**
15	1: PSB bus drivers (0) have 25 Ohm “on” resistance (should be set when On Die Termination (ODT) disable is selected) 0: PSB bus drivers (0) have 12.5 Ohm “on” resistance
14	1: PSB bus termination resistors are disabled when Intel® 855PM MCH drives the PSB low. 0: PSB bus pull-ups are always enabled.
13	0: In C0 SM input sense amps and input buffers will be dynamically disabled when no data is pending 1: in C0, SM input sense amps and input buffers will be always enabled
12	0: In C3 and S1-M states, the System Memory DLLs will be disabled. 1: In C3 and S1-M states, the System Memory DLLs will remain enabled.
11:4	**Reserved**
3:2	These bits control the PSB input sense-amps in C0 and C2 states. The PSB input sense amps are always turned off C3/C4/S1-M/S3 states. The table shows the PSB input sense amp status for different programmed values. **NOTE:** For snoop cycles and CPU Writes, the DATA input buffers will be always be enabled as needed regardless of these bit settings. Bits / State / Data / Control 00 / C0 / ON / ON C2 / ON / ON 01 / C0 / Off / ON C2 / Off / ON 10 / C0 / ON / ON C2 / ON / Off 11 / C0 / Off / ON C2 / Off / Off
1	**Reserved**
0	Setting this bit locks the entire PMCR. Once locked, this register essentially becomes Read-Only, and any writes to this register are ignored.

3.9.11. PMCER – Power Management Control Extension Register – Device #6

Address Offset: 92-93h
Default Value: 0002h
Access: Read Only, Read/Write
Size: 16 bits

Bit	Description
15	**Power-management extension register lock (PMCERLK):** When written a 1, locks the whole register for read-only. The register is re-opened for write operations only after reset.
14:8	**Reserved**
7	**Freeze PLL in S1M**. 0 - Do not send FRZ_PLL signal to PLL entering S1M (Brookdale-compatible mode) 1 - Assert FRZ_PLL signal to PLL when entering S1M. Re-enable the buffers upon deassertion of DPSLP. If DPSLP is not wired to Intel® 855PM MCH in this system, then PMCER[7] must remain 0.
6	**Reserved**
5	**Early indication from Aunit Disable:** When this bit is set, early indications for data return to the CPU will be ignored, possibly creating a 2-clock latency.
4	**Reserved**
3:2	**PLL disable during C3/C4 control (Read – Write, Locked):** This bit controls the PLL disable capability during C3/C4. 00: Disable the internal PLLs (AGP and Host PLLs). On DPSLP# negation, exit to regular C3 10: Disable the internal PLLs (AGP and Host PLLs). On DPSLP# negation exit directly to C0 01: **Reserved** 11: Do not disable internal PLLs in C3/C4
1:0	**DPWR# assertion control (Read – Write, Locked):** 00: Do not assert DPWR# to the processor 01: **Reserved** 10: Assert DPWR# two host (BCLK) clocks before data is placed for the processor to read 11: **Reserved**

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4. System Address Map

A system based on the Intel® 855PM MCH supports 4 GB of addressable memory space and 64 kB+3 of addressable I/O space. The I/O and memory spaces are divided by system configuration software into regions. The memory ranges are useful either as system memory or as specialized memory, while the I/O regions are used solely to control the operation of devices in the system.

When the Intel® 855PM MCH receives a write request whose address targets an invalid space, the data is ignored. For reads, the MCH responds by returning all zeros on the requesting interface.

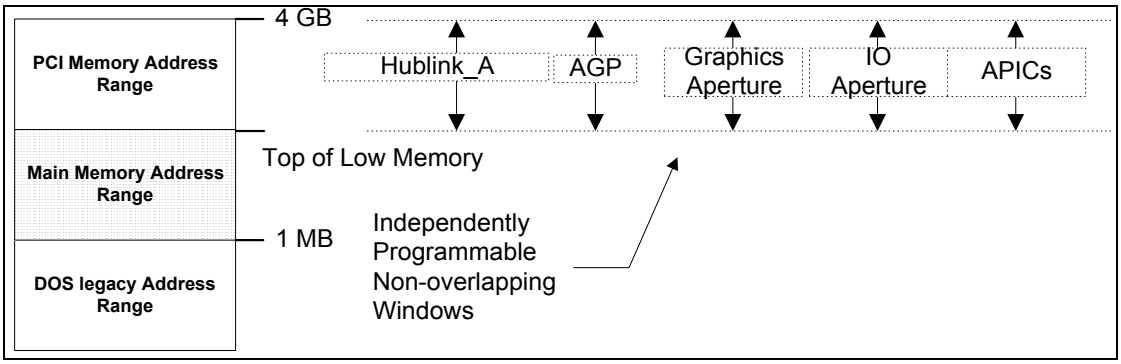
4.1. Memory Address Ranges

The system memory map is broken into two categories:

Extended Memory Range (1 MB to 4 GB) - The second is extended memory, existing between 1 MB and 4 GB. It contains a 32-bit memory space, which is used for mapping PCI, AGP, APIC, SMRAM, and BIOS memory spaces.

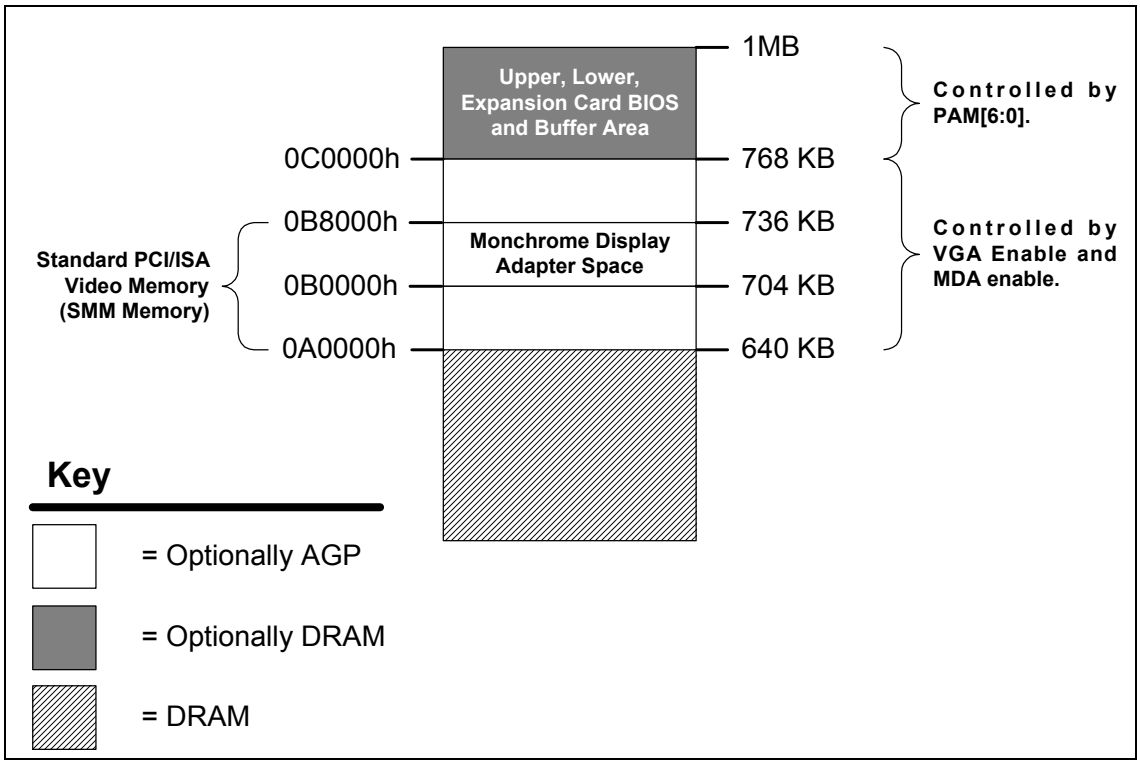
DOS Compatible Area (below 1 MB) - The final range is a DOS legacy space, which is used for BIOS and legacy devices on the LPC interface.

Figure 4. Addressable Memory Space



These address ranges are always mapped to system memory, regardless of the system configuration. Memory may be carved out of the MAINMEM segment for use by System Management Mode (SMM) hardware and software. The Top of Low Memory (TOM) register defines the top of Main Memory.

Figure 5. Detailed DOS Compatible Area Address Map



4.1.1. VGA and MDA Memory Space

VGAA	From	0_000A_0000	To	0_000A_FFFF
MDA		0_000B_0000		0_000B_7FFF
VGAB		0_000B_8000		0_000B_FFFF

Video cards use these legacy address ranges to map a frame buffer or a character-based video buffer. By default, accesses to these ranges are forwarded to hub interface. However, if the VGA_EN bit is set in the BCTRL1 configuration register, then transactions within the VGA and MDA spaces are sent to AGP.

If the configuration bit MCHCFG.MDAP is set, then accesses that fall within the MDA range will be sent to hub interface without regard for the VGAEN bits.

If the configuration bit MCHCFG.MDAP is set, then accesses that fall within the MDA range will be sent to hub interface without regard for the VGAEN bit. Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an Intel® 855PM MCH system, accesses in the standard VGA range are forwarded to AGP. Since the monochrome adapter may be on the hub interface or (or ISA) bus the MCH must decode cycles in the MDA range and forward them to hub interface. This capability is controlled by a configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh and forwards them to hub interface.

An optimization allows the system to reclaim the memory displaced by these regions. If SMM memory space is enabled by SMRAM.G_SMRARE and either the SMRAM.D_OPEN bit is set or the system bus

receives an SMM-encoded request for code (not data), then the transaction is steered to system memory rather than hub interface. Under these conditions, both the VGAEN bit and the MDAP bit are ignored.

4.1.2. PAM Memory Spaces

PAMC0	From	0_000C_0000	To	0_000C_3FFF
PAMC4		0_000C_4000		0_000C_7FFF
PAMC8		0_000C_8000		0_000C_BFFF
PAMCC		0_000C_C000		0_000C_FFFF
PAMD0		0_000D_0000		0_000D_3FFF
PAMD4		0_000D_4000		0_000D_7FFF
PAMD8		0_000D_8000		0_000D_BFFF
PAMDC		0_000D_C000		0_000D_FFFF
PAME0		0_000E_0000		0_000E_3FFF
PAME4		0_000E_4000		0_000E_7FFF
PAME8		0_000E_8000		0_000E_BFFF
PAMEC		0_000E_C000		0_000E_FFFF
PAMF0		0_000F_0000		0_000F_FFFF

The 256-kB PAM region is divided into three parts:

- **ISA expansion region**, a 128-kB area between 0_000C_0000h – 0_000D_FFFFh
- **Extended BIOS region**, a 64-kB area between 0_000E_0000h – 0_000E_FFFFh
- **System BIOS region**, a 64-kB area between 0_000F_0000h – 0_000F_FFFFh.

The ISA expansion region is divided into eight, 16-kB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through MCH and are subtractively decoded to ISA space.

The extended System BIOS region is divided into four, 16-kbytes segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to hub interface. Typically, this area is used for RAM or ROM.

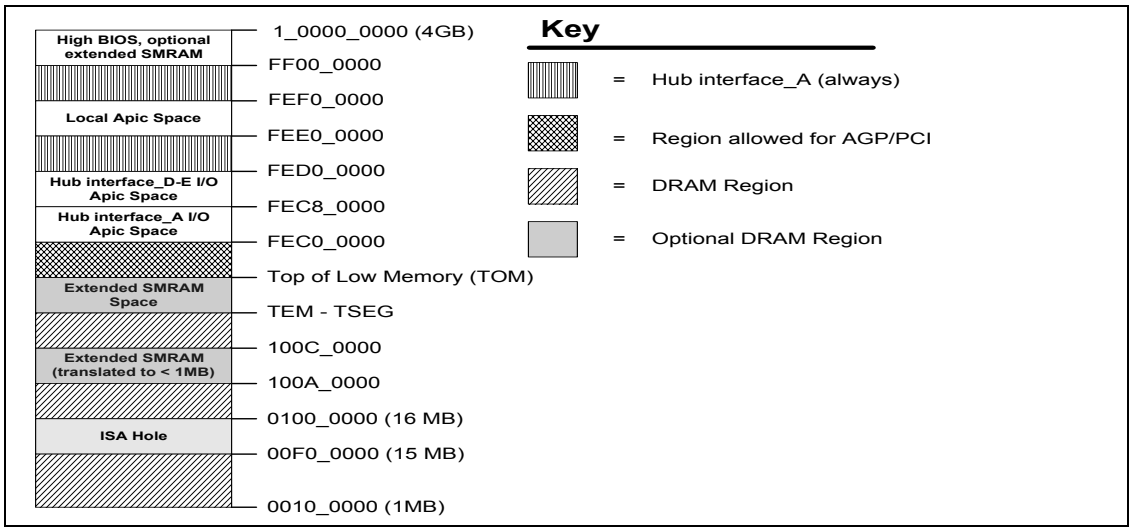
The system BIOS region is a single 64-kbyte segment. This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to hub interface. By manipulating the read/write attributes, the MCH can “shadow” BIOS into main DRAM.

4.1.3. ISA Hole Memory Space

ISA15	From	0_00F0_0000	To	0_00FF_FFFF

BIOS software may optionally open a “window” between 15 MB and 16 MB that relays transactions to hub interface instead of completing them with a system memory access. This window is opened with the FDHC.HEN configuration field.

Figure 6. Detailed Extended Memory Range Address Map



4.1.4. TSEG SMM Memory Space

TSEGSMM	From	TOM – TSEG	To	TOM

The TSEG SMM space allows system management software to partition a region of main memory just below the top of low memory (TOM) that is accessible only by system management software. This region may be 128 kB, 256 kB, 512 kB, or 1 MB in size, depending upon the ESMRAMC.TSEG_SZ field. SMM memory is globally enabled by SMRAM.G_SMRARE. Requests may access SMM system memory when either SMM space is open (SMRAM.D_OPEN) or the MCH receives an SMM code request on its system bus. In order to access the TSEG SMM space, the TSEG must be enabled by ESMRAMC.T_EN. When all of these conditions are met, then a system bus access to the TSEG space (between TOM-TSEG and TOM) is sent to system memory. If the high SMRAM is not enabled or if the TSEG is not enabled, then all memory requests from all interfaces are forwarded to system memory. If the TSEG SMM space is enabled, and an agent attempts a non-SMM access to TSEG space, then the transaction is specially terminated.

Hub interface and AGP originated accesses are not allowed to SMM space.

4.1.5. IOAPIC Memory Space

IOAPIC0 (hub interface)	From	0_FEC0_0000	To	0_FEC7_FFFF

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated on hub interface. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the IOAPIC0 region are always sent to hub interface.

4.1.6. System Bus Interrupt Memory Space

SBINTR	From	0_FEE0_0000	To	0_FEEF_FFFF

The System Bus interrupt space is the address used to deliver interrupts to the system bus. Any device on AGP or hub interface may issue a Memory Write to 0FEEx_xxxxh. The MCH will forward this Memory Write along with the data to the system bus as an Interrupt Message Transaction. The MCH terminates the system bus transaction by providing the response and asserting TRDY#. This Memory Write cycle does not go to DRAM.

4.1.7. High SMM Memory Space

HIGHSMM	From	0_FEDA_0000	To	0_FEDB_FFFF

The HIGHSMM space allows cacheable access to the compatible SMM space by re-mapping valid SMM accesses between 0_FEDA_0000 and 0_FEDB_FFFF to accesses between 0_000A_0000 and 0_000B_FFFF. The accesses are remapped when SMRAM space is enabled, an appropriate access is detected on the system bus, and when ESMRAMC.H_SMRAME allows access to high SMRAM space. SMM memory accesses from any hub interface or AGP are specially terminated: reads are provided with the value from address 0 while writes are ignored entirely.

4.1.8. AGP Aperture Space (Device #0 BAR)

AGPAPP	From	APBASE	To	APBASE + APSIZE

Processors and AGP devices communicate through a special buffer called the “graphics aperture”. This aperture acts as a window into main DRAM memory and is defined by the APBASE and APSIZE configuration registers of the Intel® 855PM MCH. Note that the AGP aperture must be above the top of memory and must not intersect with any other address space.

4.1.9. AGP Memory and Prefetchable Memory

M1	From	MBASE1	To	MLIMIT1
PM1		PMBASE1		PMLIMIT1

Plug-and-play software configures the AGP memory window in order to provide enough memory space for the devices behind this PCI-to-PCI bridge. Accesses whose addresses fall within this window are decoded and forwarded to AGP for completion. Note that these registers must be programmed with values that place the AGP memory space window between the value in the TOM register and 4 GB. In addition, neither region should overlap with any other fixed or relocatable area of memory.

4.1.10. Hub Interface A Subtractive Decode

HLA_SUB	From	TOM	To	4GB

All accesses that fall between the value programmed into the TOM register and 4 GB are subtractively decoded and forwarded to hub interface if they do not decode to a space that corresponds to another device.

4.2. AGP Memory Address Ranges

The MCH can be programmed to direct memory accesses to the AGP bus interface when addresses are within either of two ranges specified via registers in MCH Device #1 configuration space. The first range is controlled via the Memory Base Register (MBASE1) and Memory Limit Register (MLIMIT1) registers. The second range is controlled via the Prefetchable Memory Base (PMBASE1) and Prefetchable Memory Limit (PMLIMIT1) registers

The MCH positively decodes memory accesses to AGP memory address space as defined by the following equations:

- Memory_Base_Address <= Address =< Memory_Limit_Address
- Prefetchable_Memory_Base_Address =< Address <= Prefetchable_Memory_Limit_Address

The plug-and-play configuration software programs the effective size of the range, which depends on the amount of memory claimed by the AGP device.

Note: The MCH Device #1 memory range registers described above are used to allocate memory address space for any devices sitting on AGP bus that require such a window.

4.2.1. AGP DRAM Graphics Aperture

Memory-mapped, graphics data structures can reside in a Graphics Aperture to main DRAM memory. This aperture is an address range defined by the APBASE and APSIZE configuration registers of the MCH device #0. The APBASE register follows the standard base address register template as defined by the PCI 2.1 specification. The size of the range claimed by the APBASE is programmed via “back-end” register APSIZE (programmed by the chip-set specific BIOS before plug-and-play session is performed). APSIZE allows the BIOS software to pre-configure the aperture size to be 4 MB, 8 MB, 16 MB, 32 MB,

64 MB, 128 MB, or 256 MB. By programming APSIZE to a specific size, the corresponding lower bits of APBASE are forced to 0 (behave as hardwired). The default value of APSIZE forces an aperture size of 256 MB. The aperture address range is naturally aligned.

Accesses within the aperture range are forwarded to the main DRAM subsystem. The MCH will translate the originally issued addresses via a translation table maintained in main memory. The aperture range should be programmed as non-cacheable in the processor caches.

Note: Plug-and-play software configuration model does not allow overlap of different address ranges. Therefore, the AGP Graphics Aperture and AGP Memory Address Range are independent address ranges that may abut, but cannot overlap one another.

4.3. System Management Mode (SMM) Memory Range

The MCH supports the use of main memory as System Management RAM (SMRAM) enabling the use of System Management Mode. The MCH supports three SMRAM options: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM (SMRAM) space provides a memory area that is available for the SMI handler's and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. MCH provides three SMRAM options:

- Below 1 MByte option that supports compatible SMI handlers.
- Above 1 MByte option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional larger write-back cacheable T_SEG area from 128 kB to 1 MB in size above 1 MB that is reserved from the highest area in system DRAM memory. The above 1-MB solutions require changes to compatible SMRAM handlers' code to properly execute above 1 MB.

Note: Masters from the hub interface and AGP are not allowed to access the SMM space.

4.3.1. SMM Space Definition

Its addressed SMM space and its DRAM SMM space define SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Therefore the table below describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 30. SMM Space

SMM Space Enabled	Transaction Address Space (Adr)	DRAM Space (DRAM)
Compatible©	A0000h to BFFFFh	A0000h to BFFFFh
High (H)	0FEDA0000h to 0FEDBFFFFh	A0000h to BFFFFh
TSEG (T)	(TOM-TSEG_SZ) to TOM	(TOM-TSEG_SZ) to TOM

Note: High SMM: Note that this is different than in previous chip sets. In previous chip sets the High segment was the 384-kB region from A0000h to FFFFFh. However, C0000h to FFFFFh was not practically useful so it is deleted in MCH.

TSEG SMM: Note that this is different than in previous chip sets. In previous chip sets the TSEG address space was offset by 256 MB to allow for simpler decoding and the TSEG was remapped to just under the TOM. In the MCH 256 MB do not offset the TSEG region and it is not remapped.

4.3.2. SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang.

1. The Compatible SMM space must not be set-up as cacheable.
2. High or TSEG SMM transaction address space must not overlap address space assigned to system DRAM, the AGP aperture range, or to any “PCI” devices (including hub interface and AGP devices). This is a BIOS responsibility.
3. Both D_OPEN and D_CLOSE must not be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space must not be reported to the OS as available DRAM. This is a BIOS responsibility.
5. Any address translated through the AGP Aperture GTLB must not target DRAM from 000A0000h to 000FFFFFh.

4.4. I/O Address Space

The Intel® 855PM MCH does not support the existence of any other I/O devices beside itself on the system bus. The MCH generates either hub interface A or AGP bus cycles for all processor I/O accesses. The MCH contains two internal registers in the processor I/O space, Configuration Address register (CONFIG_ADDRESS) and the Configuration Data register (CONFIG_DATA). These locations are used to implement configuration space access mechanism and as described in the Configuration Register section.

The processor allows 64 k+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 byte locations. Note that the upper three locations can be accessed only during I/O address wrap-around when signal A16# address signal is asserted. A16# is asserted on the system bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the hub interface A unless they fall within the AGP I/O address range as defined by the mechanisms explained below. The MCH will not post I/O write cycles to IDE.

The MCH never responds to I/O or configuration cycles initiated on AGP or any of the hub interfaces. Hub interface transactions requiring completion are terminated with "master abort" completion packets on the hub interfaces. Hub interface write transactions not requiring completion are dropped. AGP/PCI I/O reads are never acknowledged by the MCH.

4.5. MCH Decode Rules and Cross-Bridge Address Mapping

The address map described above applies globally to accesses arriving on any of the three interfaces i.e. Host bus, the hub interface A or AGP.

4.5.1. Decode Rules for the Hub Interface A

The MCH accepts accesses from the hub interface A with the following address ranges:

- All memory read and write accesses to Main DRAM (except SMM space).
- All memory write accesses from the hub interface A to AGP memory range defined by MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1.
- All memory read/write accesses to the Graphics Aperture defined by APBASE and APSIZE.
- Memory writes to VGA range on AGP if enabled.

All memory reads from the hub interface A that are targeted > 4-GB memory range will be terminated with Master Abort completion, and all memory writes (>4 GB) from the hub interface A will be ignored.

4.5.2. AGP Interface Decode Rules

Cycles Initiated Using AGP FRAME# Protocol

The MCH does not support any AGP FRAME# access targeting the hub interface A. The MCH will claim AGP initiated memory read and write transactions decoded to the main DRAM range or the Graphics Aperture range. All other memory read and write requests will be master-aborted by the AGP initiator as a consequence of MCH not responding to a transaction.

Under certain conditions, the MCH restricts access to the DOS Compatibility ranges governed by the PAM registers by distinguishing access type and destination bus. The MCH does NOT accept AGP FRAME# write transactions to the compatibility ranges if the PAM designates DRAM as writable. If accesses to a range are not write enabled by the PAM, the MCH does not respond and the cycle will result in a master-abort. The MCH accepts AGP FRAME# read transactions to the compatibility ranges if the PAM designates DRAM as readable. If accesses to a range are not read enabled by the PAM, the MCH does not respond and the cycle will result in a master-abort.

If agent on AGP issues an I/O, PCI Configuration or PCI Special Cycle transaction, the MCH will not respond and cycle will result in a master-abort.

Cycles Initiated Using AGP PIPE# or SB Protocol

All cycles must reference main memory i.e. main DRAM address range (including PAM) or Graphics Aperture range (also physically mapped within DRAM but using different address range). AGP accesses to SMM space are not allowed. AGP initiated cycles that target DRAM are not snooped on the host bus, even if they fall outside of the AGP aperture range.

If a cycle is outside of main memory range then it will terminate as follows:

- Reads: remap to memory address oh, return data from address 0h, and set the IAAF error bit in ERRSTS register in device #0
- Writes: dropped “on the floor” i.e. terminated internally without affecting any buffers or main memory

AGP Accesses to MCH that Cross Device Boundaries

The MCH will disconnect AGP FRAME# transactions on 4-kB boundaries.

AGP PIPE# and SBA accesses are limited to 256 bytes and must hit DRAM. Read accesses crossing a device boundary will return invalid data when the access crosses out of DRAM. Write accesses crossing out of DRAM will be discarded and the IAAF Error bit will be set.

5. Functional Description

5.1. Host Interface Overview

The Intel® 855PM MCH Processor System Bus uses source synchronous transfer for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 100-MHz bus frequency, the address signals run at 200 MT/s for a maximum address queue rate of 50M addresses/sec. The data is quad pumped and an entire 64-B cache line can be transferred in two bus clocks. At 100-MHz bus frequency, the data signals run at 400 MT/s for a maximum bandwidth of 3.2 GB/s.

The Intel® 855PM MCH supports a 12 deep IOQ.

The Intel® 855PM MCH supports two outstanding deferred transactions on the system bus. The two transactions must target different IO interfaces as only one deferred transaction can be outstanding to any single IO interface at a time.

5.1.1. Dynamic Bus Inversion

The Intel® 855PM MCH supports Dynamic Bus Inversion (DBI) when driving and receiving data from the Host Bus. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the power consumption of the MCH. DINV[3:0]# indicates if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

Table 31. Relation of DBI Bits to Data Bits

DBI[3:0]#	Data Bits
DBI0#	HD[15:0]#
DBI1#	HD[31:16]#
DBI2#	HD[47:32]#
DBI3#	HD[63:48]#

Whenever the CPU or the MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus the corresponding DBI# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the MCH receives data it monitors DBI[3:0]# to determine if the corresponding data segment should be inverted.

5.1.2. System Bus Interrupt Delivery

Intel® Pentium® M processors support System Bus interrupt delivery. They do not support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the System Bus as “Interrupt Message Transactions”. In an Intel® 855PM chipset platform, System Bus interrupts may originate from the processor on the System Bus, or from a downstream device on hub interface, or AGP. In the later case the MCH drives the “Interrupt Message Transaction” onto the system bus.

In an Intel® 855PM chipset platform, the ICH4-M contains IOxAPICs and its interrupts are generated as upstream hub interface Memory Writes. Furthermore, PCI 2.2 defines MSI's (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI 2.2 device may generate an interrupt as an MSI cycle on its PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC, which in turn generates an interrupt as an upstream hub interface Memory Write. Alternatively the MSI may be directed directly to the System bus. The target of an MSI is dependent on the address of the interrupt Memory Write. The Intel® 855PM MCH forwards inbound hub interface and AGP (PCI semantic only) Memory Writes to address 0FEEx_xxxxh, to the System bus as "Interrupt Message Transactions."

5.1.3. Upstream Interrupt Messages

The MCH accepts message based interrupts from AGP (PCI semantics only) or its hub interface and forwards them to the system bus as Interrupt Message Transactions. The interrupt messages presented to the MCH are in the form of Memory Writes to address 0FEEx_xxxxh. At the hub interface or AGP interface the Memory Write interrupt message is treated like any other Memory Write; it is either posted into the inbound data buffer (if space is available) or retried (if data buffer space is not immediately available). Once posted, the Memory Write from AGP or the hub interface, to address 0FEEx_xxxxh, is decoded as a cycle that needs to be propagated by the MCH to the System bus as an Interrupt Message Transaction.

5.2. System Memory Interface

5.2.1. DDR Interface Overview

The Intel® 855PM MCH supports DDR at 200 MHz and 266 MHz only and includes support for:

- Up to 2.0 GB of PC1600/PC2100 DDR with stacked memory
- PC1600/2100 unbuffered 200 pin DDR SO-DIMMs
- Maximum of two SO-DIMMs, single-sided and/or double-sided
- Configurable optional ECC

The 2-bank select lines SBS[1:0] and the 13 Address lines SMA[12:0] allow the Intel® 855PM MCH to support 64-bit wide SO-DIMMs using 64-Mb, 128-Mb, 256-Mb, and 512-Mb DDR technology. While address lines SMA[9:0] determine the starting address for a burst, burst lengths can be 4 or 8. Four chip selects SCS# lines allow a maximum of two rows of single-sided DDR SO-DIMMs and four rows of double-sided DDR SO-DIMMs.

Intel® 855PM MCH main memory controller targets CAS latencies of 2 and 2.5 for DDR. Intel® 855PM MCH provides refresh functionality with a programmable rate (normal DDR rate is 1 refresh/15.6 µs).). For write operations of less than a full cache line, Intel® 855PM MCH will perform a cache-line read and into the write buffer and perform byte-wise write-merging in the write buffer.

5.2.2. Memory Organization and Configuration

Refer to Section 1.5.

5.2.2.1. Configuration Mechanism for SO-DIMMs

Detection of the type of DDR installed on the SO-DIMM is supported via Serial Presence Detect mechanism as defined in the JEDEC 200-pin SO-DIMM specification. This uses the SCL, SDA, and SA[2:0] pins on the SO-DIMMs to detect the type and size of the installed SO-DIMMs. No special programmable modes are provided on Intel® 855PM MCH for detecting the size and type of memory installed. Type and size detection must be done via the serial presence detection pins.

5.2.2.1.1. Memory Detection and Initialization

Before any cycles to the memory interface can be supported, the Intel® 855PM MCH DDR registers must be initialized. The Intel® 855PM MCH must be configured for operation with the installed memory types. Detection of memory type and size is done via the System Management bus (SMB) interface on the ICH4-M. This two-wire bus is used to extract the DDR type and size information from the Serial Presence Detect port on the DDR SO-DIMMs. DDR SO-DIMMs contain a 5-pin Serial Presence Detect interface, including SCL (serial clock), SDA (serial data) and SA[2:0]. Devices on the SMBus have a seven-bit address. For the DDR SO-DIMMs, the upper four bits are fixed at 1010. The lower three bits are strapped on the SA[2:0] pins. SCL and SDA are connected directly to the System Management bus on the ICH4-M. Thus data is read from the Serial Presence Detect port on the SO-DIMMs via a series of IO cycles to the south bridge. BIOS essentially needs to determine the size and type of memory used for each of the rows of memory in order to properly configure the Intel® 855PM MCH memory interface.

5.2.2.1.2. SMBus Configuration and Access of the Serial Presence Detect Ports

Refer to the *Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M) Datasheet* for more detail.

5.2.2.1.3. Memory Register Programming

This section provides an overview of how the required information for programming the DDR registers is obtained from the Serial Presence Detect ports on the SO-DIMMs. The Serial Presence Detect ports are used to determine Refresh Rate, MA and MD Buffer Strength, Row Type (on a row by row basis), DDR Timings, Row Sizes, and Row Page Sizes. The following table lists a subset of the data available through the on board Serial Presence Detect ROM on each SO-DIMM.

Table 32. Data Bytes on SO-DIMM Used for Programming DRAM Registers

Byte	Function
2	Memory Type (DDR SDRAM)
3	# of Row Addresses, not counting Bank Addresses
4	# of Column Addresses
5	# of SO-DIMM banks
11	ECC, no ECC
12	Refresh Rate/Type
17	# Banks on each Device

The above table is only a subset of the defined SPD bytes on the SO-DIMMs. These bytes collectively provide enough data for programming the Intel® 855PM MCH SDRAM registers.

5.2.3. DRAM Performance Description

The overall memory performance is controlled by the DRAM timing register, pipelining depth used in Intel® 855PM MCH, memory speed grade and the type of SDRAM used in the system. Besides this, the exact performance in a system is also dependent on the total memory supported, external buffering and memory array layout. The most important contribution to overall performance by the System Memory controller is to minimize the latency required to initiate and complete requests to memory, and to support the highest possible bandwidth (full streaming, quick turn-arounds). One measure of performance is the total flight time to complete a cache line request. A true discussion of performance really involves the entire chipset, not just the System Memory controller.

5.2.3.1. Data Integrity (ECC)

The Intel® 855PM MCH supports single-bit Error Correcting Code (or Error Checking and Correcting) and multiple-bit EC (Error Checking) on the main memory interface. The Intel® 855PM MCH generates an 8-bit code word for each 64-bit Qword of memory. Intel® 855PM MCH performs two Qword writes at a time so two 8-bit codes are sent with each write. Since the code word covers a full Qword, writes of less than a Qword require a read-merge-write operation. Consider a Dword write to memory. In this case, when in ECC mode, the Intel® 855PM MCH will read the Qword where the addressed Dword will be written, merge in the new Dword, generate a code covering the new Qword and finally write the entire Qword and code back to memory. Any correctable (single-bit) errors detected during the initial Qword read are corrected before merging the new Dword. The Intel® 855PM MCH also supports another data integrity mode, EC (Error Checking) mode. In this mode, the Intel® 855PM MCH generates and stores a code for each Qword of memory. It then checks the code for reads from memory but does not correct any errors that are found.

5.3. AGP Interface Overview

The Intel® 855PM MCH supports 1.5-V AGP 1x/2x/4x devices. The AGP signal buffers are 1.5-V drive/receive (buffers are not 3.3-V tolerant). The MCH supports 2x/4x source synchronous clocking transfers for read and write data, and sideband addressing. The MCH also supports 2x and 4x clocking for Fast Writes initiated from the MCH (on behalf of the processor).

AGP PIPE# or SBA[7:0] transactions to DRAM do not get snooped and are, therefore, not coherent with the processor caches. AGP FRAME# transactions to DRAM are snooped. AGP PIPE# and SBA[7:0] accesses to and from the hub interface are not supported. AGP FRAME# access from an AGP master to the hub interface is also not supported. Only the AGP FRAME memory writes from the hub interface are supported.

5.3.1. AGP Target Operations

As an initiator, the MCH does not initiate cycles using AGP enhanced protocols. The MCH supports AGP cycles targeting interface to main memory only. The MCH supports interleaved AGP PIPE# and AGP FRAME#, or AGP SBA[7:0], and AGP FRAME# transactions.

Table 33. AGP Commands Supported by the MCH When Acting as an AGP Target

AGP Command	C/BE[3:0]# Encoding	MCH Host Bridge	
		Cycle Destination	Response as PCIx Target
Read	0000	Main Memory	Low Priority Read
	0000	The Hub interface	Complete locally with random data; does not go to the hub interface
Hi-Priority Read	0001	Main Memory	High Priority Read
	0000	The Hub interface	Complete locally with random data; does not go to the hub interface
Reserved	0010	N/A	No Response
Reserved	0011	N/A	No Response
Write	0100	Main Memory	Low Priority Write
	0100	The Hub interface	Cycle goes to DRAM with BE's inactive; does not go to the hub interface
Hi-Priority Write	0101	Main Memory	High Priority Write
	0101	The Hub interface	Cycle goes to DRAM with BE's inactive; does not go to the hub interface
Reserved	0110	N/A	No Response
Reserved	0111	N/A	No Response
Long Read	1000	Main Memory	Low Priority Read
		The Hub interface	Complete locally with random data; does not go to the hub interface
Hi-Priority Long Read	1001	Main Memory	High Priority Read
		The Hub interface	Complete locally with random data; does not go to the hub interface
Flush	1010	MCH	Complete with QW of Random Data
Reserved	1011	N/A	No Response
Fence	1100	MCH	No Response - Flag inserted in MCH request queue
Reserved	1101	N/A	No Response
Reserved	1110	N/A	No Response
Reserved	1111	N/A	No Response

NOTE: N/A refers to a function that is not applicable.

As a target of an AGP cycle, the MCH supports all the transactions targeted at main memory (summarized in the table above). The MCH supports both normal and high priority read and write

requests. The MCH does not support AGP cycles to the hub interface. PIPE# and SBA cycles are assumed not to require coherency management and all AGP initiator accesses to main memory using AGP PIPE# or SBA protocol are treated as non-snoopable cycles. These accesses are directed to the AGP aperture in main memory that is programmed as either uncacheable (UC) memory or write combining (WC) in the processor's MTRRs.

5.3.2. AGP Transaction Ordering

The MCH observes transaction ordering rules as defined by the *AGP Interface Specification Rev 2.0*.

5.3.3. AGP Signal Levels

The 4x data transfers use 1.5-V signaling levels as described in the *AGP Interface Specification Rev 2.0*. The MCH supports 1x/2x data transfers using 1.5-V signaling levels.

5.3.4. 4x AGP Protocol

In addition to the 1x and 2x AGP protocol, the MCH supports 4x AGP read and write data transfers and 4x sideband address generation. The 4x operation is compliant with *AGP Interface Specification Rev 2.0*.

The MCH indicates that it supports 4x data transfers through RATE[2] (bit 2) of the AGP Status Register. When DATA_RATE[2] of the AGP Command Register is set to 1 during system initialization, the MCH performs AGP read/write data transactions using 4x protocol. This bit is not dynamic. Once this bit is set during initialization, the data transfer rate will not change.

The 4x data rate transfer provides 1.06 GB/s transfer rates. The control signal protocol for the 4x data transfer protocol is identical to 1x/2x protocol. In 4x mode 16 bytes of data are transferred on every 66-MHz clock edge. The minimum throttleable block size remains four, 66-MHz clocks, which means 64 bytes of data are transferred per block. Three additional signal pins are required to implement the 4x data transfer protocol. These signal pins are complementary data transfer strobes for the AD bus (2) and the SBA bus (1).

5.3.5. Fast Writes

The MCH supports 2x and 4x Fast Writes from the MCH to the graphics controller on AGP. Fast Write operation is compliant with the AGP 2.0 specification.

The MCH will not generate Fast Back to Back (FB2B) cycles in 1x mode, but will generate FB2B cycles in 2x and 4x Fast Write modes.

To use the Fast Write protocol, the Fast Write Enable configuration bit, AGPCMD[FWEN] (bit 4 of the AGP Command Register), must be set to 1.

Memory writes originating from the host or from the hub interface use the Fast Write protocol when it is both capability enabled and enabled. The data rate used to perform the Fast Writes is dependent on the bits set in the AGP Command Register bits 2:0 (DATA_RATE). If bit 2 of the AGPCMD[DATA_RATE] field is 1, the data transfers occur using 4x strobing. If bit 1 of AGPCMD[DATA_RATE] field is 1, the data transfers occur using 2x strobing. If bit 0 of AGPCMD[DATA_RATE] field is 1, Fast Writes are disabled and data transfers occur using standard PCI protocol. Note that only one of the three DATA_RATE bits may be set by initialization software. This is summarized in Table 34.

Table 34. Fast Write Initialization

FWEN	DATA_RATE [2]	DATA_RATE [1]	DATA_RATE [0]	MCH =>AGP Master Write Protocol
0	X	x	x	1x
1	0	0	1	1x
1	0	1	0	2x Strobing
1	1	0	0	4x Strobing

5.3.6. AGP FRAME# Transactions on AGP

The MCH accepts and generates AGP FRAME# transactions on the AGP bus. The MCH guarantees that AGP FRAME# accesses to DRAM are kept coherent with the processor caches by generating snoops to the host bus. LOCK#, SERR#, and PERR# signals are not supported.

MCH Initiator and Target Operations

Table 35 summarizes MCH target operation for AGP FRAME# initiators. The cycles can be either destined to main memory or the hub interface.

Table 35. PCI Commands Supported by the MCH When Acting as a FRAME# Target

PCI Command	C/BE[3:0]# Encoding	MCH	
		Cycle Destination	Response as A FRAME# Target
Interrupt Acknowledge	0000	N/A	No Response
Special Cycle	0001	N/A	No Response
I/O Read	0010	N/A	No Response
I/O Write	0011	N/A	No Response
Reserved	0100	N/A	No Response
Reserved	0101	N/A	No Response
Memory Read	0110	Main Memory	Read
	0110	The Hub interface	No Response
Memory Write	0111	Main Memory	Posts Data
	0111	The Hub interface	No Response
Reserved	1000	N/A	No Response
Reserved	1001	N/A	No Response
Configuration Read	1010	N/A	No Response
Configuration Write	1011	N/A	No Response
Memory Read Multiple	1100	Main Memory	Read
	1100	The Hub interface	No Response
Dual Address Cycle	1101	N/A	No Response
Memory Read Line	1110	Main Memory	Read
	1110	The Hub interface	No Response
Memory Write and Invalidate	1111	Main Memory	Posts Data
	1111	The Hub interface	No Response

NOTE: N/A refers to a function that is not applicable.

As a target of an AGP FRAME# cycle, the MCH only supports the following transactions:

- *Memory Read.* Recommended for reads of 32 bytes or less.
- *Memory Read Line, and Memory Read Multiple*. These commands are supported identically by the MCH and allow the MCH to continuously supply data during MRL and MRM burst. Recommended for reads of more than 32 bytes. The MCH does not support reads of the hub interface bus from AGP.
- *Memory Write and Memory Write and Invalidate*. These commands are aliased and processed identically. The MCH does not support writes to the hub interface bus from AGP.
- *Other Commands*. Other commands such as I/O R/W and Configuration R/W are not supported by the MCH as a target and result in master abort.
- *Exclusive Access*. The MCH does not support PCI locked cycles as a target.

- *Fast Back-to-Back Transactions*. MCH as a target supports fast back-to-back cycles from an AGP FRAME# initiator.

As an initiator of AGP FRAME# cycle, the MCH only supports the following transactions:

- *Memory Read and Memory Read Line*. MCH supports reads from host to AGP. MCH does not support reads from the hub interface to AGP.
- *Memory Read Multiple*. This command is not supported by the MCH as an AGP FRAME# initiator.
- *Memory Write*. MCH initiates AGP FRAME# cycles on behalf of the host or the hub interface. MCH does not issue Memory Write and Invalidate as an initiator. MCH does not support write merging or write collapsing. MCH allows non-snoopable write transactions from the hub interface to the AGP bus.
- I/*O Read and Write*. I/O read and write from the host are sent to the AGP bus. I/O base and limit address range for AGP bus are programmed in AGP FRAME# configuration registers. All other accesses that do not correspond to this programmed address range are forwarded to the hub interface.
- *Exclusive Access*. MCH does not issue a locked cycle on the AGP bus on behalf of either the host or the hub interface. The hub interface and host locked transactions to AGP are initiated as unlocked transactions by the MCH on the AGP bus.
- *Configuration Read and Write*. Host Configuration cycles to AGP are forwarded as Type 1 Configuration Cycles.
- *Fast Back-to-Back Transactions*. MCH as an initiator does not perform fast back-to-back cycles.

MCH Retry/Disconnect Conditions

The MCH generates retry/disconnect according to the AGP Specification rules when being accessed as a target from the AGP FRAME# device.

Delayed Transaction

When an AGP FRAME#-to-DRAM read cycle is retried by the MCH, it is processed internally as a Delayed transaction.

The MCH supports the Delayed transaction mechanism on the AGP target interface for the transactions issued using AGP FRAME# protocol. This mechanism is compatible with the *PCI Local Bus Specification Rev. 2.2*. The process of latching all information required to complete the transaction, terminating with Retry, and completing the request without holding the master in wait-states is called a Delayed Transaction. The MCH latches the Address and Command when establishing a Delayed Transaction. The MCH generates a Delayed transaction on the AGP only for AGP FRAME# to DRAM read accesses. The MCH does not allow more than one Delayed transaction access from AGP at any time.

5.4. Power and Thermal Management

Intel® 855PM chipset platform is intended to be compliant with the following specifications:

- APM Rev 1.2
- ACPI Rev 1.0b, ACPI Rev 2.0
- PCI Power Management Rev 1.0
- PC'99, Rev 1.0, PC'99A, and PC'01, Rev 1.0

5.4.1. Various States

Table 36. Power Management State Combinations

Global (G) State	Sleep (S) State	CPU (C) State	CPU Clock	MCH Host Clock	System Memory	Processor State
G0	S0	C0	On	On	On	Full On
G0	S0	C1	On	On	On	Auto-Halt
G0	S0	C2	On	On	On	Stop Grant
G0	S0	C3	Off	On/Off	Self Refresh	Deep Sleep
G0	S0	C4	Off	On/Off	Self Refresh	Deeper Sleep
G1	S1-M	C3/C4	Off	Off	Self Refresh	Power on Suspend (POS)
G1	S3	Off	Off	Off	Self Refresh	Suspend to RAM (STR)
G1	S4	Off	Off	Off	Off	Suspend to Disk (STD)
G2	S5	Off	Off	Off	Off	Soft-Off
G3	N/A	Off	Off	Off	Off	Mech-Off

5.4.2. General Description of Supported CPU States

- **C0 (Full On):** This is the only state that runs software. All clocks are running, STPCLK# is deasserted, and the processor core is active. The processor can service snoops and maintain cache coherency in this state.
- **C1 (Auto Halt):** The first level of power reduction occurs when the processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and reduces the processor's power consumption. The processor can service snoops and maintain cache coherency in this state.
- **C2 (Stop Grant):** To enter this low power state, STPCLK# is asserted. The processor can still service snoops and maintain cache coherency in this state.
- **C3 (Sleep or Deep Sleep):** In these states the processor clock is stopped. The MCH assumes that no AGP, AGP/PCI, or Hub Interface cycles (except special cycles) will occur while the MCH is in this state. The processor cannot snoop its caches to maintain coherency while in the C3 state. The MCH will transition from the C0 state to the C3 state when software reads the Level 3 Register. This is an ACPI defined register but BIOS or APM (via BIOS) can use this facility when entering a low power state. The AGP and Host Clock PLL within Intel® 855PM MCH can be programmed to be shut off for increased power savings and Intel® 855PM MCH uses the DPSLP# signal input for this purpose.
- **C4 (Deeper Sleep):** The C4 state appears to Intel® 855PM MCH as identical to the C3 state, but in this state the processor core voltage is lowered. There are no internal events in the Intel® 855PM MCH for the C4 state that differ from the C3 state.

5.4.3. General Description of ACPI System States

- **S0 (Awake):** In this state all power planes are active.
- **S1-M (Powered on Suspend for Mobile Systems):** Power is maintained to the CPU and all system components, but most clocks are stopped by the clock synthesizer. The processor is recommended to be in C3 or Deeper Sleep State (C4) during S1-M State.
- **S2:** ACPI S2 state is not supported in the Intel® 855PM chipset platform.
- **S3 (Suspend to RAM):** The next level of power reduction occurs when the clock synthesizer and core well power planes for the processor and chipset are shut down, but the main memory power plane and the ICH4-M resume well remain active. This is the Suspend To RAM (STR) state. All clock outputs from the clock synthesizer are shut down during the S3 state.
- **S4 (Suspend to Disk) and S5 (Soft Off):** In these states the main memory power plane is shut down in addition to the clock synthesizer and core well power planes for the processor and chipset. The ICH4-M resume well is still powered.
- **G3 (Mechanical Off):** In this state only the RTC (Real Time Clock) well is powered. The system can only be reactivated via the power switch.

5.4.4. Power Transitions

Table 37. Intel® 855PM MCH Power Transitions

ACPI State/Feature	CO	C1	C2	C3/C4	S1-M
DDR	Active/Dynamic Power-Down	Active/Dynamic Power-Down	Active/Dynamic Power-Down	Self Refresh	Self Refresh
GTL Control Buffer Sense Amp Disable	No	No	Yes (enabled during transactions)	Yes	Yes
Hub Interface	Active	Active	Active	Low Power State	Low Power State
CPU PLL	Running	Running	Running	Off (Can be programmed to be left running)	Off
AGP/Hub Interface PLL	Running	Running	Running	Off (Can be programmed to be left running)	Off

5.4.5. Enhanced Intel SpeedStep® Technology

The Intel® 855PM MCH platform with Intel® Pentium® M processor provides support for Enhanced Intel SpeedStep® technology with the following features:

- Provides improved Performance on Demand with ultra fast transitions that minimize impact on performance of frequent transitions. Seamless transition and typically 10 µs of memory and CPU unavailability
- Enables more effective software control; OS manages Enhanced Intel SpeedStep® technology transitions through ACPI and BIOS; With Performance on Demand, OS can default to lower performance states to provide just enough performance and therefore save power
- Multiple operating points thus enabling fine-grained performance/thermal control and optimizing battery life
- Flexibility in setting the number of operating points
- Simplifies platform design due to software control
- Implementation in the Processor, independent of the chip set

Enhanced Intel® SpeedStep® technology enables multiple CPU/system operating points includeing the following:

Highest CPU Frequency Mode (HFM): This is the highest core frequesncy the CPU can operate at enabling maximum performance.

Lowest CPU Frequency Mode (LFM): This is the lowest frequency the CPU can operate at. Core voltage is also lowered at this frequency resulting in lower power and longer battery life.

5.5. Internal Thermal Sensor

This section describes the new on-die thermal sensor capability.

5.5.1. Overview

The thermal sensor uses one comparator that is time multiplexed to perform two functions.

The two functions are:

Catastrophic Trip Point: This trip point is set at the temperature at which the MCH should be shut down immediately without any software support. The settings for this are lockable.

High Temperature Trip Point: This trip point is programmed through the BIOS during initialization and has the ability to provide an interrupt to ACPI (or other software) when it is crossed in either direction. Upon the trip event, hardware throttling may be enabled when the temperature is exceeded and is not lockable. Software may optionally set this as an "Interrupt me when the temperature goes above this level" setting.

5.5.2. Trip Point Operation

There are two trip points: Catastrophic and High. The trip points have similar operation. The outputs of the flip-flops may be read by software via the Thermal Sensor Status register (TSSR) and may also generate interrupts and enable throttling (catastrophic and high).

The Catastrophic trip point may be programmed to generate an interrupt, enable throttling, or immediately shut down the system. The High trip point may be programmed to generate an interrupt or enable throttling. The current state of all trip points may be read by software. The Catastrophic and High trip points may be programmed to both generate interrupts and enable throttling if necessary.

5.5.3. Hardware Throttling

The Catastrophic and High trip points may be programmed to enable throttling without intervention by software.

System memory throttling may be enabled on Catastrophic, or on High or Catastrophic, or not at all. TSHTC register selects whether it is Catastrophic or both that enable throttling, and system memory throttling registers in Device #0 configuration space determine whether throttling is enabled at all.

5.5.4. Halt on Catastrophic

The Catastrophic trip point may also be programmed to halt the system immediately. This is done by shutting off the clocks after the PLLs.

5.5.5. Register Locking

TCOR contains a lock bit that locks the catastrophic programming interface, including TCOR, TCTS, and bits in TSCR that could disable the sensor or alter the trip point.

TSHTC has a lock bit for the hardware throttling settings. It locks itself and bits 7:4 of TSHTC register, which control hardware throttling.

5.5.6. Hysteresis Operation

The thermal sensor has hysteresis built in, which is performed in analog. Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point. This is the same concept used in thermostats to prevent heating/cooling systems from turning on and off rapidly.

5.6. External Thermal Sensor Input

5.6.1. Introduction

An External Thermal Sensor with a serial interface may be placed next to DDR SO-DIMM, or a remote Thermal Diode may be placed next to the SO-DIMM and connected to the external Thermal Sensor.

The sensor would be connected to the SMBus Interface to allow programming and setup by BIOS software over the serial interface. The External Sensor's output should include an Active-Low Open-Drain signal indicating an Over-Temp condition that remains asserted for as long as the Over-Temp Condition exists, and deassert when within normal operating range. This will be connected to the Intel® 855PM MCH input (ETS#) and will trigger a preset Read-Throttle on a level-sensitive basis.

Additional external Thermal Sensor's outputs can be wire-OR'd together allow signaling from multiple sensors located physically separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the over-temp through the serial interface. However, since the SO-DIMM's will be located on the same Memory Bus Data lines, any MCH-base Read Throttle will apply equally.

5.6.2. Usage

The External Thermal Sensor input is selected via software control to derive the read throttle on signal that will activate the Read Throttle Controls. Additionally software can select if the External Sensor Trip can also cause a Thermal Event, which may steered with the Internal Sensor Trip to generate the required software interrupt. The external pin ETS# can be configured to cause throttle and/or trigger events. It is controlled via the TSHTC register. A trip on the ETS# pin can be seen by SW in TSSR[3].

5.7. MCH Clocking

The Intel® 855PM MCH is supported by the CK408 compliant clock synthesizer. Please refer to the *Intel® Pentium® M Processor Datasheet* and *Intel® Pentium M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide* for details.

5.8. MCH System Reset and Power Sequencing

Please refer to the *Intel® Pentium® M Processor Datasheet* and *Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide* for details.

5.8.1. MCH Reset

A Full MCH Reset is expected to occur when the power switch is turned on or when exiting any power-managed state where the system power supplies are shut down. A full reset is defined as when RSTIN# is asserted. All internal state machines are reset and all registers assume their default values when this reset occurs.

5.8.2. MCH Power Sequence Recommendation

Please refer to the *Intel® Pentium® M Processor Datasheet* and *Mobile Intel® Pentium® M Processor and Intel® 855PM DDR 266/200 MHz Chipset Platform Design Guide* for details.

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6. Electrical Characteristics

This chapter includes the absolute maximum operating ratings, power characteristics, and DC characteristics for the Intel® 855PM MCH.

6.1. Absolute Maximum Ratings

Table 38 lists the Intel® 855PM MCH maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the AC and DC tables.

Warning: Stressing the device beyond the absolute maximum ratings may cause permanent damage. These are stress ratings only. Operating beyond the operating conditions is not recommended and extended exposure beyond operating conditions may affect reliability.

Table 38. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_{die}	Die Temperature under Bias (with heatsink)	0	98	°C	
T_{die}	Die Temperature under Bias (without heatsink)	0	104	°C	
$T_{storage}$	Storage Temperature	-55	150	°C	
VCC1_2	1.2-V Supply Voltage with respect to Vss	-0.3	1.65	V	
VCC1_5	1.5-V Supply Voltage with respect to Vss	-0.3	1.65	V	
VCC1_8	1.8-V Supply Voltage with respect to Vss	-0.3	2.5	V	1
VCCSM	2.5-V DDR Supply Voltage with respect to Vss	-0.3	3.25	V	
VCCP	AGTL+ buffer DC input voltage with respect to Vss	-0.3	1.65	V	
V_{IL}, V_{IH} (DDR)	Voltage on 2.5-V DDR tolerant input pins with respect to Vss	-0.3	3.25	V	

NOTE: VCCGA and VCCHA pins provide the supply voltage to the Intel® 855PM MCH PLL and are connected to the VCC1_8V rail.

6.2. Thermal Characteristics

The Intel® 855PM MCH is designed for operation at die temperatures between 0°C and 104°C. The thermal resistance of the package is given in Table 39.

Table 39. Intel® 855PM MCH Package Thermal Resistance

Parameter	Airflow Velocity in Meters/Second	
	0 m/s	1 m/s
Ψ_{jt} (°C/Watt)**	0.5	1.8
Θ_{ja} (°C/Watt)**	20.0	17.3

NOTE: ** Typical value measured in accordance with EIA/JESD 51-2 testing standard.

6.3. Power Characteristics

Table 40. Power Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
TDP	Thermal Design Power		1.8		W	1
I_{VCCP}	Intel® 855PM MCH VCCP Supply Current			2.4	A	2
$I_{VCC1\_2\_CORE}$	1.2-V Core Supply Current			1.52	A	2
$I_{VCC1\_5\_AGP}$	1.5-V AGP Supply Current			0.37	A	2
I_{VCC1_8}	1.8-V Hub Interface Supply Current			0.20	A	2
I_{VCCSM}	DDR System Memory Interface (2.5 V) Supply Current			1.9	A	2
I_{SUS_VCCSM}	DDR System Memory Interface (2.5 V) Standby Supply Current			25	mA	
I_{SMVREF}	DDR System Memory Interface Reference Voltage (1.25 V) Supply Current			0.05	mA	
I_{SUS_SMVREF}	DDR System Memory Interface Reference Voltage (1.25 V) Standby Supply Current			0.05	mA	
I_{TTRC}	DDR System Memory Interface Resister Compensation Voltage (1.25 V) Supply Current			80	mA	
I_{SUS_TTRC}	DDR System Memory Interface Resister Compensation Voltage (1.25 V) Standby Supply Current			0	mA	

Note: This spec is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic

workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the Icc (Max) spec.

Note: Pre-silicon specs have a +20% / -10% tolerance.

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7. Signal Groups

The signal description includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. The Intel® 855PM MCH integrates most AGTL+ termination resistors.

AGP AGP interface signals. These signals are compatible with AGP 2.0 1.5-V Signaling Environment DC and AC Specifications. The buffers are not 3.3-V tolerant.

HI CMOS Hub Interface 1.8-V CMOS buffers.

DDR SSTL_2 DDR System memory 2.5 V SSTL_2 buffers.

Table 41. Signal Groups

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	AGTL+ I/O	ADS#, BNR#, BR0#,DBSY#, DBI[3:0]#, DRDY#, HA[31:3]#, HADSTB[1:0]#, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HIT#, HITM#, HREQ[4:0]#	
(b)	AGTL+ Common Clock Output	BPRI#, CPURST#, DEFER#, HTRDY#, RS[2:0]#; DPWR#	
(c)	AGTL+ Common Clock Input	HLOCK#	
(d)	Host Reference Voltages	HVREF, HSWNG[1:0]	
AGP Interface Signal Groups			
(e)	AGP I/O	AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, G_FRAME#, G_IRDY#, G_TRDY#, G_STOP#, G_DEVSEL#, G_AD[31:0], G_CBE[3:0]#, G_PAR	
(f)	AGP Input	PIPE#, SBA[7:0], RBF#, WBF#, SBSTB, SBSTB#, G_REQ#	
(g)	AGP Output	ST[2:0], G_GNT#	
(h)	AGP Reference Voltage	AGPREF	
Hub Interface Signal Groups			
(i)	Hub Interface's CMOS I/O	HI_[10:0], HI_STB, HI_STB#	
(j)	Hub Interface Reference Voltage	HI_REF	

DDR Interface Signal Groups			
(k)	DDR CMOS I/O	SDQ[71:0], SDQS[8:0]	
(l)	DDR CMOS Output	SCS[3:0]#, SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#, SCKE[3:0], RCVENOUT#, SCK[5:0], SCK[5:0]#	
(m)	DDR CMOS Input	RCVENIN#	
(n)	DDR Reference Voltage	SMVREF	
Clocks, Reset, and Miscellaneous Signal Groups			
(o)	CMOS Input	TESTIN#, ETS#	
(p)	CMOS Input	RSTIN#(3.3V)	
(q)	CMOS Clock Input	BCLK, BCLK#	
(v)	CMOS Clock Input	66IN(3.3V)	
(w)	Asynchronous CMOS	DPSLP#	
I/O Buffer Supply Voltages			
(r)	AGTL+ Termination Voltage	VCCP(1.05V)	
(s_0)	1.2-V Core Voltage	VCC1_2	
(s_1)	1.5-V AGP Voltage	VCC1_5	
(t)	1.8-V Hub Interface Voltage; 1.8-V Intel® 855PM MCH PLL Voltage	VCC1_8 (Hub Interface); VCCGA, VCCHA (PLL)	
(u)	2.5-V DDR Supply Voltage	VCCSM	

8. DC Characteristics

Table 42. DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage							
VCCSM	(u)	DDR I/O Supply Voltage	2.375	2.5	2.625	V	
VCC1_8	(t)	1.8V I/O Supply Voltage	1.71	1.8	1.89	V	
VCC1_5	(s_1)	AGP Voltage	1.425	1.5	1.575	V	
VCC1_2	(s_0)	Core Voltage	1.14	1.2	1.26	V	
VCCP	(r)	Host AGTL+ Termination Voltage	1.0	1.05	1.1	V	
Reference Voltages							
HVREF	(d)	Host Address and Data Reference Voltage	2/3 x VCCP – 2%	2/3 x VCCP	2/3 x VCCP + 2%	V	
HSWNG	(d)	Host Compensation Reference Voltage	1/3 x VCCP – 2%	1/3 x VCCP	1/3 x VCCP + 2%	V	
HIREF	(j)	Hub Interface Reference Voltage	0.48 x VCC1_8	1/2 x VCC1_8	0.52 x VCC1_8	V	
SMVREF	(n)	DDR Reference Voltage	0.48 x VCCSM	1/2 x VCCSM	0.52 x VCCSM	V	
AGPREF	(h)	AGP Reference Voltage	0.48 x VCC1_5	1/2 x VCC1_5	0.52 x VCC1_5	V	
Host Interface							
V_{IL_H}	(a,c)	Host AGTL+ Input Low Voltage	-0.10	0	(2/3 x VCCP) – 0.1	V	
V_{IH_H}	(a,c)	Host AGTL+ Input High Voltage	(2/3 x VCCP) + 0.1	VCCP (1.05)	VCCP + 0.1	V	
V_{OL_H}	(a,b)	Host AGTL+ Output Low Voltage			(1/3 x VCCP) + 0.1	V	
V_{OH_H}	(a,b)	Host AGTL+ Output High Voltage	VCCP-0.1		VCCP	V	
I_{OL_H}	(a,b)	Host AGTL+ Output Low Current			$VCCP_{max}$ / $0.75Rtt_{min}$	mA	Rtt_{min}=45Ω
I_{LEAK_H}	(a,c)	Host AGTL+ Input Leakage Current			2	µA	V_{OL}<Vpad< VCCP
C_{PAD}	(a,c)	Host AGTL+ Input Capacitance	1.62		2.32	pF	
C_{PCKG}	(a,c)	Host AGTL+ Input	0.90		3.02	pF	1

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
		Capacitance (common clock)					
DDR Interface							
$V_{IL(DC)}$	(k,m)	DDR Input Low Voltage			SMVREF – 0.15	V	
$V_{IH(DC)}$	(k,m)	DDR Input High Voltage	SMVREF + 0.15			V	
$V_{IL(AC)}$	(k,m)	DDR Input Low Voltage			SMVREF – 0.31	V	
$V_{IH(AC)}$	(k,m)	DDR Input High Voltage	SMVREF + 0.31			V	
DDR Interface cont.							
V_{OL}	(k,l)	DDR Output Low Voltage			TBD	V	
V_{OH}	(k,l)	DDR Output High Voltage	TBD			V	
I_{OL}	(k,l)	DDR Output Low Current			TBD	mA	
I_{OH}	(k,l)	DDR Output High Current	TBD			mA	
I_{Leak}	(k,m)	Input Leakage Current			±10	µA	
C_{PAD}	(k, l)	DDR Input/Output Pin Capacitance	2.46		3.52	pF	
C_{PCKG}	(k, l)	DDR Input/Output Pin Capacitance	1.14		2.98	pF	1
C_{PAD}	(m)	DDR Input/Output Pin Capacitance	0.95		1.35	pF	
C_{PCKG}	(m)	DDR Input/Output Pin Capacitance	1.14		1.14	pF	1
1.5 V AGP Interface							
V_{IL_A}	(e,f)	AGP Input Low Voltage			0.4 x VCC1_5	V	
V_{IH_A}	(e,f)	AGP Input High Voltage	0.6 x VCC1_5			V	
V_{OL_A}	(e,g)	AGP Output Low Voltage			0.15 x VCC1_5	V	
V_{OH_A}	(e,g)	AGP Output High Voltage	0.85 x VCC1_5			V	
I_{OL_A}	(e,g)	AGP Output Low Current			1	mA	@V_{OL_A} max
I_{OH_A}	(e,g)	AGP Output High Current	-0.2			mA	@V_{OH_A} max
I_{LEAK_A}	(e,f)	AGP Input Leakage Current			±10	µA	0<Vin< VCC1_5

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
C_{PAD}	(e,f)	AGP Input Capacitance	2.76		3.94	pF	
C_{PCKG}	(e,f)	AGP Input Capacitance	1.01		3.14	pF	1
1.8 V Hub Interface							
V_{IL_HI}	(i)	Hub Interface Input Low Voltage			HIREF - 0.15	V	
V_{IH_HI}	(i)	Hub Interface Input High Voltage	HIREF + 0.15			V	
V_{OL_HI}	(i)	Hub Interface Output Low Voltage			0.1 x VCC1_8	V	I_{OL}= 1 mA
V_{OH_HI}	(i)	Hub Interface Output High Voltage	0.9 x VCC1_8			V	I_{OH} = 1 mA
I_{OL_HI}	(i)	Hub Interface Output Low Current			1	mA	@V_{OL_HI} max
I_{OH_HI}	(i)	Hub Interface Output High Current	-1			mA	@V_{OH_HI} max
I_{LEAK_HI}	(i)	Hub Interface Input Leakage Current			±10	µA	0<Vin< VCC1_8
C_{PAD}	(i)	Hub Interface Input Capacitance	4.48		6.40	pF	
C_{PCKG}	(i)	Hub Interface Input Capacitance	1.13		2.45	pF	
Miscellaneous Signals							
V_{IL}	(o)	Input Low Voltage			HIREF - 0.15	V	
V_{IH}	(o)	Input High Voltage	HIREF + 0.15			V	
V_{OL}	(o)	Output Low Voltage			0.1 x VCC1_8	V	I_{OL}= 1 mA
V_{OH}	(o)	Output High Voltage	0.9 x VCC1_8			V	I_{OH} = 1 mA
I_{OL}	(o)	Output Low Current			1	mA	@V_{OL_HI} max
I_{OH}	(o)	Output High Current	-1			mA	@V_{OH_HI} max
I_{LEAK}	(o)	Input Leakage Current			±10	µA	0<Vin< VCC1_8
C_{PAD}	(o)	Input Capacitance	4.48		6.40	pF	
C_{PCKG}	(o)	Input Capacitance	2.22		2.22	pF	1
V_{IL}	(p)	Input Low Voltage			0.8	V	
V_{IH}	(p)	Input High Voltage	2.0			V	
I_{LEAK}	(p)	Input Leakage Current			±100	µA	**0<Vin<VCC3_3**
C_{PAD}	(p)	Input Capacitance	1.04		1.48	pF	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
C_{PCKG}	(p)	Input Capacitance	1.97		1.97	Pf	1
V_{IL}	(q)	Input Low Voltage		0		V	
V_{IH}	(q)	Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS}	(q)	Crossing Voltage	0.25V	0.35V	0.55V	V	
C_{PAD}	(q)	Input Capacitance	1.12		1.60	pF	
C_{PCKG}	(q)	Input Capacitance	1.47		1.47	pF	1
V_{IL}	(v)	Input Low Voltage			0.8	V	
V_{IH}	(v)	Input High Voltage	2.0			V	
C_{PAD}	(v)	Input Capacitance	2.10		3.00	pF	
C_{PCKG}	(v)	Input Capacitance	0.55		0.55	pF	1

NOTE: C_{PCKG} is the trace capacitance in the Intel® 855PM MCH package.

9. Ballout and Package Information

9.1. Ballout Diagram (Top View)

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
AJ			VSS		VCC1_5		VCCP		VCCP		VCCP		VSS		VSS		VSS		VSS		VSS		VSS		VSS		VSS			AJ
AH		SBA0	SBA1		G_GNT#		VSS		VSS		VSS		HD61#		HD57#		HD49#		HD44#		DBI2#		HD24#		HD31#		HD29#	HD20#		AH
AG	VCC1_5	SBA2	SBA3	ST2	ST0	G_REQ#	VCCP	VSS	VCCP	VSS	VCCP	VSS	HD56#	HD55#	HD54#	HD52#	HD48#	HD45#	HD42#	HD43#	HD38#	HD27#	HD28#	HDSTBP1#	DBI1#	HD16#	HD22#	HD17#	VSS	AG
AF			SBSTB	SBSTB#	VSS	ST1	VCC1_5	PIPE#	VSS	VCCP	VSS	VCCP	VSS	HD59#	VSS	HD51#	VSS	HD47#	VSS	HD41#	VSS	HD30#	VSS	HDSTBN1#	VSS	HD14#	HD11#			AF
AE	VSS	SBA4	SBA5	VCC1_5	SBA7	SBA6	WBF#	RBF#	VCCP	VSS	VCCP	VSS	CPURST#	HD63#	HD60#	HD53#	HD46#	HD40#	HDSTBP2#	HD36#	HD34#	HD19#	HD18#	HD25#	HD10#	VSS	HD8#	HD15#	VSS	AE
AD			NC	NC	GRCOMP	G_AD31	VCC1_5	VSS	VCC1_5	VCCP	VSS	VCCP	HD62#	VSS	DBI3#	VSS	HSWNG1	VSS	HDSTBN2#	VSS	HD37#	VSS	HD23#	VSS	DBI0#	HDSTBN0#	HDSTBP0#			AD
AC	VCC1_5	AD_STB1#	AD_STB1	VSS	G_AD28	G_AD29	VSS	G_AD30	VSS	VSS	VCCP	VSS	HD58#	HDSTBP3#	HDSTBN3#	HD50#	HRCOMP1	HD33#	HD32#	HD35#	HD39#	HD26#	HD21#	HD12#	HD5#	VSS	HD13#	HRCOMP0	VSS	AC
AB			G_AD20	G_AD22	G_AD19	G_AD27	G_AD24	VSS	VCC1_5	VCCP	VSS	VCCP	VSS	HVREF	VSS	VCCP	VSS	HVREF	VSS	VCCP	VSS	VCCP	HD9#	VSS	HD1#	HD4#	HD3#			AB
AA	VSS	G_AD18	G_AD21	VCC1_5	G_AD26	G_AD25	G_CBE3#	VCC1_5	AGPREF												HVREF	VSS	HSWNG0	HD7#	HD2#	VSS	HD6#	HD0#	VSS	AA
Y			G_AD16	G_AD17	G_CBE2#	G_FRAME#	G_AD23	VSS														DPWR#	BPRI#	VSS	HIT#	DEFER#	HITM#			Y
W	VCC1_5	G_DEVSEL#	G_IRDY#	VSS	G_PAR	G_TRDY#	G_STOP#	VCC1_5														VSS	RS0#	RS2#	RS1#	VSS	HLOCK#	DRDY#	VSS	W
V			G_AD9	G_AD8	G_CBE0#	G_AD15	G_CBE1#	VSS														DPSLP#	BR0#	VSS	DBSY#	HTRDY#	BNR#			V
U	VSS	G_AD7	G_AD6	VCC1_5	G_AD14	G_AD13	G_AD11	VCC1_5					VSS	VCC	VSS	VCC	VSS					VSS	ADS#	HA3#	HREQ3#	VSS	HA6#	HREQ0#	VSS	U
T			G_AD5	G_AD4	G_AD2	G_AD12	G_AD10	VSS					VCCGA	VSS	VCC	VSS	VCCHA					VCCP	HREQ1#	VSS	HA4#	HREQ4#	HA9#			T
R	VCC1_5	G_AD1	G_AD0	VSS	G_AD3	AD_STB0	AD_STB0#	VCC1_5					VSS	VCC	VSS	VCC	VSS					VSS	HREQ2#	HA13#	HADSTB0#	VSS	HA7#	HA5#	VSS	R
P			HLRCOMP	HI_REF	HI_0	HI_1	HI_3	66IN					VCC	VSS	VCC	VSS	VCC					HVREF	HA8#	VSS	HA12#	HA10#	HA11#			P
N	VSS	HI_9	HI_2	VCC1_8	HI_STB	HI_STB#	VCC1_8	VSS					VSS	VCC	VSS	VCC	VSS					VSS	HADSTB1#	HA24#	HA15#	VSS	HA16#	HA14#	VSS	N
M			HI_8	HI_4	HI_5	HI_10	VSS	VCC1_8														VCCP	HVREF	VSS	HA20#	HA19#	HA18#			M
L	VCC1_8	HI_6	HI_7	VSS	VCC1_8	VSS	VCCSM	VSS														VSS	HA29#	HA25#	HA21#	VSS	HA28#	HA26#	VSS	L
K			VSS	VCCSM	SCK#0	VCCSM	SCK5	VCCSM														BLOK#	VCCSM	VSS	HA27#	HA30#	HA22#			K
J	VSS	SMRCOMP	RSTIN#	VSS	SCK0	SCK#3	SCK#5	VSS	SMVREF												SMVREF	BLOK	VSS	VCCSM	HA31#	VSS	HA17#	HA23#	VSS	J
H			RSVD	TESTIN#	SDQ4	VCCSM	SCKE2	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	VSS	VCCSM	RSVD	VSS	VCCSM	ETS#	RSVD			H
G	VCCSM	SDQ0	SDQ5	VSS	SCK3	SCK2	SCKE0	RSVD	SMA12	SMA7	SMA8	SMA4	SMA3	RSVD	RCVENIN#	RCVENOUT#	SBS1	SBS0	SWE#	RSVD	RSVD	SCAS#	SCK#4	SCK4	SCK1	SDQS3	RSVD	RSVD	VCCSM	G
F			SDQ1	SDQS0	SDQ6	VSS	SCKE3	VCCSM	SMA9	VSS	SMA6	VCCSM	SMA1	VCCSM	VSS	VCCSM	SMA10	VSS	SRAS#	VCCSM	SCS#2	VSS	SCS#1	VSS	SCK#1	SDQS8	SDQS9			F
E	VSS	SDQ3	SDQ8	VSS	SDQ15	SCK#2	SDQ17	SCKE1	SDQ19	SMA11	SDQ29	SMA5	SDQ31	SMA2	SDQS8	VSS	SDQ32	SMA0	SDQ44	SDQ40	SCS#0	SDQ43	SCS#3	SDQ52	VCCSM	SDQS5	SDQS7	SDQ62	VSS	E
D			SDQ13	SDQ14	VCCSM	SDQ16	VCCSM	SDQ22	VSS	SDQ25	VCCSM	SDQ27	VSS	SDQS5	VCCSM	SDQ71	VSS	SDQS4	VCCSM	SDQ39	VSS	SDQ42	VCCSM	SDQ49	VSS	SDQ50	SDQ57			D
C	VCCSM	SDQ2	SDQ9	SDQS1	SDQ11	SDQ20	SDQS2	SDQ18	SDQ24	SDQ28	SDQ26	SDQ30	SDQ69	SDQ64	SDQ70	SDQ67	SDQ37	SDQ33	SDQ38	SDQ35	SDQ41	SDQS6	SDQ47	SDQ48	SDQS6	SDQ54	SDQ56	SDQ61	VCCSM	C
B		SDQ7	SDQ12		SDQ10		SDQ21		SDQ23		SDQS3		SDQ68		SDQ66		SDQ36		SDQ34		SDQ45		SDQ46		SDQ53		SDQ51	SDQ60		B
A			VSS		VCCSM		VSS		VCCSM		VSS		VCCSM		VSS		VCCSM		VSS		VCCSM		VSS		VCCSM		VSS			A
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9.2. Ballout Table

Signal Name	Ball#
ADS#	U7
AD_STB0	R24
AD_STB1	AC27
AD_STB0#	R23
AD_STB1#	AC28
AGPREF	AA21
BNR#	V3
BPRI#	Y7
BR0#	V7
CPURST#	AE17
DBSY#	V5
DEFER#	Y4
DBI0#	AD5
DBI1#	AG5
DBI2#	AH9
DBI3#	AD15
DPSLP#	V8
DPWR#	Y8
DRDY#	W2
G_AD0	R27
G_AD1	R28
G_AD10	T23
G_AD11	U23
G_AD12	T24
G_AD13	U24
G_AD14	U25
G_AD15	V24
G_AD16	Y27
G_AD17	Y26
G_AD18	AA28
G_AD19	AB25
G_AD2	T25
G_AD20	AB27

Signal Name	Ball#
G_AD21	AA27
G_AD22	AB26
G_AD23	Y23
G_AD24	AB23
G_AD25	AA24
G_AD26	AA25
G_AD27	AB24
G_AD28	AC25
G_AD29	AC24
G_AD3	R25
G_AD30	AC22
G_AD31	AD24
G_AD4	T26
G_AD5	T27
G_AD6	U27
G_AD7	U28
G_AD8	V26
G_AD9	V27
G_CBE0#	V25
G_CBE1#	V23
G_CBE2#	Y25
G_CBE3#	AA23
66IN	P22
G_DEVSEL#	W28
G_FRAME#	Y24
G_GNT#	AH25
G_IRDY#	W27
G_PAR	W25
GRCOMP	AD25
G_REQ#	AG24
G_STOP#	W23
G_TRDY#	W24
HA10#	P4

Signal Name	Ball#
HA11#	P3
HA12#	P5
HA13#	R6
HA14#	N2
HA15#	N5
HA16#	N3
HA17#	J3
HA18#	M3
HA19#	M4
HA20#	M5
HA21#	L5
HA22#	K3
HA23#	J2
HA24#	N6
HA25#	L6
HA26#	L2
HA27#	K5
HA28#	L3
HA29#	L7
HA3#	U6
HA30#	K4
HA31#	J5
HA4#	T5
HA5#	R2
HA6#	U3
HA7#	R3
HA8#	P7
HA9#	T3
HADSTB0#	R5
HADSTB1#	N7
BCLK#	K8
BCLK	J8
HD0#	AA2

Signal Name	Ball#
HD1#	AB5
HD10#	AE5
HD11#	AF3
HD12#	AC6
HD13#	AC3
HD14#	AF4
HD15#	AE2
HD16#	AG4
HD17#	AG2
HD18#	AE7
HD19#	AE8
HD2#	AA5
HD20#	AH2
HD21#	AC7
HD22#	AG3
HD23#	AD7
HD24#	AH7
HD25#	AE6
HD26#	AC8
HD27#	AG8
HD28#	AG7
HD29#	AH3
HD3#	AB3
HD30#	AF8
HD31#	AH5
HD32#	AC11
HD33#	AC12
HD34#	AE9
HD35#	AC10
HD36#	AE10
HD37#	AD9
HD38#	AG9
HD39#	AC9
HD4#	AB4
HD40#	AE12
HD41#	AF10

Signal Name	Ball#
HD42#	AG11
HD43#	AG10
HD44#	AH11
HD45#	AG12
HD46#	AE13
HD47#	AF12
HD48#	AG13
HD49#	AH13
HD5#	AC5
HD50#	AC14
HD51#	AF14
HD52#	AG14
HD53#	AE14
HD54#	AG15
HD55#	AG16
HD56#	AG17
HD57#	AH15
HD58#	AC17
HD59#	AF16
HD6#	AA3
HD60#	AE15
HD61#	AH17
HD62#	AD17
HD63#	AE16
HD7#	AA6
HD8#	AE3
HD9#	AB7
HDSTBN0#	AD4
HDSTBN1#	AF6
HDSTBN2#	AD11
HDSTBN3#	AC15
HDSTBP0#	AD3
HDSTBP1#	AG6
HDSTBP2#	AE11
HDSTBP3#	AC16
HIT#	Y5

Signal Name	Ball#
HITM#	Y3
HI_0	P25
HI_1	P24
HI_2	N27
HI_3	P23
HI_4	M26
HI_5	M25
HI_6	L28
HI_7	L27
HLOCK#	W3
HI_10	M24
HI_STB	N25
HI_STB#	N24
HI_REF	P26
HI_8	M27
HI_9	N28
HLRCOMP	P27
HREQ0#	U2
HREQ1#	T7
HREQ2#	R7
HREQ3#	U5
HREQ4#	T4
HTRDY#	V4
HVREF	AB16
HVREF	AB12
HVREF	AA9
HVREF	M7
HVREF	P8
HRCOMP0	AC2
HSWNG0	AA7
HRCOMP1	AC13
HSWNG1	AD13
NC	AD27
NC	AD26
Rsvd	G16
Rsvd	G10

Signal Name	Ball#
Rsvd	G9
Rsvd	H7
ETS#	H4
Rsvd	H3
Rsvd	G3
Rsvd	G2
PIPE#	AF22
RBF#	AE22
RCVENIN#	G15
RCVENOUT#	G14
RS0#	W7
RS1#	W5
RS2#	W6
RSTIN#	J27
SBA0	AH28
SBA1	AH27
SBA2	AG28
SBA3	AG27
SBA4	AE28
SBA5	AE27
SBA6	AE24
SBA7	AE25
SBS0	G12
SBS1	G13
SBSTB	AF27
SBSTB#	AF26
SCAS#	G8
SCK0	J25
SCK1	G5
SCK2	G24
SCK3	G25
SCK4	G6
SCK5	K23
SCK#0	K25
SCK#1	F5
SCK#2	E24

Signal Name	Ball#
SCK#3	J24
SCK#4	G7
SCK#5	J23
SCKE0	G23
SCKE1	E22
SCKE2	H23
SCKE3	F23
SCS#0	E9
SCS#1	F7
SCS#2	F9
SCS#3	E7
SDQ0	G28
SDQ1	F27
SDQ10	B25
SDQ11	C25
SDQ12	B27
SDQ13	D27
SDQ14	D26
SDQ15	E25
SDQ16	D24
SDQ17	E23
SDQ18	C22
SDQ19	E21
SDQ2	C28
SDQ20	C24
SDQ21	B23
SDQ22	D22
SDQ23	B21
SDQ24	C21
SDQ25	D20
SDQ26	C19
SDQ27	D18
SDQ28	C20
SDQ29	E19
SDQ3	E28
SDQ30	C18

Signal Name	Ball#
SDQ31	E17
SDQ32	E13
SDQ33	C12
SDQ34	B11
SDQ35	C10
SDQ36	B13
SDQ37	C13
SDQ38	C11
SDQ39	D10
SDQ4	H25
SDQ40	E10
SDQ41	C9
SDQ42	D8
SDQ43	E8
SDQ44	E11
SDQ45	B9
SDQ46	B7
SDQ47	C7
SDQ48	C6
SDQ49	D6
SDQ5	G27
SDQ50	D4
SDQ51	B3
SDQ52	E6
SDQ53	B5
SDQ54	C4
SDQ55	E4
SDQ56	C3
SDQ57	D3
SDQ58	F4
SDQ59	F3
SDQ6	F25
SDQ60	B2
SDQ61	C2
SDQ62	E2
SDQ63	G4

Signal Name	Ball#
SDQ64	C16
SDQ65	D16
SDQ66	B15
SDQ67	C14
SDQ68	B17
SDQ69	C17
SDQ7	B28
SDQ70	C15
SDQ71	D14
SDQ8	E27
SDQ9	C27
SDQS0	F26
SDQS1	C26
SDQS2	C23
SDQS3	B19
SDQS4	D12
SDQS5	C8
SDQS6	C5
SDQS7	E3
SDQS8	E15
SMA0	E12
SMA1	F17
SMA10	F13
SMA11	E20
SMA12	G21
Rsvd	G22
SMA2	E16
SMA3	G17
SMA4	G18
SMA5	E18
SMA6	F19
SMA7	G20
SMA8	G19
SMA9	F21
SMRCOMP	J28
SMVREF	J21

Signal Name	Ball#
SMVREF	J9
SRAS#	F11
Rsvd	H27
ST0	AG25
ST1	AF24
ST2	AG26
SWE#	G11
TESTIN#	H26
VCC	P17
VCC	N16
VCC	P15
VCC	R16
VCC	T15
VCC	U16
VCC	N14
VCC	P13
VCC	R14
VCC	U14
VCC1_5	R29
VCC1_5	W29
VCC1_5	AC29
VCC1_5	AG29
VCC1_5	U26
VCC1_5	AA26
VCC1_5	AE26
VCC1_5	AJ25
VCC1_5	AD23
VCC1_5	AF23
VCC1_5	R22
VCC1_5	U22
VCC1_5	W22
VCC1_5	AA22
VCC1_5	AB21
VCC1_5	AD21
VCCGA	T17
VCCHA	T13

Signal Name	Ball#
VCC1_8	L29
VCC1_8	L25
VCC1_8	N26
VCC1_8	N23
VCC1_8	M22
VCCSM	C29
VCCSM	G29
VCCSM	A25
VCCSM	D25
VCCSM	K26
VCCSM	D23
VCCSM	H24
VCCSM	K24
VCCSM	L23
VCCSM	A21
VCCSM	F22
VCCSM	H22
VCCSM	K22
VCCSM	D19
VCCSM	H20
VCCSM	A17
VCCSM	F18
VCCSM	H18
VCCSM	D15
VCCSM	F16
VCCSM	H16
VCCSM	A13
VCCSM	F14
VCCSM	H14
VCCSM	D11
VCCSM	H12
VCCSM	A9
VCCSM	F10
VCCSM	H10
VCCSM	D7
VCCSM	H8

Signal Name	Ball#
VCCSM	K7
VCCSM	A5
VCCSM	E5
VCCSM	H5
VCCSM	J6
VCCSM	C1
VCCSM	G1
VSS	E29
VSS	J29
VSS	N29
VSS	U29
VSS	AA29
VSS	AE29
VSS	A27
VSS	K27
VSS	AJ27
VSS	E26
VSS	G26
VSS	J26
VSS	L26
VSS	R26
VSS	W26
VSS	AC26
VSS	AF25
VSS	A23
VSS	F24
VSS	L24
VSS	M23
VSS	AC23
VSS	AH23
VSS	D21
VSS	H21
VSS	J22
VSS	L22
VSS	N22
VSS	T22

Signal Name	Ball#
VSS	V22
VSS	Y22
VSS	AB22
VSS	AC21
VSS	AD22
VSS	AF21
VSS	AG22
VSS	AH21
VSS	A19
VSS	F20
VSS	H19
VSS	AB19
VSS	AC20
VSS	AD19
VSS	AE20
VSS	AF19
VSS	AG20
VSS	AH19
VSS	D17
VSS	H17
VSS	N17
VSS	R17
VSS	U17
VSS	AB17
VSS	AC18
VSS	AE18
VSS	AF17
VSS	AG18
VSS	AJ17
VSS	A15
VSS	F15
VSS	H15
VSS	N15
VSS	P16
VSS	R15
VSS	T16

Signal Name	Ball#
VSS	U15
VSS	AB15
VSS	AD16
VSS	AF15
VSS	AJ15
VSS	D13
VSS	E14
VSS	H13
VSS	N13
VSS	P14
VSS	R13
VSS	T14
VSS	U13
VSS	AB13
VSS	AD14
VSS	AF13
VSS	AJ13
VSS	A11
VSS	F12
VSS	H11
VSS	AB11
VSS	AD12
VSS	AF11
VSS	AJ11
VSS	D9
VSS	H9
VSS	AB9
VSS	AD10
VSS	AF9
VSS	AJ9
VSS	A7
VSS	F8
VSS	J7
VSS	L8
VSS	N8
VSS	R8

Signal Name	Ball#
VSS	U8
VSS	W8
VSS	AA8
VSS	AD8
VSS	AF7
VSS	AJ7
VSS	D5
VSS	F6
VSS	H6
VSS	K6
VSS	M6
VSS	P6
VSS	T6
VSS	V6
VSS	Y6
VSS	AB6
VSS	AD6
VSS	AF5
VSS	AJ5
VSS	A3
VSS	J4

Signal Name	Ball#
VSS	L4
VSS	N4
VSS	R4
VSS	U4
VSS	W4
VSS	AA4
VSS	AC4
VSS	AE4
VSS	AJ3
VSS	E1
VSS	J1
VSS	L1
VSS	N1
VSS	R1
VSS	U1
VSS	W1
VSS	AA1
VSS	AC1
VSS	AE1
VSS	AG1
VCCP	AG23

Signal Name	Ball#
VCCP	AJ23
VCCP	AE21
VCCP	AG21
VCCP	AJ21
VCCP	AB20
VCCP	AC19
VCCP	AD20
VCCP	AE19
VCCP	AF20
VCCP	AG19
VCCP	AJ19
VCCP	AB18
VCCP	AD18
VCCP	AF18
VCCP	AB14
VCCP	AB10
VCCP	M8
VCCP	T8
VCCP	AB8
WBF#	AE23

9.3. Package Mechanical Information

The following figures provide details on the package information and dimensions of the Intel® 855PM MCH. The Intel® 855PM MCH comes in a Micro-FCBGA package similar to the mobile processors. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keepout area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

Figure 9. MCH BGA Package Dimensions (Top View)

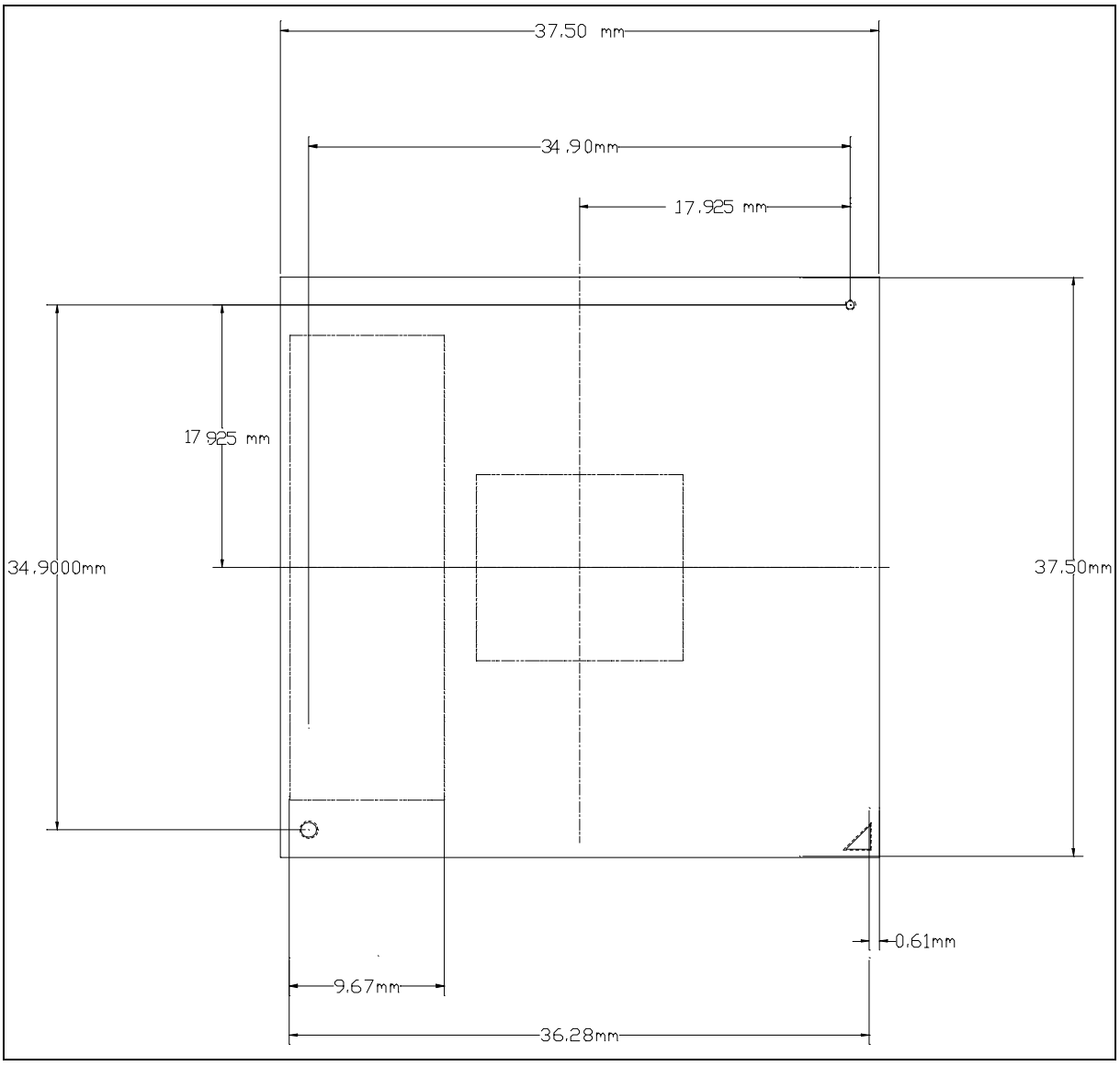


Figure 7. MCH Micro-FCBGA Package Dimensions (Side View)

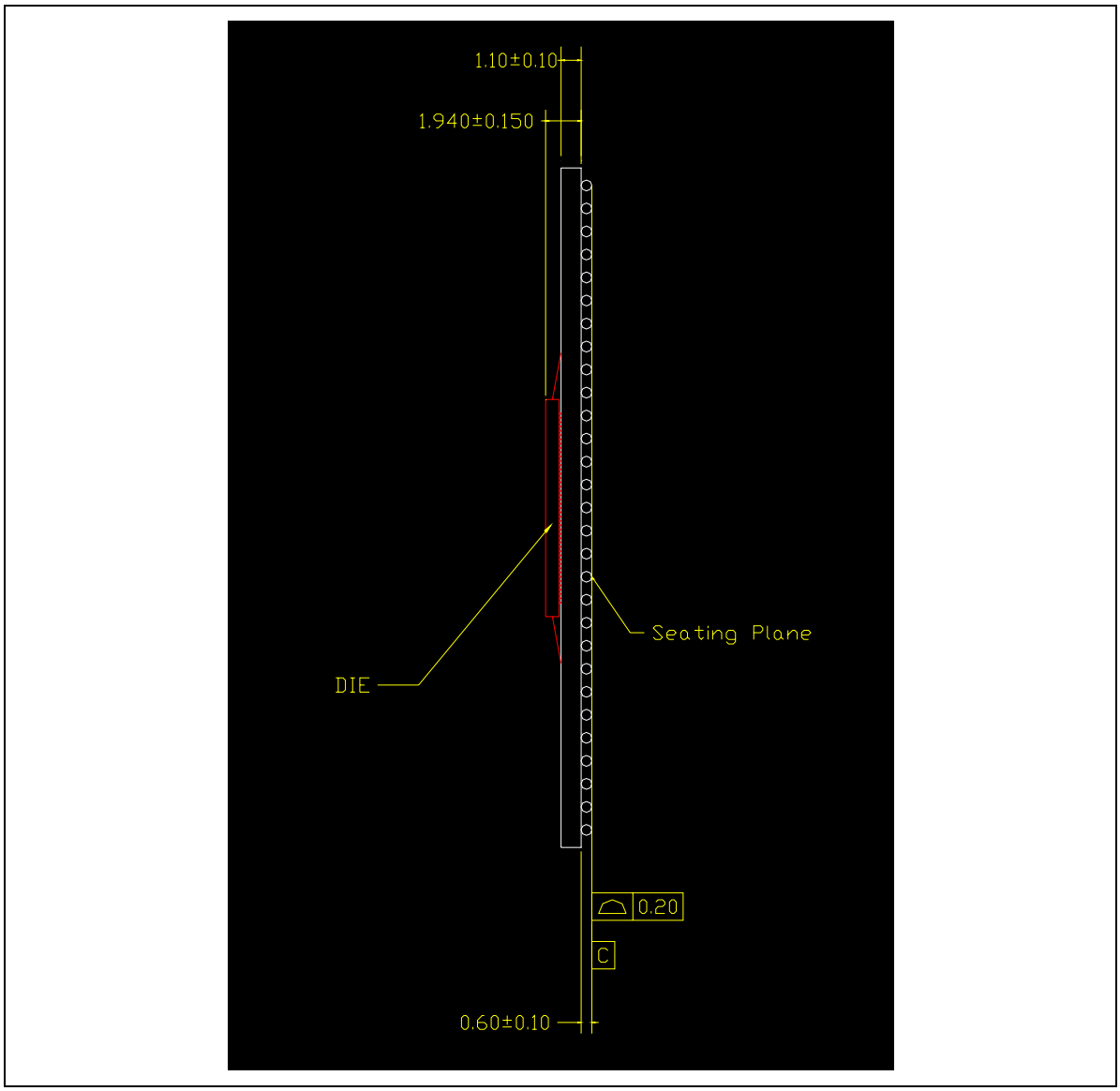
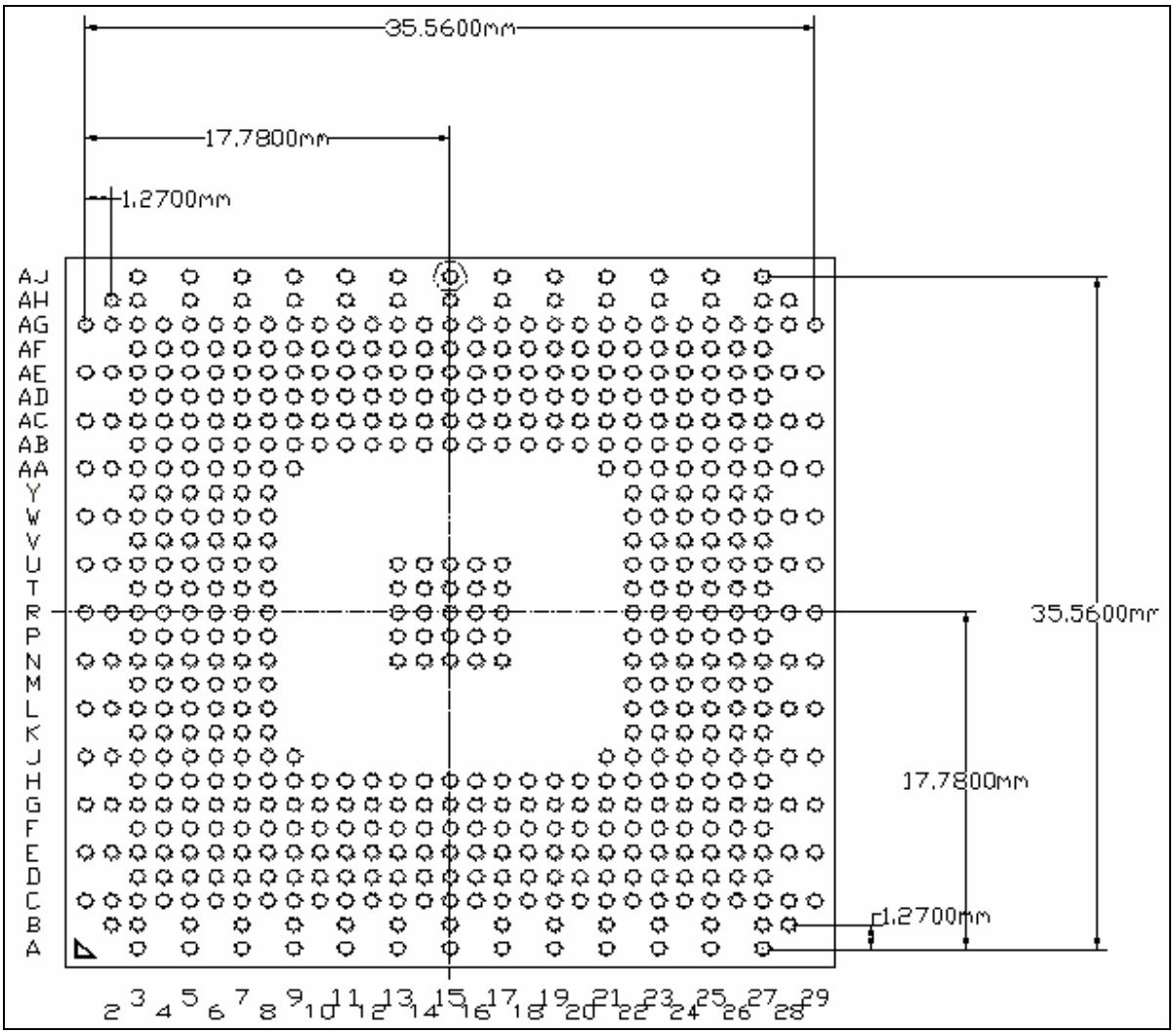


Figure 8. MCH Micro-FCBGA Package Dimensions (Bottom View)



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10. Testability

In the MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented through XOR chains and an All "Z" test mode.

The following table provides a summary on how to enter the different test modes using strapping options.

Table 43. Required Straps at Rising Edge of RSTIN#

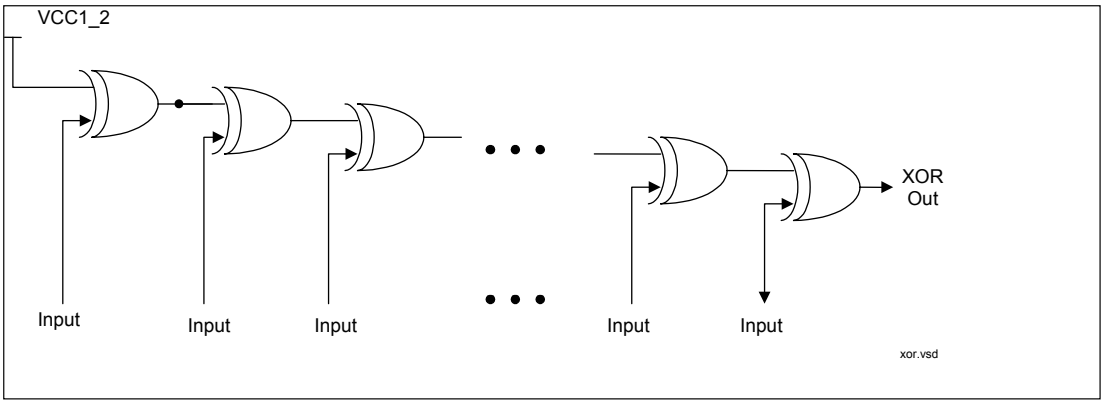
	Required Straps at Rising Edge of RSTIN#		
XOR Chains	ST[2]=0	G_GNT#=0	SBA[1]=0
SBA XOR Chain	ST[2]=0	G_GNT#=0	SBA[0]=0
All "Z" Test Mode	ST[2]=0	G_GNT#=0	SBA[7]=0

10.1. XOR Chain Mode

An XOR-tree is a chain of XOR gates, each with one input pin connected to it. When an XOR chain is enabled, all output and bi-directional buffers within that chain are tri-stated, except for the XOR chain output. However, for XOR chain testing the IO buffer sense amps and diff amps must be turned ON.

Refer to Figure 9 for example XOR chain.

Figure 9. XOR–Tree Chain



The algorithm used for in –circuit test is as follows

- Drive all input pins to an initial logic level 1. Observe the output corresponding to scan chain being tested.
- Toggle pins one at a time starting from the first pin in the chain, continuing to the last pin, from its initial logic level to the opposite logic level. Observe the output changes with each pin toggle.

10.1.1. XOR Test Mode Initialization

XOR test mode can be entered by pulling three shared pins (reset straps) low through the rising transition of RSTIN#. These signals are sampled during the rising transition or RSTIN#. The signals that need to be pulled are as follows:

ST[2] = 0 (PLL Bypass mode; it is recommended to enter PLL Bypass in XOR test mode)
G_GNT# = 0 (Global strap enable)
SBA[1] = 0 (XOR strap)

10.1.2. XOR Chains

Table 44. XOR Chains

Chain 0 Ball	Element #	Signal Name	Note	Initial Logic Level
AG6	1	HDSTBP1#	Input	1
AD3	2	HDSTBP0#	Input	1
U7	3	ADS#	Input	1
U2	4	HREQ0#	Input	1
U3	5	HA6#	Input	1
T4	6	HREQ4#	Input	1
U5	7	HREQ3#	Input	1
T5	8	HA4#	Input	1
T7	9	HREQ1#	Input	1
U6	10	HA3#	Input	1
R7	11	HREQ2#	Input	1
R5	12	HADSTB0#	Input	1
R3	13	HA7#	Input	1
R6	14	HA13#	Input	1
T3	15	HA9#	Input	1
P3	16	HA11#	Input	1
R2	17	HA5#	Input	1
N3	18	HA16#	Input	1
P5	19	HA12#	Input	1
P4	20	HA10#	Input	1
P7	21	HA8#	Input	1
N2	22	HA14#	Input	1
N5	23	HA15#	Input	1
L3	24	HA28#	Input	1
M3	25	HA18#	Input	1
M5	26	HA20#	Input	1
M4	27	HA19#	Input	1
L2	28	HA26#	Input	1
K3	29	HA22#	Input	1
N6	30	HA24#	Input	1
J2	31	HA23#	Input	1
J3	32	HA17#	Input	1
L6	33	HA25#	Input	1

Chain 0 Ball	Element #	Signal Name	Note	Initial Logic Level
L5	34	HA21#	Input	1
K5	35	HA27#	Input	1
K4	36	HA30#	Input	1
J5	37	HA31#	Input	1
L7	38	HA29#	Input	1
G15	39	RCVENIN#	Input	1
AH28	40	SBA0	Output	N/A

Chain 1 Ball	Element #	Ball Name	Note	Initial Logic Level
N7	1	HADSTB1#	Input	1
G4	2	SDQ63	Input	1
F4	3	SDQ58	Input	1
F3	4	SDQ59	Input	1
C2	5	SDQ61	Input	1
B2	6	SDQ60	Input	1
E2	7	SDQ62	Input	1
D3	8	SDQ57	Input	1
E3	9	SDQS7	Input	1
C3	10	SDQ56	Input	1
G16	11	Rsvd	Input	1
E4	12	SDQ55	Input	1
D4	13	SDQ50	Input	1
C4	14	SDQ54	Input	1
C5	15	SDQS6	Input	1
E6	16	SDQ52	Input	1
D6	17	SDQ49	Input	1
B3	18	SDQ51	Input	1
C6	19	SDQ48	Input	1
B5	20	SDQ53	Input	1
C7	21	SDQ47	Input	1
B7	22	SDQ46	Input	1
E8	23	SDQ43	Input	1
G10	24	Rsvd	Input	1
C8	25	SDQS5	Input	1
C9	26	SDQ41	Input	1
D8	27	SDQ42	Input	1
E10	28	SDQ40	Input	1
B9	29	SDQ45	Input	1
E11	30	SDQ44	Input	1
AH27	31	SBA1	Output	N/A

Chain 2 Ball	Element #	Ball Name	Note	Initial Logic Level
D10	1	SDQ39	Input	1
C10	2	SDQ35	Input	1
C11	3	SDQ38	Input	1
G9	4	Rsvd	Input	1
H7	5	Rsvd	Input	1
B11	6	SDQ34	Input	1
B13	7	SDQ36	Input	1
C12	8	SDQ33	Input	1
C13	9	SDQ37	Input	1
D12	10	SDQS4	Input	1
E13	11	SDQ32	Input	1
E15	12	SDQS8	Input	1
AG28	13	SBA2	Output	N/A

Chain 3 Ball	Element #	DDR Ball Name	Note	Initial Logic Level
C14	1	SDQ67	Input	1
D14	2	SDQ71	Input	1
C15	3	SDQ70	Input	1
C16	4	SDQ64	Input	1
D16	5	SDQ65	Input	1
B15	6	SDQ66	Input	1
C17	7	SDQ69	Input	1
B17	8	SDQ68	Input	1
D18	9	SDQ27	Input	1
E17	10	SDQ31	Input	1
B19	11	SDQS3	Input	1
C18	12	SDQ30	Input	1
E19	13	SDQ29	Input	1
C19	14	SDQ26	Input	1
C20	15	SDQ28	Input	1
D20	16	SDQ25	Input	1
C21	17	SDQ24	Input	1
B21	18	SDQ23	Input	1
E21	19	SDQ19	Input	1
C22	29	SDQ18	Input	1
D22	21	SDQ22	Input	1
C24	22	SDQ20	Input	1
C23	23	SDQS2	Input	1
B23	24	SDQ21	Input	1
D24	25	SDQ16	Input	1
E23	26	SDQ17	Input	1
B25	27	SDQ10	Input	1
C25	28	SDQ11	Input	1
C27	29	SDQ9	Input	1
D27	30	SDQ13	Input	1
B27	31	SDQ12	Input	1
C26	32	SDQS1	Input	1
E25	33	SDQ15	Input	1
E27	34	SDQ8	Input	1
N24	35	HL_STB#	Input	1
R24	36	AD_STB0	Input	1
AG27	37	SBA3	Output	N/A

Chain 4 Ball	Element #	Ball Name	Note	Initial Logic Level
D26	1	SDQ14	Input	1
F25	2	SDQ6	Input	1
B28	3	SDQ7	Input	1
C28	4	SDQ2	Input	1
E28	5	SDQ3	Input	1
F26	6	SDQS0	Input	1
H25	7	SDQ4	Input	1
H4	8	ETS#	Input	1
H3	9	Rsvd	Input	1
G3	10	Rsvd	Input	1
F27	11	SDQ1	Input	1
G2	12	Rsvd	Input	1
G28	13	SDQ0	Input	1
G27	14	SDQ5	Input	1
M27	15	HI_8	Input	1
M24	16	HI_10	Input	1
N28	17	HI_9	Input	1
L28	18	HI_6	Input	1
M25	19	HI_5	Input	1
N27	20	HI_2	Input	1
M26	21	HI_4	Input	1
N25	22	HI_STB	Input	1
L27	23	HI_7	Input	1
P25	24	HI_0	Input	1
P23	25	HI_3	Input	1
P24	26	HI_1	Input	1
R27	27	G_AD0	Input	1
R28	28	G_AD1	Input	1
U27	29	G_AD6	Input	1
R25	30	G_AD3	Input	1
T27	31	G_AD5	Input	1
T26	32	G_AD4	Input	1
U28	33	G_AD7	Input	1
R24	34	AD_STB0	Input	1
V27	35	G_AD9	Input	1
T25	36	G_AD2	Input	1

Chain 4 Ball	Element #	Ball Name	Note	Initial Logic Level
V26	37	G_AD8	Input	1
T24	38	G_AD12	Input	1
U24	39	G_AD13	Input	1
U25	40	G_AD14	Input	1
T23	41	G_AD10	Input	1
V24	42	G_AD15	Input	1
U23	43	G_AD11	Input	1
AE28	44	SBA4	Output	N/A

Chain 5 Ball	Element #	Ball Name	Note	Initial Logic Level
V25	1	G_CBE0#	Input	1
V23	2	G_CBE1#	Input	1
W28	3	G_DEVSEL#	Input	1
W25	4	G_PAR	Input	1
W27	5	G_IRDY#	Input	1
Y24	6	G_FRAME#	Input	1
W24	7	G_TRDY#	Input	1
AE23	8	WBF#	Input	1
W23	9	G_STOP#	Input	1
Y25	10	G_CBE2#	Input	1
AA23	11	G_CBE3#	Input	1
AA28	12	G_AD18	Input	1
Y26	13	G_AD17	Input	1
Y27	14	G_AD16	Input	1
AB27	15	G_AD20	Input	1
AB26	16	G_AD22	Input	1
AA25	17	G_AD26	Input	1
AA24	18	G_AD25	Input	1
AA27	19	G_AD21	Input	1
AC27	20	AD_STB1	Input	1
Y23	21	G_AD23	Input	1
AC25	22	G_AD28	Input	1
AB25	23	G_AD19	Input	1
AB23	24	G_AD24	Input	1
AD24	25	G_AD31	Input	1
AC24	26	G_AD29	Input	1
AC22	27	G_AD30	Input	1
AB24	28	G_AD27	Input	1
AE22	29	RBF#	Input	1
AF24	30	ST1	Input	1
AF22	31	PIPE#	Input	1
AF27	32	SBSTB	Input	1
AH25	33	G_GNT#	Input	1
AG25	34	ST0	Input	1
AG24	35	G_REQ#	Input	1
AG26	36	ST2	Input	1

Chain 5 Ball	Element #	Ball Name	Note	Initial Logic Level
AH17	37	HD61#	Input	1
AG16	38	HD55#	Input	1
AG17	39	HD56#	Input	1
AC16	40	HDSTBP3#	Input	1
AE11	41	HDSTBP2#	Input	1
AE27	42	SBA5	Output	N/A

Chain 6 Ball	Element #	Ball Name	Note	Initial Logic Level
R24	1	AD_STB1	Input	1
AF27	2	SBSTB	Input	1
AE17	3	CPURST#	Input	1
AD17	4	HD62#	Input	1
AE16	5	HD63#	Input	1
AH15	6	HD57#	Input	1
AG15	7	HD54#	Input	1
AF16	8	HD59#	Input	1
AC15	9	HDSTBN3#	Input	1
AE15	10	HD60#	Input	1
AG14	11	HD52#	Input	1
AC17	12	HD58#	Input	1
AF14	13	HD51#	Input	1
AE14	14	HD53#	Input	1
AH13	15	HD49#	Input	1
AD15	16	DBI3#	Input	1
AG13	17	HD48#	Input	1
AC14	18	HD50#	Input	1
AF12	19	HD47#	Input	1
AG12	20	HD45#	Input	1
AE12	21	HD40#	Input	1
AE13	22	HD46#	Input	1
AH9	23	DBI2#	Input	1
AG10	24	HD43#	Input	1
AH11	25	HD44#	Input	1
AG9	26	HD38#	Input	1
AG11	27	HD42#	Input	1
AD11	28	HDSTBN2#	Input	1
AF10	29	HD41#	Input	1
AE10	30	HD36#	Input	1
AC12	31	HD33#	Input	1
AC11	32	HD32#	Input	1
AC9	33	HD39#	Input	1
AE9	34	HD34#	Input	1
AC10	35	HD35#	Input	1

Chain 6 Ball	Element #	Ball Name	Note	Initial Logic Level
AD9	36	HD37#	Input	1
AH7	37	HD24#	Input	1
AH5	38	HD31#	Input	1
AG8	39	HD27#	Input	1
Y4	40	DEFER#	Input	1
W5	41	RS1#	Input	1
Y8	42	DPWR#	Input	1
AE24	43	SBA6	Output	N/A

Chain 7 Ball	Element #	Ball Name	Note	Initial Logic Level
AH3	1	HD29#	Input	1
AG4	2	HD16#	Input	1
AG7	3	HD28#	Input	1
AE8	4	HD19#	Input	1
AF8	5	HD30#	Input	1
AF6	6	HDSTBN1#	Input	1
AG5	7	DBI1#	Input	1
AE6	8	HD25#	Input	1
AE7	9	HD18#	Input	1
AG2	10	HD17#	Input	1
AC8	11	HD26#	Input	1
AH2	12	HD20#	Input	1
AD7	13	HD23#	Input	1
AG3	14	HD22#	Input	1
AC7	15	HD21#	Input	1
AE5	16	HD10#	Input	1
AF3	17	HD11#	Input	1
AF4	18	HD14#	Input	1
AD5	19	DBI0#	Input	1
AC6	20	HD12#	Input	1
AE2	21	HD15#	Input	1
AB7	22	HD9#	Input	1
AE3	23	HD8#	Input	1
AD4	24	HDSTBN0#	Input	1
AC3	25	HD13#	Input	1
AB5	26	HD1#	Input	1
AC5	27	HD5#	Input	1
AA6	28	HD7#	Input	1
AA5	29	HD2#	Input	1
AB3	30	HD3#	Input	1
AA3	31	HD6#	Input	1
AB4	32	HD4#	Input	1
AA2	33	HD0#	Input	1
Y5	34	HIT#	Input	1
Y7	35	BPRI#	Input	1
W6	36	RS2#	Input	1

Chain 7 Ball	Element #	Ball Name	Note	Initial Logic Level
Y3	37	HITM#	Input	1
V4	38	HTRDY#	Input	1
W3	39	HLOCK#	Input	1
V7	40	BR0#	Input	1
V3	41	BNR#	Input	1
W7	41	RS0#	Input	1
V5	43	DBSY#	Input	1
W2	44	DRDY#	Input	1
V8	45	DPSLP#	Input	1
AE25	46	SBA7	Output	N/A

NOTE: RSTIN# and all Rcomp buffers are not part of any XOR chain.

10.1.3. SBA XOR Test Mode Initialization

SBA XOR test mode will test the SBA pins and can be entered by pulling three shared pins (reset straps) low through the rising transition of RSTIN#. The signals that need to be pulled are as follows:
G_GNT# = 0 (Global strap enable)
SBA[0] = 0 (XOR SBAstrap)
ST[2] = 0 (PLL Bypass mode; it is recommended to enter PLL Bypass in XOR test mode)

10.1.4. SBA XOR Chain

Table 45. XOR Chains

SBA Chain Ball	Element #	Signal Name	Note	Initial Logic Level
AE27	1	SBA5	Input	1
AE25	2	SBA7	Input	1
AE28	3	SBA4	Input	1
AE24	4	SBA6	Input	1
AG27	5	SBA3	Input	1
AH28	6	SBA0	Input	1
AG28	7	SBA2	Input	1
AH27	8	SBA1	Input	1
Y24	9	G_FRAME#	Output	N/A

10.2. All “Z” Test Mode

In All “Z” mode all pure output and bi-direct buffers are tri-stated by the chip. This mode is used to measure pin leakage.

10.2.1. All “Z” Test Mode Initialization

The All “Z” test mode is entered by holding SBA[7] low while RSTIN# is active. SBA[7] must be held for a long enough time after the rising edge of RSTIN# to ensure hold time. The signals that need to be pulled low are as follows:

G_GNT# = 0 (Global strap enable)
SBA[7] = 0 (All “Z” strap)
ST[2] = 0 (PLL Bypass mode; Intel recommendsto enter PLL Bypass in XOR test mode)

The following pins can not be tristated during ALLZ or Leakage test mode: RSTIN#, 66IN, BCLK#, BCLK and all voltage reference pads.