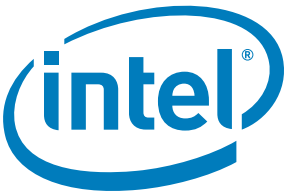


Intel® 82801DBM I/O Controller Hub 4 Mobile (ICH4-M)

Specification Update

September 2006

Document Number: 252663-008

Contents

Revision History

Version	Description	Date
001	Initial Release	January 2003
002	Updates include: • Added Specification Clarification for CTS bit	April 2003
003	Updates include: • Added PCI Non Linear Addressing Errata • Added Specification Clarification for Subtractive decode. • Added Document Change for HIREF values	June 2003
004	Updates include: • Added Multi Word DMA Mode 1 Errata	October 2003
005	Updates include: • Added USB Buffer Overrun Errata	February 2004
006	Updates include: • Added USB 2.0 Incorrect Periodic Frame List Pointer Fetch Erratum • Added USB CONFIGFLAG Clarification • Added CTS Clarification • Added Pb-Free Identification Information • Added Documentation Change - LPC I/F Generic I/O Decode Range 2 Base Address Aligned on 16-byte Boundary • Added Specification Clarification for GPIO_ROUT Register • Added Specification Clarification for GPIO Note Change • Added Specification Clarification for LPC Cycle Types • Added DPRSLPVR May Not Be Properly Initiated on Cold Boot Errata • Added Full-speed USB ISOC End of Packet Errata	June 2005
007	Updates include: • Added Specification Change for Delayed Transaction Discard Timer • Added Documentation Change for Power Management Timings	October 2005
008	Updates include: • Added Unexpected SMI with S1-M • Added AC ‘97 FIFO Error Bit Software Overrun • Added LPC Starvation Erratum	September 2006

§

Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. All references to ICH4 in this document refer to ICH4-M component.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 82801DBM I/O Controller Hub 4 - Mobile (ICH4-M) Datasheet	252337-001

Nomenclature

Errata are design defects or errors. Errata may cause the ICH4's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the Intel® 82801DBM I/O Controller Hub 4-Mobile (ICH4-M). Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document

Errata (Sheet 1 of 2)

Erratum Number	Stepping	Status	ERRATA
1	B1	No Fix	SMBus Arbitration Erratum
2	B1	No Fix	LPC Reset Timing
3	B1	No Fix	Master Abort Mode
4	B1	No Fix	SE0 during Resume Causes Disconnect
5	B1	No Fix	PCI Non-Linear Addressing Erratum
6	B1	No Fix	Multi word DMA Mode 1 Erratum
7	B1	No Fix	USB Buffer Overrun Erratum

Errata (Sheet 2 of 2)

Erratum Number	Stepping	Status	ERRATA
8	B1	No Fix	USB2 Incorrect Periodic Frame List Pointer Fetch
9	B1	No Fix	DPRSLPVR May Not Be Properly Initiated on Cold Boot
10	B1	No Fix	Full-speed USB ISOC End of Packet
11	B1	No Fix	Unexpected SMI with S1-M
12	B1	No Fix	AC 97' FIFO Error Bit Software Overrun
13	B1	No Fix	LPC Starvation Erratum

Specification Changes

Number	SPECIFICATION CHANGES
1	Delayed Transaction Discard Timer.

Specification Clarifications

Number	SPECIFICATION CLARIFICATIONS
1	CTS (CPU Thermal Trip Status) Bit Clarification
2	Subtractive Decode Clarification
3	USB CONFIGFLAG Clarification
4	CTS Clarification
5	GPIO_ROUT Register Clarification
6	GPIO Note Change Clarification
7	LPC Cycle Clarification

Documentation Changes

Number	DOCUMENTATION CHANGES
1	PCI Device Revision ID
2	Section 9.7.5 Correction
3	HIREF Tolerance Change
4	Generic Decode Range 2 Register Description Change
5	THRMTRIP# Timing Correction

§

Identification Information

Markings

Stepping	S-Spec	Top Marking	Notes
B1	SL6DN	82801DBM	Production sample
B1	SL8DE	82801DBM	Production Pb-Free

§

Errata

1. SMBus Arbitration Erratum

Problem: ICH4-M will not detect a bus collision when attempting to STOP at the end of a SMBus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, ICH4 does not set the Bus Error bit.

Implication: A master attempting a transfer that had actually "lost" may think that its transaction was completed when it was not completed.

Workaround: None

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

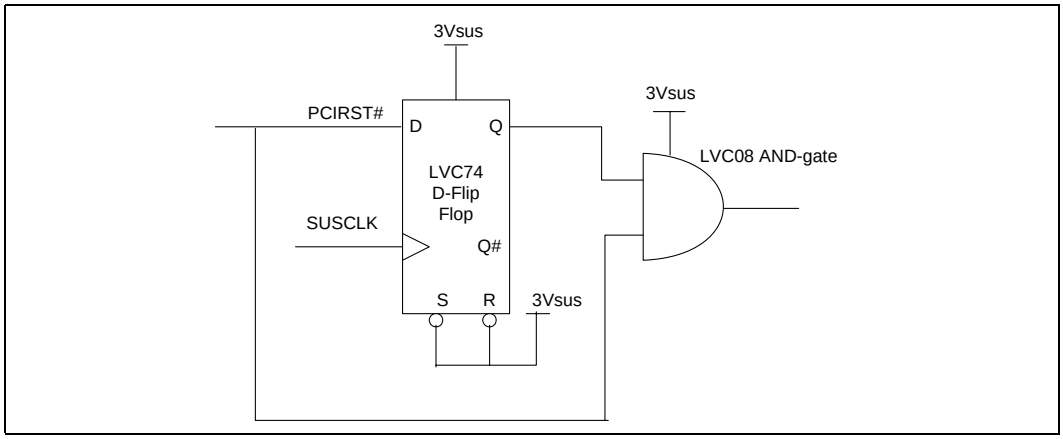
2. LPC Reset Timing

Problem: The ICH4-M specified 1–3 RTC timing of SUS_STAT# inactive to PCIRST# inactive violates the LPC Rev 1.0 specification of "at least 60 μs."

Implication: Some LPC devices (based on LPC Rev 1.0) may not properly reset resulting in failure of the system to boot or resume from a sleep state.

Workaround: Use any one of these three workarounds:

1. Delay PCIRST# by 1 SUSCLK using a D-flop and an AND gate to the LPC devices.



2. Do a CF9 hard reset within the 1st 100 ms of POST. This will reset the system.
3. Do not connect the SUS_STAT# to the SIO PD input; instead, implement an external pull-up resistor on the PD input of the SIO.

Status: There are no plans to fix this erratum.For steppings affected, see the *Summary Tables of Changes*.

3. Master Abort Mode

Problem: ICH4-M Master Abort Mode (BRIDGE_CNT – Bridge Control Register, D30:F0, offset 3E–3Fh, bit 5) is a new function. It was implemented incorrectly. A missing qualification can cause a Target Abort signal to a PCI agent that was uninvolved in the transfer.

Implication: ICH4-M could Target Abort the wrong bus master.

Workaround: De-feature Master Abort Mode. Power on default is Master Abort Mode bit is disabled. BIOS needs to make sure this bit is not enabled.

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

4. SE0 during Resume Causes Disconnect

Problem: A transient SE0 during an upstream resume signal from the USB peripheral to the ICH4-M while the system is in S3/S4 sleep states will cause the ICH4 to register a disconnect. This violates the USB Specification, Revision 1.1.

Implication: The implication is Operating System dependent. It can range from additional latency on a resume before the USB device is functional (after a resume), to the USB device no longer works after a resume - in which case a system reboot must be done to obtain USB device functionality. In all cases the rest of the system does resume.

Workaround: None

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

5. PCI Non-Linear Addressing

Problem: If a PCI Memory Read Multiple or Memory Read Line transaction falls on the last DWORD of a 32 byte cache line boundary and non-linear addressing (cache-line wrap mode) is used, the ICH4-M will pre-fetch data past the cache line boundary. All subsequent PCI bus master reads will get incorrect data. Subsequent processor cycles to PCI/LPC will get blocked behind the surplus data resulting in a system hang.

Implication: System hang only seen in synthetic test environment. No known commercial PCI devices support cache-line wrap mode using Memory Read Multiple or Memory Read Line.

Workaround: None

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

6. Multi Word DMA Mode 1

Problem: Data hold time of multi word DMA Mode 1 writes may not meet ATA specification

Implication: No known implication.

Workaround: Program the controller to (Programmed Input/Output) PIO Mode 4 instead.

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

7. USB Buffer Overrun Erratum

Problem: If a USB full-speed isochronous or asynchronous inbound transaction is on the verge of an overrun event (requires 20 µs of system latency) and the USB FIFO begins to empty during a 30 ns window immediately prior to the overrun event actually occurring, extra data can be sent to memory. This erratum has only been reproduced with synthetic test environments and not with real world applications.

Implication: Extra data may be sent to memory and/or data could be erroneously written beyond the boundary of the USB buffer allocation. This may result in unpredictable system behavior. There is no known exposure with real world applications.

Workaround: No workaround.

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

8. USB2 Incorrect Periodic Frame List Pointer Fetch

Problem: The USB2 controller may fetch an incorrect periodic frame list pointer when the periodic activity is heavily scheduled and there are large latencies on descriptor requests to memory when running HS isochronous or interrupt traffic. Note: This has only been reproduced in synthetic test environments.

Implication: There may be intermittent audio pops or lost video frames on USB2 HS devices when the system is heavily loaded in synthetic test environments

Workaround: No workaround.

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

9. DPRSLPVR May Not Be Properly Initiated on Cold Boot

Problem: DPRSLPVR signal may not be properly initialized until ICH4-M's core well power rails (Vcc1_5, Vcc3_3) become stable and ICH4-M receives PCI clock.

Implication: System may fail to boot depending on the power sequencing logic implementation and CPU VR solution used on the platform. Observing the failure is platform design dependent, not all systems are susceptible to this erratum.

Workaround: An external weak pull down resistor of 100 kΩ will ensure DPRSLPVR does not float on affected systems.

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

10. Full-speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None

Status: There are no plans to fix this erratum. For steppings affected, see the *Summary Tables of Changes*.

11. Unexpected SMI with S1-M

Problem: When entering S1-M, peripheral PCI clocks including the PCI clock to the Super IO will be stopped one clock after STP_PCI# is asserted. In the S1-M transition SUS_STAT# is asserted, and in response some SERIRQ agents may drive active low on SERIRQ. The active low may be maintained on the SERIRQ line, as the SERIRQ agents observes SUS_STAT# assertion. The PCI clock to the ICH4-M is stopped later after SLP_S1# is asserted. Since PCI clocks to ICH4-M are still running for some time, the ICH4-M may misinterpret this as a request for a SMI#, INTR, or NMI (depending on which SERIRQ slot is being sampled). Upon exit from S1-M and SMI#, INTR or NMI may occur in reponse to this misinterpretation.

Implication: Unexpected INTR, SMI#, or NMI may occur when resuming from S1-moble suspend state. System implications will be BIOS/OS dependent. Based on the type of interrupt detected this may result in a system hang.

Workaround: A BIOS workaround has been validated in which SERIRQ must be disabled before entering S1-M state and re-enabled after exiting from S1-M. This will prevent generation of unexpected interrupts. SERIRQ can be disabled by writing a '0' to D31:F0;64h bit 7.

Contact your local Intel Field representative if you require more detailed BIOS workaround.

Status: There are no plans to fix this erratum. For affected steppings, see the *Summary Tables of Changes*.

12. AC'97 FIFO Error Bit Software Overrun

Problem: The ICH4 may set the FIFOE Bit in the Input Status Register after a software overrun error occurs on a highly stressed system. The ICH4 should only set the FIFOE bit on a hardware overrun.

Bit affected depends on which stream is currently running:

PCM IN - PISR (D31:F5: I/O Offset NABMBAR+06h:bit-4)

Mic IN - MCSR (D31:F5: I/O Offset NABMBAR+26h:bit-4)

Mic 2 IN - MC2SR (D31:F5: I/O Offset MBBAR+46h:bit-4)

PCM 2 IN - PI2SR (D31:F5: I/O Offset MBBAR+56h:bit-4)

Modem IN - MISR (D31:F6: I/O Offset MBAR+06h:bit-4)

Implication: No data was lost because the software did not expect an additional sample. Driver vendors typically do not use this status bit in their production drivers.

Workaround: None.

Status: There are no plans to fix this erratum. For affected steppings, see the *Summary Tables of Changes.*

13. LPC Starvation Erratum

Problem: Latency issues on LPC may occur if a PCI bus master is performing large upstream bursts to memory and no other PCI devices are requesting the bus. If an LPC cycle occurs during an upstream PCI burst, the completion of the LPC cycle may get delayed until the PCI device completes its transaction and de-asserts it REQ#.

Implication: Under certain operating conditions, latency on the LPC bus may cause delays in accessing data from an LPC based device.

Workaround: None.

Status: No Fix. For affected steppings, see the *Summary Tables of Changes*.

§

Specification Changes

1. Delayed Transaction Discard Timer

Section 8.1.27 describes the ICH4 configuration register. Bit-2 is now defined as indicated.

2	**Delayed Transaction Discard Timer** — R/W. When set to 1 this bit shortens all delayed transaction discard timers from 32 µs to 4 µs. Note: Setting this bit may improve system performance issues with certain non-optimally behaved PCI devices but may violate the *PCI-to-PCI Bridge Architecture Specification* Rev 1.1 (section 5.3.2).

§

Specification Clarifications

1. CTS (CPU Thermal Trip Status) Bit Clarification

The following note has been added to bit 3 of GEN_PMCON_2 register in Section 9.8.12.

Note: The CF9 reset in the description refers to CF9h type core well reset which includes SYSRST#, PWROK/VGATE Low, SMBus hard reset, TCO Timeout. This type of reset will clear CTS bit.

2. Subtractive Decode Clarification

Change Dependency/Comments of Memory Range “All other” in Table 6-4 “Memory Decode Ranges from processor perspective” to the following:

Table 6-4 Memory Decode Ranges from Processor Perspective

Memory Range	Target	Dependency/Comments
All Other	PCI	If the address is below 16M, is not in one of the above BIOS. Ranges, and positive decode is disabled; then the cycle will be forwarded to LPC as a standard LPC memory cycle. If the address is above 16M, if the cycle is not claimed by a device on PCI and not the Intel ICH4-M, then the cycle will Master-Abort on PCI.

3. USB CONFIGFLAG Clarification

The paragraph associated with Section 12.2.2.8 (CONFIGFLAG - Configure Flag Register) is completely replaced with the paragraph below:

This register is in the suspend power well. It is only reset by hardware when the suspend power is initially applied or in response to a host controller reset.

4. CTS Clarification

The following note is added to the description of the CTS bit (Section 9.8.1.2):

Note: The CF9h reset in this description refers to the CF9h type core well reset which includes SYS_RESET#, PWROK/VRMPWRGD low, SMBus hard reset, and TCO timeout. This type of reset will clear the CTS bit.

5. GPIO_ROUT Register Clarification

The GPIO0 Route register description should read as follows:

Software must set this bit field to generate the appropriate type of system interrupt, depending on how the **SCI_EN** bit is set. For example, if the **SCI_EN** bit is set, then this field must be programmed to 00b or 10b. If the **SCI_EN** bit is cleared, then this field must be programmed to 00b or 01b. Software must also update this field if the **SCI_EN** bit is changed.

6. GPIO Note Change Clarification

Note 1 of Table 5-50 (GPIO Implementation) should read as follows:

All GPIOs default to their alternate function and therefore may be subject to further design constraints.

7. LPC Cycle Clarification

The following changes are made to Table 5-2 LPC Cycle Types Supported in section 5.3.1.1:

- “See Note 1” is removed from the comment column for both I/O Read and I/O Write cycle types.
- “See Note 1” is added to the comment column for both Memory Read and Memory Write types.

§

Documentation Changes

1. PCI Device Revision ID

PCI Revision ID Register Values (PCI Offset 08h) for all ICH4-M functions are shown below.

This information is not found in the datasheet. This is the standard reference document.

Table 1. PCI Device Revision ID Table

Device Function	Description	ICH4-M Dev ID	ICH4-M B1 Rev ID
D30, F0	P2P Bridge	2448h	83h
D31, F0	P2L Bridge	24CCh	03h
D31, F1	IDE	24CAh	03h
D31, F3	SMBus	24C3h	03h
D31, F5	AC '97 Audio	24C5h	03h
D31, F6	AC '97 Modem	24C6h	03h
D8, F0	LAN	103Ah	83h[1]
D29, F0	USB UHCI #1	24C2h	03h
D29, F1	USB UHCI #2	24C4h	03h
D29, F2	USB UHCI #3	24C7h	03h
D29, F7	USB EHCI	24CDh	03h

Note: Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 103Ah is used. Lan Device ID's correspond to each of the PHY types listed:
1039h 82562ET/EZ,
103Ah 82562ET/EZ (CNR),
103Bh 82562EM/EX,
103Ch 82562EM/EX (CNR),

2. Section 9.7.5 Correction

Section 9.7.5 Reset Control Register, bit-1 incorrectly refers to the term EDS which is replaced with the term datasheet.

3. HiREF Tolerance Change

The HIREF tolerance has changed from 350 mV ±2% to 350 mV ±8%. The HIREF entry in Table 17-6 "Other DC Characteristics" has been changed to the following:

Table 17-6 Other DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
HIREF	Hub Interface Reference Voltage	0.322	0.378	V	HI 1.5 Mode

4. Generic Decode Range 2 Register Description Change

The description in Section 9.1.33 for the Generic I/O Decode Range Base Address should read the following:

> "This address is aligned on a 16-byte boundary and must have address lines 31:16 as 0."

5. THRMTRIP# Timing Correction

The THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active time, t220, in Table 17-20 (Power Management Timings) is corrected from 2 PCI CLK to 3 PCI CLK.

§