



## Low EMI, Spread Modulating, Clock Generator

### Features:

- ICS91730 is a Spread Spectrum Clock targeted for Mobile PC and LCD panel applications that generates an EMI-optimized clock signal (EMI peak reduction of 7-14 dB on 3rd-19th harmonics) through use of Spread Spectrum techniques.
- ICS91730 focuses on the lower input frequency range of 14.318 to 80.00 MHz with a spread modulation of 20kHz to 40kHz.

### Specifications:

- Supply Voltages:  $V_{DD} = 3.3V \pm 0.3V$
- Frequency range:  $14.318 \text{ MHz} \leq F_{in} \leq 80 \text{ MHz}$
- Cyc to Cyc jitter: <150ps
- Output duty cycle 45-55%
- Guarantees +85°C operational condition.
- 8-pin SOIC
- Reference input

### Pin Configuration

CLKIN	1	8	PD#*
VDD	2	7	SCLK
GND	3	6	SDATA
CLKOUT	4	5	REF_OUT/FS_IN1*

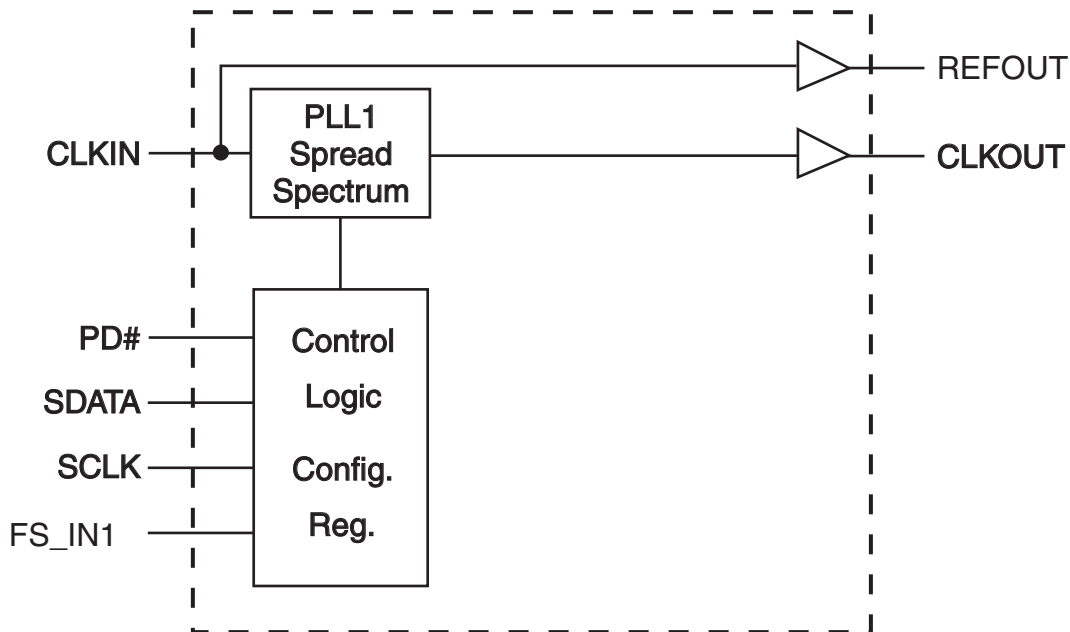
#### 8 Pin SOIC

\* Internal Pull-Up Resistor

### Functionality

FSIN 1	MHz	Spread % default
0	14.318 MHz in --> 27MHz out	-0.8 down spread
1	27.00MHz in --> 27.00MHz out	-1.25 down spread

### Block Diagram





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### Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	CLKIN	POWER	Input for reference clock.
2	VDD	INPUT	Power supply, nominal 3.3V
3	GND	OUTPUT	Ground pin.
4	CLKOUT	I/O	Modulated clock output.
5	REF_OUT/FS_IN1*	I/O	Un-modulated 3.3V reference clock output.
			Frequency select latch input. Refer to the functionality table.
6	SDATA	POWER	Data pin for SMBus circuitry, 5V tolerant.
7	SCLK	POWER	Clock pin of SMBus circuitry, 5V tolerant.
8	PD#*	POWER	Asynchronous active low input pin, with 120Kohm internal pull-up resistor, used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.

\* Internal Pull-Up Resistor \*\* Internal Pull-Down Resistor



**Table 1: Frequency Configuration Table**  
(See I2C Byte 0)

	FS4	FS3	FS2	FS1	FS0	Sprd Type	Sprd %
14in/27out	0	0	0	0	0	DOWN SPREAD (-)	0.60
	0	0	0	0	1		0.80
	0	0	0	1	0		1.00
	0	0	0	1	1		1.25
	0	0	1	0	0		1.50
	0	0	1	0	1		2.00
	0	0	1	1	0	CENTER SPD (+/-)	0.50
	0	0	1	1	1	CENTER SPD (+/-)	1.00
14in/14out 27in/27out	0	1	0	0	0	DOWN SPREAD (-)	0.60
	0	1	0	0	1		1.00
	0	1	0	1	0		0.80
	0	1	0	1	1	CTR SPD	0.3
	0	1	1	0	0	DOWN SPREAD (-)	1.50
	0	1	1	0	1		1.75
	0	1	1	1	0		2.00
	0	1	1	1	1		2.50
	1	0	0	0	0		3.00
	1	0	0	0	1		1.25
	1	0	0	1	0	CENTER SPD (+/-)	0.40
	1	0	0	1	1		0.50
	1	0	1	0	0		0.70
	1	0	1	0	1		1.00
1	0	1	1	0	1.20		
1	0	1	1	1	1.50		
48in/48out 66in/66out	1	1	0	0	0	DOWN SPREAD (-)	0.60
	1	1	0	0	1		0.80
	1	1	0	1	0		1.00
	1	1	0	1	1		1.25
	1	1	1	0	0		1.50
	1	1	1	0	1		2.00
	1	1	1	1	0	CENTER SPD (+/-)	0.50
	1	1	1	1	1	CENTER SPD (+/-)	1.00

Above is the hard coded 5 bit (32 entry) ROM table.

FS3:0 are ONLY accessible through I2C software programming bits (byte0 bits5:7). FS4 can also be decoded from FS\_IN1 latched input hardware pins.

FS\_IN1 →FS4. Upon power-up the default is to use hardware selection of FS\_IN1 latched value.

FS3 = 0, FS2 = 0, FS1 = 0, FS0 = 1 upon power-up (refer to the functionality table on page 1).

To access non-default spread entries in the ROM, byte0 programming should be used. In order to change the power up default of FS\_IN1 = 1 (-1.25% down spread) to any other spread % entry, first change byte0bit 0 to software selection by switching this bit to a '1' and then program the desired percentage by changing byte0 bits 7:3.



## General I<sup>2</sup>C serial interface information

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D4<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D4<sub>(H)</sub>
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D5<sub>(H)</sub>
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if X<sub>(H)</sub> was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D4 <sub>(H)</sub>			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
Data Byte Count = X			
		ACK	
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
Byte N + X - 1			
		ACK	
P	stoP bit		

Index Block Read Operation			
Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address D4 <sub>(H)</sub>			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address D5 <sub>(H)</sub>			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK		X Byte	
ACK			Beginning Byte N
○			
○			○
○			○
		Byte N + X - 1	
N	Not acknowledge		
P	stoP bit		



Byte 0	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	-	FS0	Spread/FS0	RW	Srpead Pcentage See Table1 These are I2C bits only		1
Bit 6	-	FS1	Spread/FS1	RW			
Bit 5		FS2	Spread/FS2	RW			
Bit 4		FS3	Spread/FS3	RW			
Bit 3		FS4	FS4	RW			
Bit 2		PD# Tri_Sate	PD# Tri_Sate	RW	Hi-Z	LOW	1
Bit 1		Spread Enable	Spread Enable	RW	OFF	ON	1
Bit 0		HW/SW Control	Spread Spectrum Control FS 3:4 Hard/Software Select	RW	HW	SW	0

Byte 1	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7		REF_OUT	REF_OUT_Enable	RW	Disable	Enable	1
Bit 6	-	REF_OUT	Slew Rate REF-OUT	RW	Nominal	Fast	1
Bit 5		FS-IN_1	FS-IN_1 Readback	R	-	-	X
Bit 4		(Reserved)	(Reserved)	R	-	-	0
Bit 3		CLK_OUT	Slew Rate CLK-OUT	RW	Nominal	Fast	1
Bit 2		CLK_OUT	CLK_OUT_Enable	RW	Disable	Enable	1
Bit 1		(Reserved)	(Reserved)	R	-	-	1
Bit 0		(Reserved)	(Reserved)	R	-	-	1

Byte 2	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	x	-	(Reserved)	-	-	-	1
Bit 6	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 5	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 4	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 3	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 2	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 1	x	(Reserved)	(Reserved)	RW	Disable	Enable	1
Bit 0	x	(Reserved)	(Reserved)	RW	Disable	Enable	1



Byte 3	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	x	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 4	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 6	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 5	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 4	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 5	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	(Reserved)	(Reserved)	-	-	-	1
Bit 6	X	(Reserved)	(Reserved)	-	-	-	1
Bit 5	X	(Reserved)	(Reserved)	-	-	-	1
Bit 4	X	(Reserved)	(Reserved)	-	-	-	1
Bit 3	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 2	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 1	X	(Reserved)	(Reserved)	RW	-	-	1
Bit 0	X	(Reserved)	(Reserved)	RW	-	-	1

Byte 6	Affected Pin			Type	Bit Control		PWD
	Pin #	Name	Control Function		0	1	
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1



### Absolute Maximum Ratings

- Supply Voltage..... 3.7 V
- Voltage on any pin with respect to GND ... -0.5 to +3.7 V
- Storage Temperature..... -55°C to +125°C
- Power Dissipation ..... 0.5 W

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 85°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V <sub>IH</sub>		2		V <sub>DD</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>		V <sub>SS</sub> - 0.3		0.8	V
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-5		5	mA
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5			mA
Powerdown Current	I <sub>DD3,3PD</sub>			1	5	mA
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V		14.318		MHz
Pin Inductance	L <sub>pin</sub>				7	nH
Input Capacitance <sup>1</sup>	C <sub>IN</sub>	Logic Inputs			5	pF
	C <sub>OUT</sub>	Output pin capacitance			6	pF
	C <sub>INX</sub>	X1 & X2 pins	27	36	45	pF
Transition time <sup>1</sup>	T <sub>trans</sub>	To 1st crossing of target frequency			3	ms
Settling time <sup>1</sup>	T <sub>s</sub>	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization <sup>1</sup>	T <sub>STAB</sub>	From V <sub>DD</sub> = 3.3 V to 1% target frequency			3	ms
Delay <sup>1</sup>	t <sub>PZH</sub> , t <sub>PZL</sub>	Output enable delay (all outputs)	1		10	ns

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**Electrical Characteristics - CLKOUT**

$T_A = 0 - 85^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	$V_{OH3}$	$I_{OH} = -1\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL3}$	$I_{OL} = 1\text{ mA}$			0.4	
Rise Time	$t_{r3}$	$V_{OL} = 0.41\text{V}$ , $V_{OH} = 0.86\text{V}$	0.5	0.6	1	ns
Fall Time	$t_{f3}$	$V_{OH} = 0.86\text{V}$ , $V_{OL} = 0.41\text{V}$	0.5	0.6	1	ns
Duty Cycle	$d_{i3}$	measurement from differential waveform - 0.35V to +035V	45	50	55	%
Jitter, Cycle to cycle	$t_{j\text{cyc-cyc}}^1$	$V_T = 50\%$		50	150	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

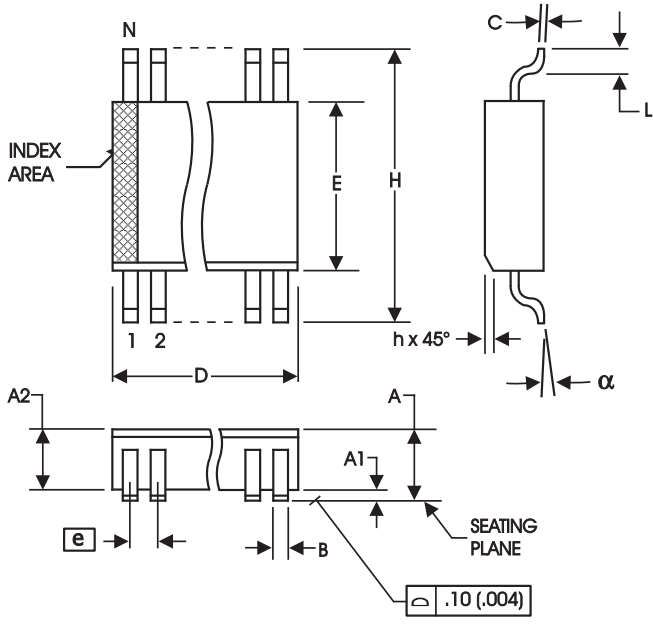
**Electrical Characteristics - REF**

$T_A = 0 - 85^\circ\text{C}$ ;  $V_{DD} = 3.3\text{V} \pm 5\%$ ;  $C_L = 10\text{-}20\text{ pF}$  (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	$R_{DSP1}^1$	$V_O = V_{DD} \cdot (0.5)$	20	48	60	$\Omega$
Output High Voltage	$V_{OH}^1$	$I_{OH} = -1\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}^1$	$I_{OL} = 1\text{ mA}$			0.4	V
Output High Current	$I_{OH}^1$	$V_{OH@MIN} = 1.0\text{ V}$ , $V_{OH@MAX} = 3.135\text{ V}$	-29		-23	mA
Output Low Current	$I_{OL}^1$	$V_{OL@MIN} = 1.95\text{ V}$ , $V_{OL@MAX} = 0.4\text{ V}$	29		27	mA
Rise Time	$t_{r1}^1$	$V_{OL} = 0.4\text{ V}$ , $V_{OH} = 2.4\text{ V}$	1	1.2	2	ns
Fall Time	$t_{f1}^1$	$V_{OH} = 2.4\text{ V}$ , $V_{OL} = 0.4\text{ V}$	1	1.2	2	ns
Duty Cycle	$d_{t1}^1$	$V_T = 1.5\text{ V}$	45	51	55	%
Jitter	$t_{j\text{cyc-cyc}}^1$	$V_T = 1.5\text{ V}$		105	300	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.





8-pin SOIC

150 mil (Narrow Body) SOIC

SYMBOL	In Millimeters		In Inches	
	COMMON DIMENSIONS		COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	SEE VARIATIONS		SEE VARIATIONS	
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	4.80	5.00	.1890	.1968

Reference Doc.: JEDEC Publication 95, MS-012

10-0030

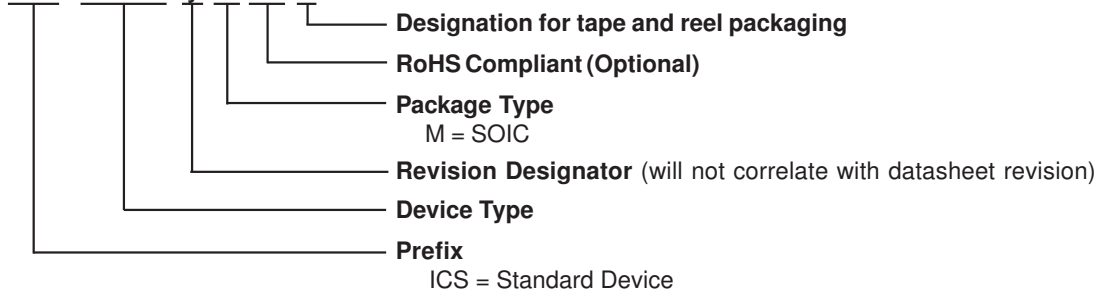
Ordering Information

ICS91730yMLFT

\*Due to package size constraints actual top side marking may differ from the full orderable part number.

Example:

ICS XXXX y M LFT





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### Revision History

Rev.	Issue Date	Description	Page #
B	06/25/04	Add Lead Free package description to Ordering Information	10
C	06/29/04	Add Revision History table to datasheet.	11
D	05/23/05	1. Revise ABS Max Ratings. 2. Updated REF Electrical Characteristics Table. 3. Updated LF Ordering Information from "Lead Free" to "RoHS Compliant".	8-10
E	06/04/08	Updated MLF Ordering Information	9