High Definition Audio SoundMAX Codec

AD1984A

FEATURES

Microsoft Vista Premium Logo for desktop
- **96+ dB audio outputs, 90 dB audio inputs**
- **WLP 3.0 and 4.0**

Security feature prevents unauthorized recording
2 stereo headphone amplifiers
Internal 32-bit arithmetic for greater accuracy
Impedance and presence detection on all jacks
Full analog mixer with DAC inputs
3 independent microphone bias pins
Digital and analog PCBeep
3 general-purpose digital I/O (GPIO) pins
3.3 V analog supply voltage
1.7 V to 1.9 V or 3.3 V digital supply voltages
1.5 V or 3.3 V HD Audio link signaling voltage
Advanced power management modes
48-lead, RoHS compliant LFCSP_VQ package

192 kHz DACs/ADCs

2 independent stereo DAC/ADC pairs
Simultaneous record of 2 stereo channels
Simultaneous playback of 2 stereo channels
Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
16-, 20-, and 24-bit resolution
Selectable stereo mixer on outputs

STEREO DIGITAL MICROPHONE INTERFACE

Two 192 kHz digital microphone channels
Supports 1 or 2 microphones per pin
Selectable bit clock rates of 1.5 MHz, 2.0 MHz, and 3.0 MHz
Mono and stereo array support
8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
16-, 20-, and 24-bit resolution

S/PDIF OUTPUT

Supports 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sample rates
16-, 20-, and 24-bit data; PCM and AC3 formats
Digital PCM gain control

AUXILIARY PINS

Stereo CD/auxiliary I/O port with ground sense
Stereo auxiliary/dock I/O port
Mono out pin for internal speakers or telephony

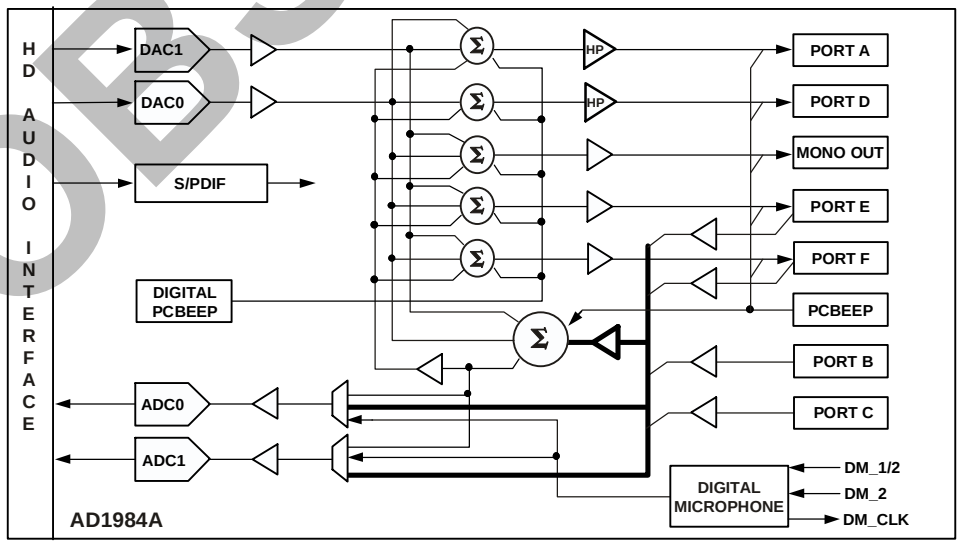

Figure 1. Functional Block Diagram

Rev. 0

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REVISION HISTORY

4/08—Rev 0. Initial version

GENERAL DESCRIPTION

The AD1984A audio codec and SoundMAX® software provide superior high definition audio quality that exceeds Vista Premium performance. The AD1984A has two 192 kHz DAC pairs, two 192 kHz ADC pairs, an S/PDIF output, a 2-channel digital microphone interface, and digital and analog PCBeep. These features make the AD1984A the right choice for desktop and notebook PCs where performance is key.

The AD1984A is available in a 48-lead, RoHS compliant lead frame chip scale package in both reels and trays. See Ordering Guide on Page 19.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the AD1984A SoundMAX codec's architecture and functionality. Detailed widget information is available in the AD1984A Programmers Reference Manual. Please contact your local Analog Devices, Inc., sales representative for more information.

JACK CONFIGURATION

The guidelines shown in Table 1 through Table 3 should be used when selecting ports for particular functions.

Table 1. Typical Desktop Configuration

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Microphone
Port D	Rear Panel Line-Out/Headphone
S/PDIF	Optical/RCA S/PDIF Output

Table 2. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port F	Internal Stereo Speakers
S/PDIF	Optical/RCA S/PDIF Output

Table 3. Typical Notebook Configuration with Dock Interface

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Dock Line-Out/Headphone
Port E	Dock Line-In/Microphone
Port F	Internal Stereo Speakers
S/PDIF	Optical/RCA S/PDIF Output

AD1984A SPECIFICATIONS

TEST CONDITIONS

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate F_S	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	–3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC[1]	10 kΩ Output Load: Line-Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

[1] DAC/ADC tests are performed with AES-17 filter enabled.

PERFORMANCE

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 kΩ loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–86		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		96		dB
Signal-to-Noise Ratio		96		dB
Headphone Drive (32 Ω loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		–80		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		96		dB
Signal-to-Noise Ratio		96		dB
Microphone/Line-In (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		–81		dB
Dynamic Range (–60 dB in ref to f_S A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

GENERAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
DIGITAL DECIMATION AND INTERPOLATION FILTERS—f_S = 8 kHz to 192 kHz[1]				
Pass Band	0		0.4 f_S	Hz
Pass-Band Ripple			±0.005	dB
Stop Band	0.6 f_S			Hz
Stop-Band Rejection			–100	dB
Group Delay		20		$1/f_S$
Group Delay Variation over Pass Band		0		µs
ANALOG-TO-DIGITAL CONVERTERS				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)		±0.2	±0.5	dB
ADC Offset Error[1]			±5	mV
ADC Crosstalk[1]				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–85		dB
Line Inputs to Other		–100	–80	dB

Parameter		Min	Typ	Max	Unit
DIGITAL-TO-ANALOG CONVERTERS					
Resolution			24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)[1]				±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)				±0.5	dB
Total Audible Out-of-Band Energy (Measured from 0.6 × f_S to 20 kHz)[1]			–85		dB
DAC Crosstalk (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)[1]			–95		dB
DAC VOLUMES					
Step Size			1.5		dB
Output Gain/Attenuation Range		–58.5		0	dB
Mute Attenuation of 0 dB Fundamental[1]			–80		dB
ADC VOLUMES					
Step Size			1.5		dB
PGA Gain/Attenuation Range		–58.5		+22.5	dB
ANALOG MIXER					
Signal-to-Noise Ratio Input to Output—Ports B, C, E, or F to Port D Output			95		dB
Step Size: All Mixer Inputs			–1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		–34.5		+12.0	dB
ANALOG LINE LEVEL OUTPUTS					
Full-Scale Output Voltage		1.0			V rms
		2.83			V p-p
Ports A, D, E, F, and Mono Out					
	Output Impedance[1]		190		Ω
	External Load Impedance[1]	10			kΩ
	Output Capacitance[1]		15		pF
	External Load Capacitance			1000	pF
ANALOG HP DRIVE OUTPUTS					
Full-Scale Output Voltage		1.0			V rms
		2.83			V p-p
Ports A and D					
	Output Impedance[1]			0.5	Ω
	External Load Impedance[1]	32			Ω
	Output Capacitance[1]		15		pF
	External Load Capacitance[1]			1000	pF
ANALOG INPUTS					
Input Voltages—Ports B, C, E, or F					
	Mic Boost = 0 dB		1		V rms
			2.83		V p-p
Input Voltages—Microphone Boost	Mic Boost = 10 dB		0.316		V rms
Amplifier, Ports B, C, or E			0.894		V p-p
	Mic Boost = 20 dB		0.1		V rms
			0.283		V p-p
	Mic Boost = 30 dB		0.032		V rms
			0.089		V p-p
Input Impedance					
PCBeep			23		kΩ
Ports B, C, E (Mic Boost = 0 dB)			150		kΩ
Port F			45		kΩ
Input Capacitance[1]			5	7.5	pF

Parameter		Min	Typ	Max	Unit
MICROPHONE BIAS					
MIC_BIAS-B, MIC_BIAS-C					
MIC_BIAS_IN (Pin 33) = 5 V or 3.3 V	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
MIC_BIAS_IN (Pin 33) = 5 V	V_{REF} Setting = 80%		3.7		V dc
	V_{REF} Setting = 100%		3.9		V dc
MIC_BIAS_IN (Pin 33) = 3.3 V	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
MIC_BIAS-E (When Enabled as BIAS)	V_{REF} Setting = High-Z		High-Z		
	V_{REF} Setting = 0 V		0		V dc
	V_{REF} Setting = 50%		1.65		V dc
	V_{REF} Setting = 80%		2.86		V dc
	V_{REF} Setting = 100%		3.0		V dc
Output Drive Current	V_{REF} Setting = 50%, 80%, or 100%		1.6		mA
GPIO 0					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
GPIO 1 and GPIO 2					
Input Signal High (V_{IH})		$AV_{DD} \times 0.60$		AV_{DD}	V
Input Signal Low (V_{IL})		0		$AV_{DD} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$AV_{DD} \times 0.72$		AV_{DD}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$AV_{DD} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA
DM Clock					
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$AV_{DD} \times 0.72$		AV_{DD}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$AV_{DD} \times 0.10$	V
DM_1/2 and DM_2					
Input Signal High (V_{IH})		$AV_{DD} \times 0.60$		AV_{DD}	V
Input Signal Low (V_{IL})		0		$AV_{DD} \times 0.24$	V
Input Leakage Current (Signal High) (I_{IH})			–150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		nA
S/PDIF					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Output Signal High (V_{OH})	I_{OUT} = –500 µA	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	I_{OUT} = +1500 µA	0		$DV_{IO} \times 0.10$	V
Input Leakage Current (Signal High) (I_{IH})			150		nA
Input Leakage Current (Signal Low) (I_{IL})			–50		µA

Parameter	Min	Typ	Max	Unit
POWER SUPPLY				
Analog (AV_{DD}) 3.3 V ± 5%				
Power Supply Range	3.13	3.30	3.46	V
Power Dissipation		75.9		mW
Supply Current		23		mA
Digital (DV_{DD}) 3.3 V ± 10%				
Power Supply Range	2.97	3.30	3.63	V
Power Dissipation		141.9		mW
Supply Current		43		mA
Digital (DV_{CORE}) 1.7 through 1.9 V ± 10%				
Power Supply Range	1.615	1.70	1.995	V
Power Dissipation		61		mW
Supply Current		36		mA
Digital I/O (DV_{IO}) 3.3 V ± 10%				
Power Supply Range	2.97	3.30	3.63	V
Power Dissipation		3.3		mW
Supply Current		1		mA
Digital I/O (DV_{IO}) 1.5 V ± 5.5%				
Power Supply Range	1.418	1.50	1.583	V
Power Dissipation		0.08		mW
Supply Current		0.05		mA
Power Supply Rejection (Reference to f_S 100 mV p-p Signal @ 1 kHz)[1]		80		dB

[1] Guaranteed but not tested.

HD AUDIO LINK SPECIFICATION

High definition audio signals comply with the High Definition Audio Specification. Please refer to these specifications at www.intel.com/standards/hdaudio.

POWER-DOWN STATES

Parameter	ID_{VDD} Typ (1.7 V)	ID_{VDD} Typ (3.3 V)	IA_{VDD} Typ	Unit
Function Node in D0, All Nodes Active	36	43	23	mA
Function Node in D3	15.75	17	1	mA
Function Node in D3[1]	7.5	7.5	1	mA
Codec in $\overline{\text{RESET}}$	3	3	3	mA
Individual Block Power Savings				
DAC Pair Powered Down Saves (Each)	4.5	6	5	mA
ADC Pair Powered Down Saves (Each)	4.5	6	3	mA
Mixer Power Control (and Associated Amps) Saves	0	0	2	mA
DM_CLK Powered Down Saves[2]	0	0	1	mA
MIC_BIAS Powered Down Saves[3]	0	0	0.1	mA

[1] Maximum power saving mode; Register 0x31FD, Bit 4.
[2] Test conditions: 30 pF load, 2.0 MHz frequency, 3.3 V A_{VDD}.
[3] Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the high-Z state. The 0 V and high-Z states remain unaffected by the MIC_BIAS power state.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Digital (DV_{DD})	–0.30 V to +3.65 V
Digital (DV_{CORE})	–0.30 V to +2.10 V
Digital I/O (DV_{IO})	–0.30 V to +3.65 V
Analog (AV_{DD})	–0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	–0.30 V to AV_{DD} +0.3 V
Digital Input Voltage (Signal Pins)	–0.30 V to DV_{IO} +0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	–65°C to +150°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = case temperature in °C
PD = power dissipation in W
θ_{CA} = thermal resistance (case-to-ambient)
θ_{JA} = thermal resistance (junction-to-ambient)
θ_{JC} = thermal resistance (junction-to-case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Package	θ_{JA}	θ_{JC}	θ_{CA}	Unit
LFCSP_VQ	47	15	32	°C/W

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

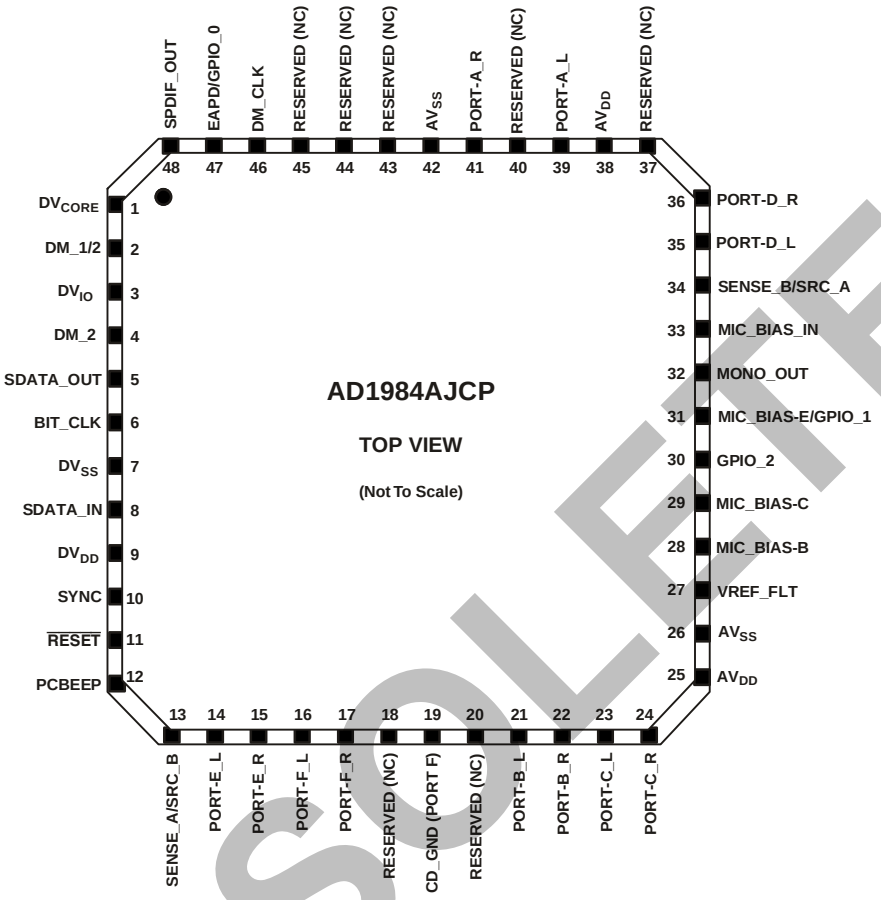

Figure 2. AD1984A 48-Lead Package and Pinout

Table 4. Pin Function Descriptions

Mnemonic	Pin No.	I/O	Description
DIGITAL INTERFACE			
SDATA_OUT	5	I	Link Serial Data Output. AD1984A input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1984A output stream clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
$\overline{\text{RESET}}$	11	I	Link Reset. AD1984A master hardware reset.
DIGITAL I/O and EAPD			
DM_1/2	2	I	Digital Microphone 1 and 2 Inputs (for Biphase Microphones), or Digital Microphone 1 Input (for Single-phase Microphones).
DM_2	4	I	Digital Microphone 2 Input (for Single-phase Microphones).
DM_CLK	46	O	Clock to Drive External Digital Microphones.
GPIO_2	30	I/O	General-Purpose Input/Output Pins. Digital signals used to control or sense external circuitry.
MIC_BIAS-E/GPIO_1	31	I/O	Microphone Bias for Port E/General-Purpose Input/Output. Capable of high-Z, 1.65 V, and 2.86 V. Pin 31 shares functionality between MIC_BIAS_E (default) and GPIO_1. These functions are mutually exclusive and the MIC_BIAS function takes priority over the GPIO function.
EAPD/GPIO_0	47	I/O	EAPD/General-Purpose Input/Output pin. Pin 47 shares functionality between GPIO_0 and EAPD. These functions are mutually exclusive and the EAPD function takes priority over the GPIO function. By default, the pin is in a high-Z state. External resistors should be used to ensure the proper circuit state when this pin is in high-Z.
SPDIF_OUT	48	O	Supports S/PDIF Output.
JACK SENSE			
SENSE_A/SRC_B	13	I/O	Jack Sense A-D Input/Sense B drive.
SENSE_B/SRC_A	34	I/O	Jack Sense E-F Input/Sense A drive.
ANALOG I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO	Auxiliary Input/Output Right Channel.
PORT-F_L	16	LI, LO	Auxiliary Input/Output Left Channel.
PORT-F_R	17	LI, LO	Auxiliary Input/Output Right Channel.
CD_GND (PORT F)	19	I	CD Audio Analog Ground Reference. Must be connected to AGND via a 0.1 μF capacitor if not in use as CD_GND. MUST always be ac-coupled.
PORT-B_L	21	LI, MIC	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC	Rear Panel Stereo MIC/Line-In.
MONO_OUT	32	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-D_L	35	HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	HP, LO	Front Panel Headphone/Line-Out.
PORT-A_R	41	HP, LO	Front Panel Headphone/Line-Out.

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier.

Table 4. Pin Function Descriptions (Continued)

Mnemonic	Pin No.	I/O	Description
FILTER/MIC_BIAS			
VREF _FILT	27	O	Voltage Reference Filter.
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24). Both MIC bias pins are capable of high-Z, 0 V, 1.65 V, 3.7 V, and 3.9 V (with 5.0 V on Pin 33), high-Z, 0 V, 1.65 V, 2.86 V, and 3.0 V (with 3.3 V on Pin 33).
MIC_BIAS_IN 5.0 V or 3.3 V	33	I	Source Power for Microphone Bias Boost Circuitry. Connect this pin to 5.0 V via a low-pass filter. When connected this way the AD1984A is capable of providing 3.9 V as a mic bias to all of the mic bias pins (except on Pin 31). If 5 V is not available, connect this pin to 3.3 V (AV_{DD}) via a low-pass filter.
POWER AND GROUND			
DV_{CORE} 1.7 V to 1.9 V or FILTER	1	I/O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. If Pin 9 is connected to 3.3V DV_{DD}, this pin must be connected to filter caps: 10µF, 1.0 µF, and 0.1 µF connected in parallel between Pin 1 and DV_{SS} (pin 7). Direct, filtered 1.7 V to 1.9 V DV_{DD} may be applied to Pin 1 to lower the digital power requirements. Pin 9 MUST be connected to Pin 1 in this case.
DV_{IO} 1.5 V or 3.3 V	3	I	Link Digital I/O Voltage Reference. 3.3 V ± 10% or 1.5 V ± 5.5%
DV_{SS}	7	I	Digital Supply Return (Ground).
DV_{DD} 1.7 V to 1.9 V or 3.3 V	9	I	Digital Supply Voltage 3.3 V ± 10%. This is regulated down to DV_{CORE} on Pin 1 to supply the internal digital core internal to the AD1984A. Direct, filtered 1.7 V to 1.9 V DV_{DD} may be applied to Pin 1 to lower the digital power requirements. Pin 9 MUST be connected to Pin 1 in this case.
AV_{DD} 3.3 V	25, 38	I	CAUTION: DO NOT APPLY 5 V TO THESE PINS! Analog Supply Voltage 3.3 V ONLY. Note: AV_{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
AV_{SS}	26, 42	I	Analog Supply Return (Ground). AV_{SS} should be connected to DV_{SS} using a conductive trace under, or close to, the AD1984A.

The symbols used in this table are defined as: I = input, O = output, LI = line level input, LO = line level output, HP = output capable of driving headphone load, MIC = input supports microphones with MIC bias and boost amplifier.

DIGITAL MICROPHONE INTERFACE TIMING SPECIFICATIONS

The digital microphone interface can support one or two digital microphones using two or three codec pins. Both uniplex (one microphone per data pin) and multiplex (two microphones sharing the same data pin) are supported. The timing for these configurations is shown in Table 5 and Figure 3, Figure 4 and Figure 5. The interface can generate a microphone clock at 1.5 MHz, 2.0 MHz, or 3.0 MHz to suit quality and power requirements.

Table 5. Microphone Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
Timing Requirements					
t_0	DM_CLK (1.5 MHz) Period		667		ns
	Duty Cycle		50/50		%
t_0	DM_CLK (2.0 MHz) Period		500		ns
	Duty Cycle		50/50		%
t_0	DM_CLK (3.0 MHz) Period		333		ns
	Duty Cycle		50/50		%
t_1	DM_CLK Rise Time			5	ns
t_2	DM_CLK Fall Time			5	ns
t_3	Data Setup to DM_CLK Edge	10			ns
t_4	Data Hold from DM_CLK Edge	5			ns

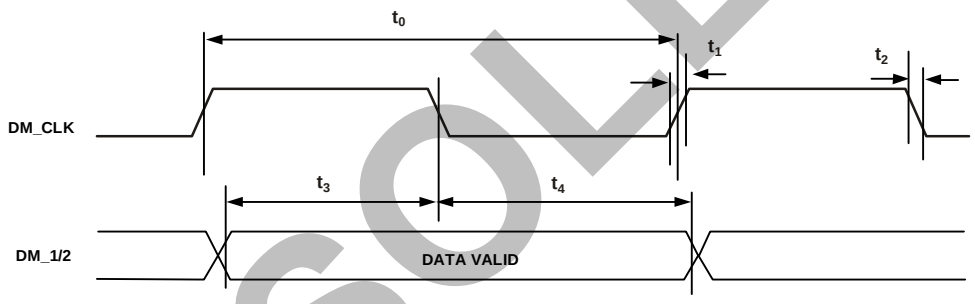

Figure 3. Uniplex Microphone Timing

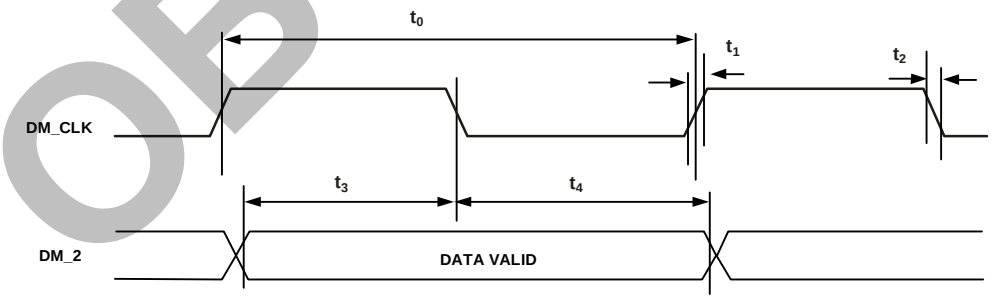

Figure 4. DM_2 Uniplex Microphone Timing

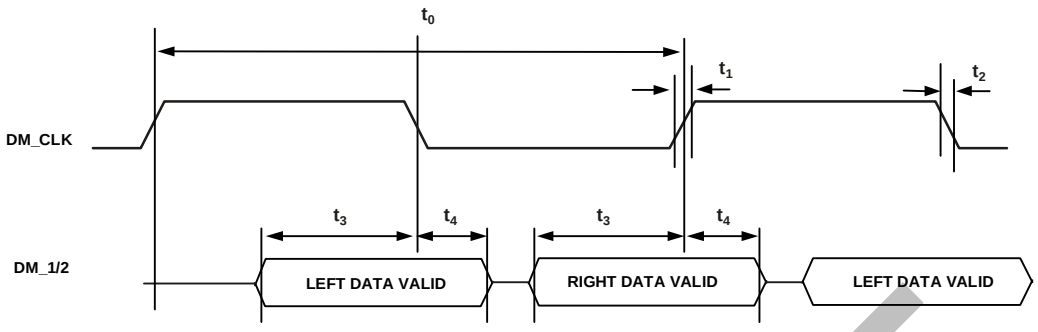

Figure 5. Multiplex Microphone Timing

HD AUDIO WIDGETS

Table 6. HD Audio Widgets[1]

Node ID	Name	Type ID	Type	Description
0x00	ROOT	x	Root	Device identification
0x01	FUNCTION	x	Function	Designates this device as an audio codec
0x02	S/PDIF DAC	0	Audio Output	S/PDIF digital stream output interface
0x03	DAC_0	0	Audio Output	Stereo headphone channel digital/audio converter
0x04	DAC_1	0	Audio Output	Stereo front channel digital/audio converter
0x07	Port A Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port A
0x08	ADC_0	1	Audio Input	Stereo record Channel 0 audio/digital converters
0x09	ADC_1	1	Audio Input	Stereo record Channel 1 audio/digital converters
0x0A	Port D Mixer	2	Audio Mixer	Mixes the DAC_1 and analog mixer output to drive Port D
0x0B	Port F Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port F
0x0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_0
0x0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_1
0x0E	Mono Out Selector	3	Audio Selector	Selects the mono out DAC_(0, 1)
0x0F	Port F Out Selector	3	Audio Selector	Selects the Port F DAC_(0, 1)
0x10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
0x11	Port A (Headphone)	4	Pin Complex	Headphone jack pins
0x12	Port D (Line Out)	4	Pin Complex	Line out jack pins
0x13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
0x14	Port B (Mic In)	4	Pin Complex	Microphone in jack pins
0x15	Port C (Line In)	4	Pin Complex	Line in jack pins
0x16	Port F (Aux In/Out)	4	Pin Complex	Auxiliary I/O pins
0x17	Dig Microphone	4	Pin Complex	Digital microphone input pin
0x19	Mixer Power Down	5	Power Widget	Powers down the analog mixer and associated amps
0x1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
0x1B	S/PDIF-Out	4	Pin Complex	S/PDIF output pin
0x1C	Port E (Dock I/O)	4	Pin Complex	Analog dock I/O pins
0x1D	V_{REF} Power Down	F	Vendor Defined	Powers down the V_{REF} circuitry
0x1E	Mono Out Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive mono out
0x1F	Stereo Mix-Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
0x20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs
0x21	Mixer Output Atten	3	Audio Selector	Attenuates the analog mixer output to drive the port mixers
0x22	Port A Out Selector	3	Audio Selector	Selects the Port A DAC_(0, 1)
0x23	Port E Out Selector	3	Audio Selector	Selects the Port E DAC_(0, 1)
0x24	Port E Mixer	2	Audio Mixer	Mixes the DAC_(0, 1) and analog mixer output to drive Port E
0x25	Port E Mic Boost	3	Audio Selector	0 dB, 10 dB, 20 dB, or 30 dB gain boost for Port E
0x26	BIAS Power Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS pins

[1] All node IDs (NIDs) are sequential in the codec. Any NIDs missing for this table are vendor defined.

HD AUDIO PARAMETERS

Table 7. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	Revision ID 02[1]	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
0x00	ROOT	0x11D4 194A	0x0010 0400	0x0001 0001			
0x01	FUNCTION			0x0002 0029	0x0000 0001	0x0001 0C0C	0x4000 0003

[1] Subject to change with silicon stepping.

Table 8. Subsystem ID

Node ID	Name	Type	Value	31:16 SSID	15:8 SKU	7:0 ASM ID
0x01	FUNCTION	Function	0xBFD4 0000	0xBFD4	0x00	0x00

WIDGET PARAMETERS

Table 9. Widget Parameters

Node ID	Widget Capabilities 0x09	PCM Size, Rate 0x0A	Stream Formats 0x0B	Pin Capabilities 0x0C	Input Amp Capabilities 0x0D	Con. List Length 0x0E	Power States 0x0F	Output Amp Capabilities 0x12
0x01	0x0000 04C0	0x000E 07FF	0x0000 0001		0x8000 0000		0x0000 0009	0x0005 2727
0x02	0x0003 0211	0x000E 07E0	0x0000 0005			0x0000 0000		
0x03	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
0x04	0x0000 0405	0x000E 07FF	0x0000 0001			0x0000 0000	0x0000 0009	0x0005 2727
0x07	0x0020 0103				0x8000 0000	0x0000 0002		
0x08	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
0x09	0x0010 0501	0x000E 07FF	0x0000 0001			0x0000 0001	0x0000 0009	
0x0A	0x0020 0103				0x8000 0000	0x0000 0002		
0x0B	0x0020 0103				0x8000 0000	0x0000 0002		
0x0C	0x0030 010D					0x0000 0006		0x8005 3627
0x0D	0x0030 010D					0x0000 0006		0x8005 3627
0x0E	0x0030 0101					0x0000 0002		
0x0F	0x0030 0101					0x0000 0002		
0x10	0x0070 000C					0x0000 0000		0x800B 0F0F
0x11	0x0040 018D			0x0000 001F		0x0000 0001		0x8000 0000
0x12	0x0040 058D			0x0001 001F		0x0000 0001	0x0000 0009	0x8000 0000
0x13	0x0040 050C			0x0001 0010		0x0000 0001	0x0000 0009	0x8005 1F1F
0x14	0x0040 008B			0x0000 3727	0x0027 0300	0x0000 0000		
0x15	0x0040 008B			0x0000 3727	0x0027 0300	0x0000 0000		
0x16	0x0040 058D			0x0001 0037		0x0000 0001	0x0000 0009	0x8000 0000
0x17	0x0040 020B			0x0000 0020	0x0017 0300	0x0000 0000		
0x19	0x0050 0500					0x0000 0002	0x0000 0009	
0x1A	0x0040 0000			0x0000 0020		0x0000 0000		
0x1B	0x0040 038D			0x0000 0014		0x0000 0001		0x8005 2727
0x1C	0x0040 018D			0x0000 3737		0x0000 0001		0x8000 0000
0x1D	0x00F0 0100					0x0000 000A		
0x1E	0x0020 0103				0x8000 0000	0x0000 0002		
0x1F	0x0020 0100					0x0000 0001		
0x20	0x0020 010B				0x8005 1F17	0x0000 0007		
0x21	0x0030 010D					0x0000 0001		0x8005 1F1F
0x22	0x0030 0101					0x0000 0002		
0x23	0x0030 0101					0x0000 0002		
0x24	0x0020 0103				0x8000 0000	0x0000 0002		
0x25	0x0030 010D					0x0000 0001		0x0027 0300
0x26	0x00F0 0100					0x0000 0003		

CONNECTION LIST

Table 10. Connection List

Node ID	Connections			0	1		2		3		4		5		6		7		8		9	
	[0–3]	[4–7]	[8–11]	NID	R[1]	NID	R	NID	R	NID	R	NID	R	NID	R	NID	R	NID	R	NID	R	NID
0x02																						
0x03																						
0x04																						
0x07	0x0000 2122			0x22		0x21																
0x08	0x0000 000C			0x0C																		
0x09	0x0000 000D			0x0D																		
0x0A	0x0000 2104			0x04		0x21																
0x0B	0x0000 210F			0x0F		0x21																
0x0C	0x2016 1514	0x0000 1725		0x14		0x15		0x16		0x20		0x25		0x17								
0x0D	0x2016 1514	0x0000 1725		0x14		0x15		0x16		0x20		0x25		0x17								
0x0E	0x0000 0403			0x03		0x04																
0x0F	0x0000 0403			0x03		0x04																
0x10																						
0x11	0x0000 0007			0x07																		
0x12	0x0000 000A			0x0A																		
0x13	0x0000 001F			0x1F																		
0x14																						
0x15																						
0x16	0x0000 000B			0x0B																		
0x17																						
0x19	0x0000 2120			0x20		0x21																
0x1A																						
0x1B	0x0000 0002			0x02																		
0x1C	0x0000 0024			0x24																		
0x1D	0x118F 0A07	0x1C1A 1996	0x0000 A61E	0x07		0x0A	1	0x0F		0x11	1	0x16		0x19		0x1A		0x1C		0x1E	1	0x26
0x1E	0x0000 210E			0x0E		0x21																
0x1F	0x0000 001E			0x1E																		
0x20	0x1A16 1514	0x004 0325		0x14		0x15		0x16		0x1A		0x25		0x03		0x04						
0x21	0x0000 0020			0x20																		
0x22	0x0000 0403			0x03		0x04																
0x23	0x0000 0403			0x03		0x04																
0x24	0x0000 2123			0x23		0x21																
0x25	0x0000 001C			0x1C																		
0x26	0x001C 1514			0x14		0x15		0x1C														

[1] R = the MS bit of any node ID indicates a 2-tuple NID pair delineating a continuous range of nodes. If the MS bit is set (=1), that list entry forms a range of entries from the previous NID to the current NID. For additional information, see chapter 7.1.2, "Node Addressing" in the *High Definition Audio Specification*.

DEFAULT CONFIGURATION BYTES

Table 11. Default Configuration Bytes

			31:30	29:28	27:24	23:20
				Location		
Node ID	Name	Value	Connectivity	Chassis	Position	Def. Device
0x11	Port A (Headphone)	0x0321 40F0	Jack	External	Left	HP Out
0x12	Port D (Line Out)	0x2121 4010	Jack	Separate	Rear	HP Out
0x13	Mono Out	0x9017 01F0	Fixed	Internal	N/A	Speaker
0x14	Port B (Mic In)	0x03A1 90F0	Jack	External	Left	Mic In
0x15	Port C (Line In)	0xB7A7 0121	Fixed	Other	Special 1	Mic In
0x16	Port F (Aux In/Out)	0x9933 012E	Fixed	Internal	Special 3	CD
0x17	Dig Mic Pin	0x97A6 01F0	None	Internal	Special 1	Mic In
0x1A	Analog PCBeep	0x90F3 01F0	Fixed	Internal	N/A	other
0x1B	S/PDIF Out-1	0x0145 10F0	Jack	External	Rear	SPDIF Out
0x1C	Port E (Dock I/O)	0x21A1 9020	Jack	Separate	Rear	Mic In

Table 11. Default Configuration Bytes (Continued)

			19:16	15:12	8	7:4	3:0
Node ID	Name	Value	Conn Type	Color	JD OVRD	Def Assn.	Seq.
0x11	Port A (Headphone)	0x0321 40F0	1/8″ Jack	Green	0	0xF	0x0
0x12	Port D (Line Out)	0x2121 4010	1/8″ Jack	Green	0	0x1	0x0
0x13	Mono Out	0x9017 01F0	Other Analog	Unknown	1	0xF	0x0
0x14	Port B (Mic In)	0x03A1 90F0	1/8″ Jack	Pink	0	0xF	0x0
0x15	Port C (Line In)	0xB7A7 0121	Other Analog	Unknown	1	0x2	0x1
0x16	Port F (Aux In/Out)	0x9933 012E	ATAPI	Unknown	1	0x2	0xE
0x17	Dig Mic Pin	0x97A6 01F0	Other Digital	Unknown	1	0xF	0x0
0x1A	Analog PCBeep	0x90F3 01F0	ATAPI	Unknown	1	0xF	0x0
0x1B	S/PDIF Out-1	0x0145 10F0	Optical	Black	0	0xF	0x0
0x1C	Port E (Dock I/O)	0x21A1 9020	1/8″ Jack	Pink	0	0x2	0x0

OUTLINE DIMENSIONS

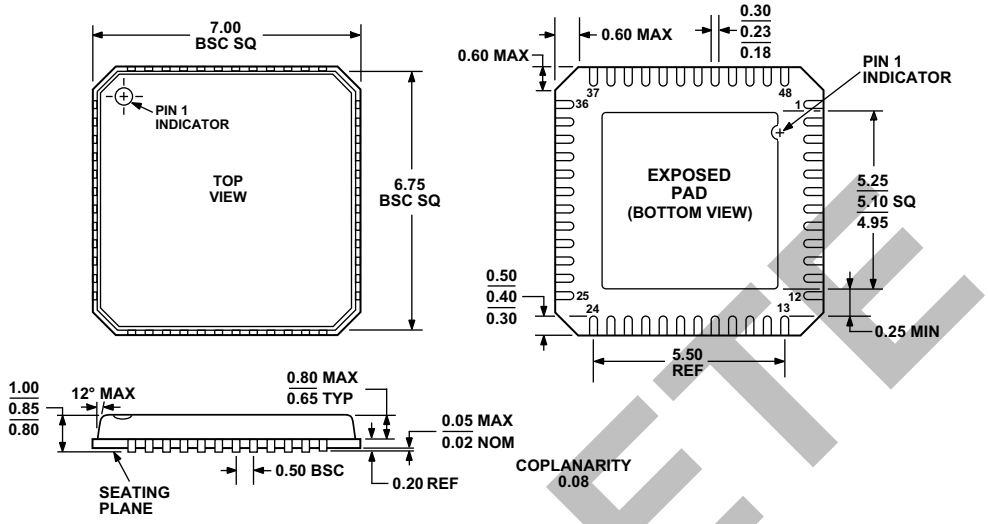

Figure 6. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm x 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1984AJCPZ[1]	0°C to 70°C	48-Lead LFCSP_VQ	CP-48-1
AD1984AJCPZ-RL[1]	0°C to 70°C	48-Lead LFCSP_VQ, 13″ Tape and Reel	CP-48-1

[1] Z = RoHS Compliant Part.

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